NVIDIA®

Data Sheet

GoForce 4000
Media Processor

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Revision History

Date	Revision	Description
11/14/03	Advance Release, v01	First version of Data Sheet for SC4.
12/12/03	Advance Release, v02	Chapter 3: Added mechanical drawing. Chapter 2: Removed voltage level from pin description/power and ground planes. Put note with each section telling which power plane was used with the pins in that section. Added new VI pins. Added detailed descriptions to pin names (in tables) - descriptions were formerly part of Technical Manual. This consolidated the pin/signal description information.
1/30/04	Advance Release, v03	Chapter 2: Added Byte Enable (Write Enable) [3:2] signal information for Type A, Type B, and Type C interfaces: was missing from v02. Chapter 3: Added: Type A, Type B, and Type C Host Interface TIming DIagrams, timing parameter tables.
2/9/04	Advance Release, v04	Chapter 3: New mechanical drawing: changes to several dimensions, shown in Table 3.43. Added Table 3.10: lists timing diagrams and pages for customer reference. Chapter 2: BGP0 description: Added AUDIOCLK: for synchronization of audio and video when MPEG-4 encoding. Added: BGP0 can be used to test clock signals.
3/9/04	Advance Release, v05	Chapter 2: Video Input Pins: Was: VGP[4:3] used as ICSK and ICSDA. This was incorrect (change to registers as well.) Is: VGP1 = ICSK when SSP enabled, otherwise general purpose video pin. VGP2 = ICSDA when SSP enabled, otherwise general purpose video pin. Ch 3: TImings: spec change for Trdl and Tracc to: 4*mclk + 35 ns (memory read) 45 ns (register read) Tds = 20 ns. Indirect Timing Diagrams: Register Mapping: D[2], D[1], and D0 changed (corrected) for ADDR2 and ADDR3. Memory Mapping: Added A19 to tables, was missing. OSCI/OSCO: oscillation frequency range changed was: 2 to 6 MHz Is: 2 to 13 MHz

Date	Revision	Description
4/19/04	Advance Release, v06	Chapter 3: Figure 3.23, 3.25, and 3.41: each of these is a direct addressing timing diagram. The note below each diagram states, "To perform Burst Read operations as shown in Figure 3.41 set DC01[8] = 1." This is not correct. Direct addressing does not need auto-incrementing, which is enabled by DC01[8]. The note was removed. Changes to timing diagrams: All references to Burst/Page mode (above diagrams) were removed and replaced with Burst. These are burst timings, not Burst/Page timings. Timing definitions type A: Removed: Twrlaind, Twrasidn, Twrldind, Twrdsind, Twrhaind, Twrlaind, and Twrasind. Not used. Changed: Twras to be defined with reference to the falling edge, not rising edge. Timing definitions type B: Removed: Tasash, Twrasind, Twrlaind, and Twrldind. Changed: Twras to be defined with reference to the falling edge, not rising edge. Timing definitions type C: Removed: Twrlaind, Twrasind, and Twrldidn Changed: Twras to be defined with reference to the falling edge, not rising edge. Removed Tj, junction temperature, information: is not useful data. Timing Diagrams: Corrections to diagrams. Many showed ASn transitioning after CSn, which was wrong. Changed to show ASn transitions first. Setup time parameters corrected to match. Corrections to timing diagrams caused some timing labels to be deleted, some to be moved. Please refer to all timing diagrams of this version, v06, to ensure use of correct timing diagrams. Removed all Type B Burst Timings: not supported. Corrected waveforms where Address was valid after CSn/WRn, etc. Should go valid before. Removed Tdh from all Read diagrams.
6/04/04	Preliminary Release, v07	Flat Panel GPIOs: FGP13 and FGP14 were missing (chapter 2), Table 2.8. Chapter 3: Type A, Type B, and Type C Host Interface Timing parameters were updated, format of tables changed for legibility.
6/24/04	Preliminary Release, v08	Chapter 2: Corrected typo in Table 2.12, Miscellaneous Pins. BGP3 information was missing. An extra line in the table between the MD[2:0] and corresponding BGP pin information made it look like MD[2:0] and BGP[3:1] were on different pins (balls); they are not. Added note to Table 2.9, Clock Interface Pins: The external clock source (NOT the external crystal - this is when the crystal is bypassed) can be in the 2 MHz to 50 MHz range.
8/17/04	Preliminary Release, v09	Changed all references to VCLK max frequency from 72 MHz to 54 MHz. Changed all references to VCLK min cycle time from 13.9 ns to 18.5 ns. (See Page 1-3 under VI features, Table 2.7, and Table 3.38.) Removed fps references.
9/24/04	Preliminary Release, v10	Section 3.4.4, Table 3.38: VCLK pulse width specified for low and high pulse width separately. Previously min pulse width was only true for low pulse. VCLK rise/fall transition time was on same level in table as VCLK pulse width and made it look like the max value was 2 ns. VCLK rise/fall transition time was removed, low pulse width is 6 ns min, and high pulse width is 10.5 ns min.
10/22/04	Preliminary Release, v11	Table 3.3: Changed VDD to VDDcore for clarity. (Not a change, just better explanation.) Removed all references to Twraswaitn in chapter 3: It is an undefined and uneeded timing parameter. Removed Idd value: it is TBD (Table 3.3) Added GoForce 4000 Rev B Silicon information
11/17/04	Preliminary Release, v12	Table 3.38: Rev A/Rev B parameters were not clearly spec'd. Clarified.

Date	Revision	Description
11/29/04	Preliminary Release, v13	Chapter 3: Value for Tracc has a value added, the same in all 3 host interface types: Tracc: Added timing value for FIFO Status Registers
03/23/05	Preliminary Release, v14	Chapter 3: Added information for RevB power sequencing: Power supply, power off, and PORn sequencing.
04/06/05	Preliminary Release, v15	Chapter 3: Figure 3.63: Changed parameters for Tpvcw to show Tpvcwl and Tpvcwh (low and high, respectively.) Table 3.40: Added rev B information to timing parameters for Tpvcwl and Tpvcwh. Previously showed only rev A values. Added Tpvct: VCLK rise/fall transition times. (They are equal.)
08/16/05	v16	Chapter 3: Added note (below Table 3.40) defining requirements for Tpvct period.
12/08/05	v17	Chapter 3: Section 3.4.3.2 Table 3.10: Changed Tmin for power on sequencing (delay between CVDD power on and the remaining power supplies) to 1 ms. Removed Typical and Maximum columns from the table: these do not apply.

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Chapter 1 Overview

1.1 Introduction

NVIDIA's® GoForce™ products set the standard for high performance, low power media processors for advanced multi-media handheld devices. The GoForce 4000 is the latest entry in the product line and enables the user to capture, view and share high quality images and video anytime, anywhere with the device they always carry with them.

Creating a high resolution, fluid-motion video used to require a camcorder. The GoForce 4000 makes it possible to capture high quality video with a cell phone. A hardware-based MPEG-4 encoder captures video, using a proprietary diamond search algorithm and hardware rate control which produce high quality video with a minimum of artifacts, even at low bit rates. Software-based solutions running on a CPU dissipate up to 10 times as much power; and may still not equal the frame rate, resolution, or visual quality provided by the GoForce 4000.

A hardware-based video decoder allows you to watch the video you just recorded, or any other MPEG-4 clip or streaming video. As with the encoder, handling the computationally intensive operations in hardware dramatically extends the battery life of the handheld device. This could mean the difference between being able to watch just a single music video on a CPU-based solution, and an entire movie on GoForce 4000. Not only will the video play back longer, it can be scaled and rotated to fit your screen with the video scaler, and contain fewer visible artifacts after passing through post processing filters, which incorporate deblocking and deringing.

In addition to recording and watching video, the full hardware codec in the GoForce 4000 makes video conferencing possible anytime, anywhere.

Removable storage is especially important in handheld devices for archiving and transferring megapixel images and high quality video clips. To meet this need, the GoForce 4000 features an integrated SD/SDIO host controller that supports both 1-bit and 4-bit interfaces. In addition to storing photographic quality images, SD cards can also be used to play back video clips, movie trailers, TV shows, or even full length movies which were recorded on another device. The SDIO slot may be used to enable wireless connections, such as Bluetooth, via card.

To show as much information as possible on the screen, the GoForce 4000 is designed to support an industry-leading VGA (640x480) resolution LCD, at 16-bpp using only an embedded frame buffer. Double buffering is supported at resolutions up to HVGA. Over 75 different models of LCD displays are supported by a programmable display interface which is capable of handling new displays as they become available.

The GoForce 4000 supports 3MP cameras with resolutions up to 2048x1536, for true photographic-quality image capture with preview. No external crystal or oscillator is required to drive the camera when it is connected to the GoForce 4000, saving both board space and cost.

The enhanced 8-bit ITU-R 656-compliant Video Input (VI) supports both CCD and CMOS camera modules. A video hardware processing engine handles both color space conversion and image scaling. During decimation, horizontal averaging and low-pass filtering are performed, in addition to vertical averaging, to provide a smooth preview image, free of artifacts. Camera programming and control is supported by a synchronous serial bus (SSB) interface. This provides such advantages as allowing the resolution of the camera to be changed quickly, enabling the user to preview at a lower resolution (for increased frame rates and reduced camera power consumption), while capturing the final image at the highest possible quality.

To create a high quality camera phone, the GoForce 4000 controller offers advanced filtering features to give a crisp preview image. The fine-grained 8X digital zoom functionality of GoForce 4000 is comparable to that of digital still camera. Picture compositing, album, and other camera applications are possible at amazing speed.

The video processing engine is coupled with a JPEG encoder capable of encoding still images with 3MP resolution. The computationally intensive JPEG decoding task is handled by a dedicated hardware engine which can decode images with amazing speed. To capture motion video, the GoForce 4000 JPEG codec can record and playback motion JPEG.

The GoForce 4000 contains an industry leading 640 KB of embedded SRAM. The size of this internal memory was carefully selected to support all of the advanced functions, from driving a VGA display to video conferencing at CIF resolution video or capturing a 3MP image. Embedded memory uses dramatically less power than external memory, provides significantly higher bandwidth and performance, and saves both board space and system cost.

The host bus interface of GoForce 4000 is both flexible and fast. It provides an 8, 16, or 32-bit asynchronous interface that supports both direct and indirect addressing modes. ARM® and Dragonball™ type processor interfaces are supported.

The GoForce 4000 flexible clocking features allow each module in the chip to operate at a different frequency. This means that each hardware engine needs to run only as fast as required, at any given time, to accomplish its tasks. This, along with a feature that automatically turns off unused stages of pipelines, dramatically reduces power consumption. Additionally, a digital bypass mode means the GoForce 4000 can use a clock generated by a baseband or CPU which can eliminate the need for an external crystal or oscillator.

The GoForce 4000 brings true photographic-quality 3MP imaging and camcorder-quality CIF movie capture and playback to handheld devices such as cell phones and PDAs. Video conferencing at QCIF resolution can now be done anywhere, anytime. Proprietary algorithms and filtering techniques result in superb image quality, both during image preview and video playback. VGA resolution LCDs are supported from an internal frame buffer. A built-in interface for SD cards let you share and store multi-media content. Embedded memory, 0.15µ low-leakage process, flexible clocking, and dedicated hardware engines provide all these high performance features while actually reducing the overall power consumption of the system.

1.2 Features

- **MPEG-4 / H.263 Hardware Codec**
  - Full duplex
  - MPEG4 Simple Profile, Level 1, 2, 3
  - H.263 support
  - Back-end MPEG4 video processing including hardware color space conversion and image scaling
  - De-blocking and de-ringing filters to
  - reduce the visibility of compression
  - artifacts during playback
- **JPEG Hardware Codec**
  - Motion JPEG capture/playback for VGA resolution
  - Low shutter lag (two frame maximum)
  - Composite, framing, and overlay
  - Thumbnail support (store both image and thumbnail in same file)
  - Hardware Huffman decode for JPEG
  - Programmable Q-table
  - Hardware DCT, RLE, and Huffman encoding
  - Output from JPEG Decode to host CPU interface in YUV format (Rev B only)
- **High Resolution Color Display**
  - Support for VGA (640 x 480) LCD
  - Double-buffering support on HVGA
  - Fast switching between main/sub-LCD
  - Hardware support for sub-LCD display
  - 18-bpp panel support
- **SD/SDIO Host Controller**
  - 1 bit and 4 bit SD/SDIO
  - Support for storage or Bluetooth cards
  - Store directly to SD card in continuous JPEG encode mode
- **Video Input**
  - 3MP camera module support
  - ITU-R 656-compliant 8-bit interface
  - Horizontal scaling with horizontal averaging and low-pass filtering
  - Vertical averaging
  - Synchronous serial bus (SSB) for camera control & programming
  - 54 MHz output to drive the camera master clock
  - YUV422 to RGB565 color space conversion
  - Single and double buffering support
  - Double buffering synchronization with graphics controller
  - Fine-grained digital zoom, up to 8X
- **64-Bit 2d Graphics Acceleration**
  - BitBLT with 256 3-operand raster operations
  - Video scaling with range of 8x expansion to 1/60th contraction
  - Mono and solid pattern
  - Mono-to-color expansion
  - Mono source/pattern transparency
  - Destination read/write color transparency
  - All angle (Bresenham) line draw
  - Rectangle fill
  - Alpha blending (Rev B only)
- **Flat Panel (LCD) Interface**
  - Direct interface to LCD drivers with embedded memory
  - Built-in timing generator
  - Color FRC S-STN at 4, 8, and 16 bits/clock
  - Color PWM S-STN at 9 and 12 bits/clock
  - Color TFT at 9, 12, 16 and 18 bit/clock
  - Partial pixel per clock mode
  - Up to 16-level FRC and up to 4-bit spatial dithering
  - CPU, RGB, Serial, NEC M-CMADS, AMLCD, LTPS, and Sharp ULC display support

- **Graphics Controller**
  - Hardware rotation (90˚, 180˚, and 270˚)
  - Flip and mirror
  - Partial display support (any size/position)
  - Triple 6-bit look-up-table
  - Overlay support
  - Encode predefined region of display
- **Integrated 640kB 64-bit SRAM**
  - 640KB of 64-bit wide on-board frame, video, and transactional buffers minimize external bus traffic and significantly reduce system power
- **32-Bit Flexible Host Bus Interface**
  - Indirect and direct addressing support
  - 8/16/32-bit asynchronous interface for base-band processors (ARM based)
  - MDB-style (Dragonball) 8-bit and 16-bit mode
  - Burst mode support
  - Fixed and variable latency host bus
- **Clock Options**
  - On-chip oscillator for 2 MHz to 13 MHz crystals
  - Digital bypass mode for external clock sources (e.g. baseband or CPU)
  - Low-power relaxation oscillator
  - On-chip PLL with VCO range of 50 MHz to 100 MHz (Rev A) and 20 MHz to 200 MHz (Rev B)
- **Advanced Power Management**
  - Fully-static CMOS technology
  - Low-Leakage process
  - Individual module enables
  - Automatic shut-off of unused pipeline stages
- **Packaging & Power**
  - 168-pin BGA, 10 x 10mm, 0.65mm ball spacing, 1.2mm height (GoForce 3000 compatible with one extra row)
  - JTAG boundary scan
  - 1.425 V to 1.57 V core, 1.71 V to 3.60 V I/O
- **Serial Peripheral Bus**
  - Convenient communication among system components using a two-wire interface
  - Operation in Standard and Fast modes
  - Combined 7 bit and 10 bit addressing
  - Programmable transfer count for transmit and receive
  - Clock synchronization for multi-master environments

Chapter 2 Signals

2.1 Introduction

This chapter provides a description of the GoForce 4000 pins. The first section provides an overview of the pin types and the conventions used in the descriptions. In the subsequent section, the signals are grouped by module or functionality and described in alphabetic order.

2.2 Pin Types and Conventions Used

Table 2.1 provides notations that indicate valid pin types.

Table 2.1: Pin Types

Pin Type	Pin Type Description
I	CMOS Input Pin.
IS	Schmitt-Trigger CMOS Input Pin.
O	CMOS Output Pin.
OD	Open-Drain Output
I / O	Bi-Directional CMOS Input / Output Pin.
IS / O	Bi-Directional CMOS Input / Output Pin with Schmitt-Trigger CMOS Input Pin.
A	Analog Pin.
AI	Analog Input Pin.
AO	Analog Output Pin.
P	Power (VDD) Pin.
G	Ground (GND) Pin.

The following conventions are used:

- Inputs and outputs are all CMOS buffers.
- A lower case “n” at the end of a pin name indicates an active low signal.
- Output buffer drive strength is specified in mA for operation at 3.3V.

2.3 Power and Ground Pins

Table 2.2: Power and Ground Pins

Name	Type	Drive (mA)	Pin Description
CVDD	P	-	Power for Core Logic and Embedded SRAM, Crystal Oscillator, Relaxation Oscillator, and Internal PLL
BVDD	P	-	Power for Host Bus Interface
FVDD	P	-	Power for Flat Panel Interface
VVDD	P	-	Power for Video Interface
SDVDD	P	-	Power for Secure Digital and JTAG pins
GND	G	-	Ground Pin

2.4 Host Bus Interface Pins

The Host Bus Interface Pins are referenced to BVDD. Three types of fixed latency and variable-latency bus interfaces are supported; Type A, Type B, and Type C; each in 8bit, 16bit, and 32bit widths.

The Type A host interface has separate signals for write and read cycle control (WRn and RDn respectively). If the BEns are active, they control enabling bytes for write cycles.

The Type B host interface utilizes one control signal (RD/WR_n) to indicate a write or a read cycle; the low state (0) indicates write, high (1) indicates read. Separate data strobe signals are used for each byte.

The Type C host interface also utilizes one control signal for write and read (OEn); the low state indicates read, the high state indicates write. Separate write enable signals are utilized for each byte. Note that GoForce 4000 ball labeled WRn does not map to a signal used when interfacing to Type C Hosts. Tie it low externally when using Type C interfaces.

Table 2.3: Host Bus Interface Pins Overview

Ball Name	Type A	Type B	Type C
CSn	CSn	ASn	CSn
D[31:0]	D[31:0]	D[31:0]	D[31:0]
A[19:1] [1]	A[19:1]	A[19:1]	A[19:1]
BEn0 [2]	BEn0	DSn0	WEn0
BEn1 [3]	BEn1	DSn1	WEn1
A1	BEn2	DSn2	WEn2
BEn3 [4]	BEn3	DSn3	WEn3
RDn	RDn	CS	OEn
WRn [5]	WRN	RD / WRn	- [5]
INTRn [6]	INTRn	INTRn	INTRn
RDYn	RDYn	RDYn	RDYn

1. A1 is used as BEn2 during 32-bit mode;
2. Tie BEn0 to ground for eight-bit type-A style host interfaces. If type-B or type-C 8-bit host interfaces already drive BEn0 (or DSn0 or WEn0, respectively), tie BEn0 (or DSn0 or WEn0) to the related host pin.
3. BEn1 serves as address bit 0 (A[0]) with all the supported eight-bit host interfaces.
4. Tie BEn3 low for 16bit mode. It is only used during 32-bit mode.
5. Tie the WRn pin to low externally with type-C style host interfaces.
6. The polarity of INTRn is controlled by Register DC0B[2].

Note: Tie all remaining unused pins high or low.

Table 2.4: Type A Style Bus Interface Pins

Pin Name	Pin Type	Drive (mA)	Pin Description
A[19:1]	IS	-	**Host Address Bus** This bus is driven constantly by the host. direct addressing mode: Host drives address bus with a valid word address during both read and write accesses. GoForce 4000 direct addressing mode, 32bit Host Address Bus: A1 is used as BEn2. GoForce 4000 indirect addressing mode: Host drives A[1] only, all the time, to indicate whether the host cycle is for data transfer or address transfer.
BEn3	IS	-	**Byte Write Enable 3 (Active Low)** Asserted by a 32bit host during write cycles to enable byte data writes [31:24]. Tie BEn3 low externally for 8bit and 16bit host interfaces.
BEn2	IS	-	**Byte Write Enable 2 (Active Low)** Asserted by a 32bit host during write cycles to enable byte data writes [23:16]. A1 becomes BEn2 when the Host Address Bus is 32 bits wide.
BEn[1:0]	IS	-	**Byte Write-Enable [1:0] (Active Low)** Asserted by a 16-bit host during write cycles to enable byte data writes. For an 8-bit host interface, tie BEn0 to low connect BEn1 to Address bit 0 (A[0]).
CSn	IS	-	**Chip Select (Active Low)** Asserted by the host to activate the host cycles for the GoForce 4000. The GoForce 4000 decodes the other host inputs only when this signal is asserted.
D[31:16]	IS / O	8	**Host Data Bus Bits [31:16]** For a 32bit host bus interface: Data bus driven by the host during write accesses and by the GoForce 4000 during read accesses. These pins are tri-stated during reset, and when an 8bit or a 16bit host interface is used.
D[15:8]	IS / O	8	**Host Data Bus Bits [15:8]** For a 16bit host bus interface, this data bus is driven by the host during write accesses and driven by the GoForce 4000 during read accesses. These pins are tri-stated during reset, and when an 8-bit host interface is used.
D[7:0]	IS/O	8	**Host Data Bus Bits [7:0]** This data bus is driven by the host during write access and driven by the GoForce 4000 during read access. These pins are tri-stated during reset.
INTRn BGP5	OD IS / O	8	**Interrupt Request Line (Programmable Polarity)** This is the interrupt request from the GoForce 4000 to the host interface. **General Purpose Bus Input Output Bit 5** After reset, this pin can be configured as a general-purpose input/output pin. This pin is powered by BVDD.
RDn	IS	-	**Read (Active Low)** This signal is asserted by the host for a read cycle and is valid throughout the read cycle. This signal must be de-asserted for a host write cycle.
RDYn WAITn BGP4	OD OD IS / O	8	**Ready (Active Low)** If the GoForce 4000 is configured for active low ready handshake mode: The GoForce 4000 de-asserts RDYn at the appropriate time during CPU read/write access to request additional wait states. The GoForce 4000 then asserts RDYn until the ongoing host cycle is completed. **Wait (Active Low)** If the GoForce 4000 is configured for active low wait handshake mode: GoForce 4000 asserts WAITn at the appropriate time during CPU read/write access to request additional wait states. The GoForce 4000 then asserts WAITn until the ongoing host cycle is completed. **General Purpose Bus Input Output Bit 4** After reset, this pin can be configured as a general-purpose input/output pin. This pin is powered by BVDD.
WRn	IS	-	**Write (Active Low)** Asserted by the host for a write cycle, WRn stays valid throughout the write cycle. WRn must be de-asserted for a host read cycle.

Table 2.5: Type B Style Bus Interface Pins

Pin Name	Pin Type	Drive (mA)	Pin Description
A[19:1]	IS	-	**Host Address Bus** This bus is driven constantly by the host. GoForce 4000 direct addressing mode: Host drives address bus with a valid word address during both read and write accesses. GoForce 4000 direct addressing mode, 32bit Host Address Bus: A1 is used as DSn2. GoForce 4000 indirect addressing mode: Host drives A[1] only, all the time, to indicate whether the host cycle is for data transfer or address transfer.
DSn3	IS	-	**Data Strobe 3 (Active Low)** Asserted by a 32bit host during write cycles to enable byte data writes [31:24]. Tie DSn3 low externally for 8bit and 16bit host interfaces.
DSn2	IS	-	**Data Strobe 2 (Active Low)** Asserted by a 32bit host during write cycles to enable byte data writes [23:16]. A1 becomes DSn2 when the Host Address Bus is 32 bits wide.
DSn1	IS	-	**Data Strobe 1 (Active Low)** This signal is asserted by a 16-bit host during read/write cycles in order to indicate byte [15:8] data read/write. This signal is used as Address bit 0 by 8-bit host interfaces.
DSn0	IS	-	**Data Strobe 0 (Active Low)** This signal is asserted by the host during read/write cycles in order to indicate byte [7:0] data read/write. The GoForce 4000 uses DSn0 as a byte enable signal for writes. If an 8-bit host is not driving this signal, tie this input of the GoForce 4000 to low externally, or to the related host pin.
ASn	IS	-	**Address Strobe (Active Low)** Driven by the host to indicate a read or a write cycle. The GoForce 4000 decodes other inputs only when this signal is asserted.
CS	IS	-	**Chip Select** Asserted by the host to select the GoForce 4000.
D[31:16]	IS/O	8	**Host Data Bus Bits [31:16]** For a 32bit host bus interface: Data bus driven by the host during write accesses and by the GoForce 4000 during read accesses. These pins are tri-stated during reset, and when an 8bit or a 16bit host interface is used.
D[15:8]	IS / O	8	**Host Data Bus Bits [15:8]** For a 16-bit host bus interface, this data bus is driven by the host during write access and driven by the GoForce 4000 during read access. These pins are tri-stated during reset, and when an 8-bit host interface is used.
D[7:0]	IS / O	8	**Host Data Bus Bits [7:0]** This data bus is driven by the host during write access and driven by the GoForce 4000 during read access. These pins are tri-stated during reset.
INTRn BGP5	OD IS / O	8	**Interrupt Request Line (Active Low)** This generates an interrupt request from the GoForce 4000 to the host interface. **General Purpose Bus Input Output Bit 5** After reset, BGP5 can be configured as a general-purpose input/output pin, BGP5 is powered by BVDD.
RD / WRn	IS	-	**Read (Active High) / Write (Active Low)** This signal is driven high by the host for read accesses to the GoForce 4000 and driven low by the host for write accesses to the GoForce 4000.
RDYn WAITn BGP4	OD OD IS / O	8	**Ready (Active Low)** If the GoForce 4000 is configured for active low ready handshake mode: the GoForce 4000 de-asserts RDYn at the appropriate time during CPU read/write access to request additional wait states. The GoForce 4000 then asserts RDYn until the on-going host cycle is completed. **Wait (Active Low)** If the GoForce 4000 is configured for active low wait handshake mode, the GoForce 4000 asserts WAITn at the appropriate time during CPU read/write access to request additional wait states. After asserting WAITn, the GoForce 4000 de-asserts WAITn until the on-going host cycle is completed. **General Purpose Bus Input Output Bit 4** After reset, this pin can be configured as a general-purpose input/output pin. This pin is powered by BVDD.

For Type B bus interfaces, the first access to the GoForce 4000 is a register write cycle to program DC01[1:0] = 1. This selects the Type-B style bus interface.

Table 2.6: Type-C Style Bus Interface Pins

Pin Name	Pin Type	Drive (mA)	Pin Description
A[19:1]	IS	-	**Host Address Bus** This bus is driven constantly by the host; it must be driven with a valid word address during read and write accesses if the GoForce 4000 is configured in direct addressing mode. If the GoForce 4000 is configured in indirect addressing mode only A[1] is driven by the host all the time to indicate if the host cycle is for data transfer or address transfer.
WEn3	IS	-	**Write Enable 3 (Active Low)** Asserted by a 32bit host during write cycles to enable byte data writes [31:24]. Tie WEn3 low externally for 8bit and 16bit host interfaces.
WEn2	IS	-	**Write Enable 2 (Active Low)** Asserted by a 32bit host during write cycles to enable byte data writes [23:16]. A1 becomes WEn2 when the Host Address Bus is 32 bits wide.
WEn1	IS	-	**Write Enable 1 (Active Low)** Asserted by a 16-bit host during write cycles to indicate upper byte data write enable. This signal is used as Address bit 0 by 8-bit host interfaces.
WEn0	IS	-	**Write Enable 0 (Active Low)** Asserted by the host during write cycles to indicate lower byte write enable. Tie this input of the GoForce 4000 to the related host pin.
CSn	IS	-	**Chip Select (Active Low)** This signal is driven by the host to select the GoForce 4000. The GoForce 4000 decodes the other host control inputs only when this signal is asserted.
D[31:16]	IS/O	8	**Host Data Bus Bits [31:16]** For a 32bit host bus interface: Data bus driven by the host during write accesses and by the GoForce 4000 during read accesses. These pins are tri-stated during reset, and when an 8bit or a 16bit host interface is used.
D[15:8]	IS / O	8	**Host Data Bus Bits [15:8]** For 16-bit host bus interface, this data bus is driven by the host during write access and by the GoForce 4000 during read access. These pins are tri-stated during reset, and when an 8-bit host interface is used.
D[7:0]	IS / O	8	**Host Data Bus Bits [7:0]** This data bus is driven by the host during write access and by the GoForce 4000 during read access. These pins are tri-stated during reset.
INTRn BGP4	OD IS / O	8	**Interrupt Request Line (Active Low)** This generates an interrupt request from the GoForce 4000 to the host interface. **General Purpose Bus Input Output Bit 4** After reset, this pin can be configured as a general-purpose input/output pin. This pin is powered by BVDD.
OEn	IS	-	**Output Enable (Active Low)** This signal is driven low by the host for read access to this chip and driven high by the host for write access to this chip.
RDYn WAITn BGP3	OD OD IS / O	8	**Ready (Active Low)** If the GoForce 4000 is configured for active low ready handshake mode: the GoForce 4000 de-asserts RDYn at the appropriate time during CPU read/write access to request additional wait states. The GoForce 4000 then asserts RDYn until the on-going host cycle is completed. **Wait (Active Low)** If the GoForce 4000 is configured for active low wait handshake mode: the GoForce 4000 asserts WAITn at the appropriate time during CPU read/write access to request additional wait states. After driving low, the GoForce 4000 then asserts WAITn until the on-going host cycle is completed. **General Purpose Bus Input Output Bit 3** After reset, this pin can be configured as a general-purpose input/output pin. This pin is powered by BVDD.

2.5 Video Input Pins

Table 2.7 lists and provides a brief description of the VI Interface signals. The VI pins are referenced to VVDD.

Table 2.7: Video Input Pins

Pin Name	Type	Drive (mA)	Description
VCLK VGP13	IS / O	8	**Video Input Clock** This clock is used to latch video input data. This signal can be programmed as either input or output. On reset, this pin is tri-stated with its input disabled. When using this pin as an clock signal input, the clock frequency must not exceed 54 MHz for Rev A, or 72 MHz for Rev B. **Video General Purpose Input/Output 13** This pin can be used as general-purpose input/output.
VSNCLK VGP0	O IS / O	12	**Video Sensor Master Clock** **Video General-Purpose Input/Output 0**
VGP[2:1] ICSCK ICSDA	IS / O	12	**Video General Purpose Input/Output** These pins are used as general-purpose input/output. Upon reset, these pins are tri-stated and their input buffers are disabled. **ICSCK** When SSP is enabled VGP1 is the SSP Clock pin. **ICSDA** When SSP is enabled VGP2 is the SSP Data pin.
VID[7:0] VGP[12:5]	IS IS / O	8	**Video Input Data** This is interleaved Y/U/V input data from an external video source. On reset, these pins are tri-stated, and the input buffers of these pins are all disabled. **Video General Purpose Input Output [12:5]** These pins can be used as general-purpose input/output.
VHSYNC VGP14	IS / O	8	**Video Input Horizontal Sync** This signal indicates horizontal sync for incoming video data that can optionally be used as a reference to indicate start of active pixel in video input line. This signal can be programmed as either input or output. On reset, this pin is tri-stated, and its input buffer is disabled. **Video General Purpose Input Output 14** This pin can be used as general-purpose input/output.
VVSYNC VGP15	IS / O	8	**Video Input Vertical Sync** This signal indicates vertical sync for incoming video data that can optionally be used as a reference to indicate start of active line in video input frame. This signal can be programmed as either input or output. On reset, this pin is tri-stated, and its input buffer is disabled. **Video General Purpose Input Output 15** This pin can be used as general-purpose input/output.
VGP[4:3]	IS/O	4	**Video General Purpose Input/Output [4:3]** These pins are used as general-purpose input/output. Upon reset, these pins are tri-stated and their inputs are disabled.

2.6 Flat Panel Interface Pins

Table 2.8 lists and provides a brief description of the FPI signals. The FPI pins are referenced to FVDD. In addition to the FGPx pins, each of these pins can be optionally programmed as GPOs.

Table 2.8: FPI Pins

Pin Name	Type	Drive (mA)	Description
ENCTL	O	8	**Enable Data/Control** In panel power-up sequence, this signal is asserted after ENVDD while in panel power-down sequence, this signal is de-asserted after ENVEE. After reset, this pin is de-asserted.
ENVDD	O	8	**Enable VDD** In panel power-up sequence, this signal is asserted first, while in panel power-down sequence, this signal is de-asserted last. After reset, this pin is de-asserted.
ENVEE	O	8	**Enable VEE** In panel power-up sequence, this signal is asserted last, while in panel power-down sequence, this signal is de-asserted first. After reset, this pin is de-asserted.
FD[17:0]	O	8	**Flat Panel Data (Programmable Polarity)** These signals provide data to the flat panel. These signals are de-asserted during reset and when the flat panel is disabled, regardless of its polarity.
FDE FSCLK2	O	8	**Flat Panel Display Enable** This signal qualifies the display data area (active area). The polarity is register programmable. **Flat Panel Shift Clock 2** For some panels, this pin is used to output either inverted shift clock or delayed shift clock. This signal is de-asserted during reset and when the flat panel is disabled, regardless of its polarity.
FFCLK	O	8	**Flat Panel Frame Clock** This signal is a programmable clock pulse that continuously runs at the frame frequency. This signal is de-asserted during reset and when the flat panel is disabled, regardless of its polarity
FHSYNC	O	8	**Flat Panel Horizontal Sync (Programmable Polarity)** Horizontal sync or Line Pulse (LP) signal for some panels. This signal is de-asserted during reset and when the flat panel is disabled, regardless of its polarity.
FLCLK[1:0]	O	8	**Flat Panel Line Clock [1:0]** These clock pulses occur once per line with a programmable duty cycle and can be used as a clock for the gate (row) driver. This signal is de-asserted during reset and when the flat panel is disabled, regardless of its polarity.
FMOD[1:0]	O	8	**Flat Panel Modulation Clock [1:0] (Programmable Polarity)** This signal can be driven to toggle every frame or every programmable number of lines. This signal is de-asserted during reset and when the flat panel is disabled, regardless of its polarity.
FSCLK	O	12	**Flat Panel Shift Clock** For active high FSCLK, the rising edge of this clock is used to output flat panel data and control signals; thus, the falling edge of this clock is normally used to externally latch flat panel data and control signals. For active low FSCLK, the falling edge of this clock is used to output flat panel data and control signals; thus, the rising edge of this clock is normally used to externally latch flat panel data and control signals. This signal is de-asserted during reset and when the flat panel is disabled, regardless of its polarity.

Table 2.8: FPI Pins (Cont.)

Pin Name	Type	Drive (mA)	Description
FVSYNC	O	8	**Flat Panel Vertical Sync (Programmable Polarity) or First Line Marker (FLM) signal.** This signal is de-asserted during reset and when the flat panel is disabled, regardless of its polarity.
FGP0 PWM0	O	8	**Flat Panel General Purpose Output 0.** This is a general purpose output pin. On reset, this pin is de-asserted. **PWM 0 Output.**
FGP1 PWM1 GS1	O	8	**Flat Panel General Purpose Output 1.** This is a general purpose output pin. On reset, this pin is de-asserted. **PWM 1 Output.** **GS1 signal for ULC TFT.**
FGP2 GS2	O	8	**Flat Panel General Purpose Output 2.** This is a general purpose output pin. On reset, this pin is de-asserted. **GS2 signal for ULC TFT.**
FGP3 CSBO	O	8	**Flat Panel General Purpose Output 3.** This is a general purpose output pin. On reset, this pin is de-asserted. **Serial Output Chip Select.**
FGP4 SDAO	O	8	**Flat Panel General Purpose Output 4.** This is a general purpose output pin. On reset, this pin is de-asserted. **Serial Data Output.**
FGP5 SCLO	O	8	**Flat Panel General Purpose Output 5.** This is a general purpose output pin. On reset, this pin is de-asserted. **Serial Clock Output.**
FGP6 FDI FLCLK2 GCS1	O	8	**Flat Panel General Purpose Output 6.** This is a general purpose output pin. On reset, this pin is de-asserted. **Flat Panel Data Inversion** **Flat Panel Line Clock 2** **GCS1 signal for ULC TFT**
FGP7 FPWMCLK GCS2	O	8	**Flat Panel General Purpose Output 7.** This is a general purpose output pin. On reset, this pin is de-asserted. **Flat Panel PWM clock.** **GCS2 signal for ULC TFT**
FGP8 FDI ALW	O	8	**Flat Panel General Purpose Output 8.** This is a general purpose output pin. On reset, this pin is de-asserted. **Flat Panel Data Inversion.** **ALW signal for ULC TFT**
FGP9 FPWMCLK ECK	O	8	**General Purpose Output 9.** This is a general purpose output pin. On reset, this pin is de-asserted. **Flat Panel PWM clock.** **ECK signal for ULC TFT**
FGP10 CV4	O	8	**General Purpose Output 10.** This is a general purpose output pin. On reset, this pin is de-asserted. **CV4 signal for ULC TFT**
FGP11 PSK	O	8	**General Purpose Output 11.** This is a general purpose output pin. On reset, this pin is de-asserted. **PSK signal for ULC TFT.**
FGP12	IS/O	8	**General Purpose Input/Output 12.** This is a general purpose input/output pin. On reset, this pin is floated.
FGP13 FGP14	O I/O	8	**General Purpose Input/Output 13.** This is a general purpose output pin. On reset, this pin is de-asserted. **General Purpose Input/Output 14.** This is a general purpose input/output pin. On reset, this pin is de-asserted.

2.7 Clock Pins

Table 2.9: Clock Pins

Pin Name	Pin Type	Drive (mA)	Pin Description
OSCFI	AI	-	**Crystal Oscillator Input** This pin is connected to an external crystal in the range of 2 to 13 MHz.
OSCFO	AI / O	-	**Crystal Oscillator Output** This pin is connected to an external crystal in the range of 2 to 13 MHz. When the oscillator is bypassed, this input can be driven by an external source; it is used as input for crystal oscillator by-pass mode. When this is the case, the external clock source can be in range of 2 MHz to 50 MHz.
OSCR	A	-	**Relaxation Oscillator Resistor** This pin is connected to an external 200 kΩ connected to AVDDO. This resistor is needed by all internal clocks; relaxation oscillator, crystal oscillator, clock multiplier.

Note: When using an external crystal (at pin OSCFI), use pin OSCFO as the output for the internal crystal oscillator. When using an external oscillator, use pin OSCFO as input and leave pin OSCFI floating (not connected.)

Note: When using an external clock input through OSCFO, the amplitude of the signal should be between the amplitude of CVDD and BVDD.

2.8 JTAG Interface Pins

JTAG pins are used for interfacing with the GoForce 4000 for diagnostic and testing purposes. Table 2.10 lists the five GoForce 4000 JTAG interface pins. The JTAG interface pins are referenced to SDVDD.

Refer to Design Guide *DG-01098-001* for information on utilizing the JTAG interface pins for boundary testing.

Table 2.10: Description of the JTAG Interface Pins

Pin Name	Type	Drive (mA)	Description
TCK	I	4	**JTAG Clock**
TDI	I	4	**JTAG Data Input**
TDO	O	4	**JTAG Data Output**
TMS	I	4	**JTAG Mode Select**
TRST	I	4	**JTAG Reset**

2.9 Secure Digital (SD) Interface Pins

Table 2.11 lists and briefly describes the GoForce 4000 SD/GPIO[65:60] pins. The SD Interface pins are referenced to SDVDD.

Table 2.11: Description of the Secure Digital (SD) / GPIO[65:60] Pins

Pin Name	Type	Drive (mA)	Description
SDD3 GPIO[63]	IS/O	4	**Card Detect/Data Line 3 (DAT3/CD)** On power up, the host uses this pin for card detection. Later this pin will be used as DATA line 3 in wide-bus mode. **General Purpose Input/Output**
SDCMD GPIO[65]	IS/O	4	**Secure Digital Command** This pin is used to send commands to the SD card and responses to the SD Host. **General Purpose Input/Output**
SDCLK GPIO[64]	IS/O	4	**Secure Digital Clock** The host provides the clock to the SD card through this pin. The maximum frequency on this pin is 25MHz **General Purpose Input/Output**
SDD0 GPIO[60]	IS/O	4	**Data Line 0 (DAT0)** This pin is used as the data line in both single pin and wide-bus data transfer modes. **General Purpose Input/Output**
SDD1 GPIO[61]	IS/O	4	**Data Line 1(DAT1)** This pin is used as the data line 1 in wide-bus data transfer mode. **General Purpose Input/Output**
SDD2 GPIO[62]	IS/O	4	**Data Line 2 (DAT2)** This pin is used as the data line 2 in wide-bus data transfer mode. **General Purpose Input/Output**
SDGP0	IS/O	4	**SD GPIO0** General Purpose Input/Output. It is typically used for SD card detection.
SDGP1	IS/O	4	**SD GPIO1** General Purpose Input/Output. It is typically used for SD write protection.

2.10 Miscellaneous Pins

Table 2.12: Miscellaneous Pins

Pin Name	Pin Type	Drive (mA)	Pin Description
AUDIOCLK	IS / O	8	**MPEG-4 Encoder Time stamp generation clock input** Input for a clock signal source to synchronize audio and video timing to minimize the drifting of audio time versus video time in MPEG encoding.
BGP0			**General-Purpose Bus Input / Output Bit [0]** After reset, this pin may be configured as a general-purpose output to allow the internal clocks to be routed to the outside of the GoForce 4000 for testing purposes.
MD[2:0]	IS	8	**Mode Select Bits [2:0]** These pins are configured as input pins during/following power-on reset. The state of these pins is latched with a transparent latch at the trailing edge of the power-on reset pulse, in order to decide the mode of operation. Normally, high impedance pull-down or pull-up resistors are attached to these pins for mode setting. **MD2 MD1 MD0** Chip configuration 0 0 0 Fixed cycle host mode (no wait control) 0 0 1 Reserved 0 1 0 Active low ready handshake mode 0 1 1 Active low wait handshake mode 1 0 0 Indirect fixed cycle addressing mode (no wait control) 1 0 1 Reserved 1 1 0 Indirect Active low Ready Handshake 1 1 1 Indirect Active low Wait Handshake mode
BGP[3:1]	IS/O	8	**General Purpose Bus I/O Bits** After reset, these pins can be configured as general-purpose input/output pins. These pins are powered by BVDD.
PORn	IS	-	**Power-On Reset (Active Low)** This signal resets the GoForce 4000. It also puts the GoForce 4000 in low power state, where all modules are disabled except for some registers.

Chapter 3 Specifications

3.1 Absolute Maximum Ratings

Table 3.1 specifies the absolute maximum ratings allowed for the GoForce 4000.

Table 3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
VDD_{CORE}	Supply voltage for the internal core and memory (CVDD)	–0.3	2.0	V
VDD_{IO}	Supply voltage for all other I/O pins (BVDD, FVDD, VVDD, SDVDD)	–0.3	4.0	V
V_{IN}	DC voltage on input or 3-state pins	–0.5	VDD_{IO}[1] + 0.5	V
T_{STG}	Storage temperature	–55	125	°C
T_{SOL}	Peak packaged device soldering temperature: SnPb Eutectic Solder Pb-free solder	 - -	 240 (+0/-5) 250 (+0/-5)	 °C °C

1. Voltage level at the respective I/O supply pins.

Note: Permanent device damage may occur if the specifications for the Absolute Maximum Ratings are exceeded. All voltages are defined with respect to ground.

3.2 Normal Operating Conditions

Operation of the GoForce 4000 device must be restricted to normal operating conditions specified in Table 3.2.

Table 3.2 Normal Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VDD_{CORE}	Supply voltage for the internal core (CVDD)	1.425	1.5	1.65	V
VDD_{IO}	Supply voltage for all other I/O pins (BVDD, FVDD, VVDD, SDVDD)	1.71	3.0	3.6	V
T_A	Free-air operating ambient temperature	–30	-	85	°C

3.3 DC Characteristics

The following subsections provide information on the DC characteristics of the GoForce 4000.

3.3.1 I/O Pin DC Specifications

Table 3.3 provides the I/O pin DC specifications of the GoForce 4000.

Table 3.3 DC Characteristics

Symbol	Parameter	Notes	Minimum	Maximum	Unit
I_{DD}	Quiescent supply current	_	_	TBD	µA
I_{IH}	Input high leakage current at typical conditions	Input-only pins	_	1.0	µA
		Bidirectional pins	_	1.0	µA
I_{IL}	Input low leakage current at typical conditions	Input-only pins	_	1.0	µA
		Bidirectional pins	_	1.0	µA
I_{OZH}	Output high impedance leakage current at typical conditions	All I/O pins	_	-5.0	µA
I_{OZL}	Output low impedance leakage current at typical conditions	All I/O pins	_	5.0	µA
V_{IH}	Input high voltage	All inputs	0.8 x VDD_{CORE}	VDD_{IO}	V
V_{IL}	Input low voltage	All inputs	GND	0.2 x VDD_{IO}	V
V_{OL} (@ 4 mA load)	Output low voltage	All outputs	GND	0.15 x VDD_{IO}	V
V_{OH}	Output high voltage	All outputs	0.8 x VDD_{IO} (See Note)	VDD_{IO}	V

Note: Note: VDD_{IO} is the respective power supply voltage.
2.35 V < VDD_{IO} < 3.60 V @ 4 mA load OR
1.7 V < VDD_{IO} < 2.35 V @ 3 mA load.

3.3.2 I/O Pin Load Capacitance

Table 3.4 provides the I/O pin load capacitance of the GoForce 4000.

Table 3.4 Pin Load Capacitance

Symbol	Parameter	Maximum	Unit
C_{BID}	Bidirectional buffer capacitance	4	pF
C_{IN}	Input capacitance	4	pF
C_{OUT}	Output capacitance	4	pF

3.4 AC Characteristics

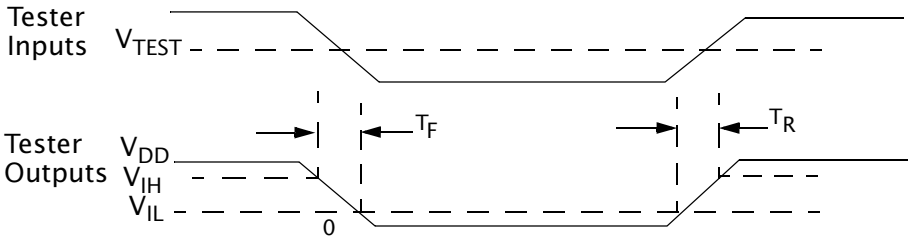
This section describes the GoForce 4000 AC characteristics, which consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. Table 3.5 lists the conditions used for testing the GoForce 4000 AC timing. Tests are performed under the conditions specified in Table 3.5.

Table 3.5 AC Test Conditions

Symbol	Parameter	Value	Unit
T_F	Input fall time	2	ns
T_R	Input rise time	3	ns
V_{IH}	Input high voltage	0.8 x VDD	V
V_{IL}	Input low voltage	0.2 x VDD	V
V_{TEST}	Output trip point	0.5 x VDD	V

Figure 3.1 illustrates the AC test timing.

Figure 3.1 AC Test Timing



3.4.1 Clock

Figure 3.2 shows the reference clock timing.

Figure 3.2 Reference Clock Timing

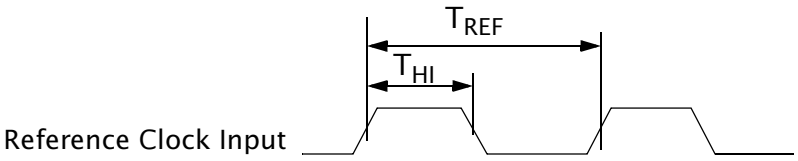


Table 3.6 and Table 3.7 provide the AC timing characteristic values of the crystal oscillator input clock (OSCFI) and the external oscillator input clock (OSCFO). The values are created by altering the crystal's oscillation signal. The test circuit consists of a 1 MΩ resistor in parallel with the 2 - 6 MHz crystal and two capacitors (C1 = C2) to ground, which are connected to each side of the crystal/resistor configuration. (C1 = C2 = 2 x C_{load}Crystal)

Table 3.6 AC Timing Characteristics - Crystal Input Clock (OSCFI)

Symbol	Parameter	Min	Max	Units
T_{REF}	Crystal input frequency	2	13	MHz
T_{HI}/T_{REF}	Clock duty cycle	40	60	%

Table 3.7 AC Timing Characteristics - External Oscillator Clock Input (OSCFO)

Symbol	Parameter	Min	Max	Units
T_{REF}	External oscillator clock frequency	2	50	MHz
T_{HI}/T_{REF}	Clock duty cycle (BVDD)	40	60	%
	Clock duty cycle (3.3 V)	30	70	%

Note: When using an external oscillator, the input voltage should be 1.5 V. If the input voltage is 3.3 V, the oscillator will function correctly but the duty cycle will vary between 30% and 70%, rather than 40% to 60%.

3.4.2 Reset

Figure 3.3 Reset Timing

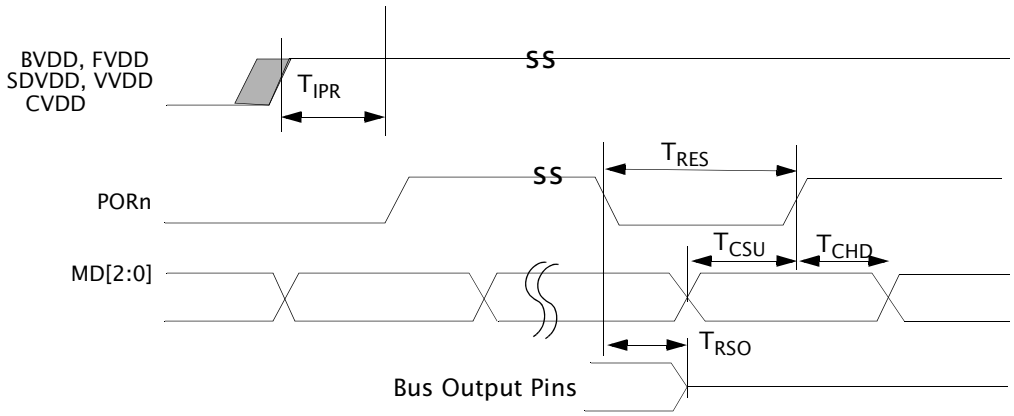


Table 3.8 AC Timing Characteristics - Reset

Symbol	Parameter	Min	Max	Units
T_{IPR}	Reset inactive from power stable[1]	1	–	ms
T_{RES}	Minimum reset pulse width	100	–	µs
T_{RSO}	Reset active to output float delay	–	40	ns
T_{CSU}	Configuration setup time[2]	20	–	ns
T_{CHD}	Configuration hold time	5	–	ns

1. This parameter includes time for internal voltage stabilization of all sections of the chip, start-up and stabilization of the internal clock, and setting of all internal logic to a known state.
2. This parameter specifies the absolute minimum setup time to reliably latch the state of the mode select bits. The recommended configuration bit setup time is T_{RES} to ensure that the chip is in a completely stable state when Reset goes inactive.

3.4.3 Power Sequencing

Note that the power sequencing for GoForce 4000 Rev A and GoForce 4000 Rev B are different. Each is detailed separately below.

3.4.3.1 GoForce 4000 Rev A Power Sequencing

Figure 3.4 GoForce 4000 Rev A Power Sequencing

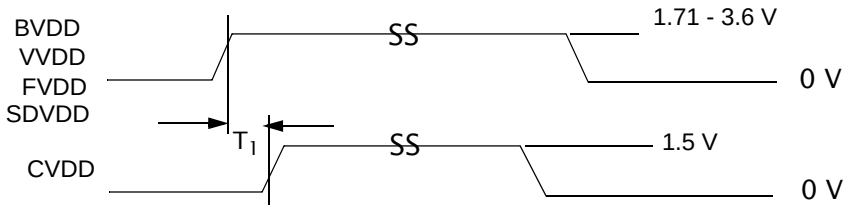


Table 3.9 GoForce 4000 Rev A Power Sequencing

Symbol	Parameter	Min	Max	Units
T_1	I/O supply voltage applied to core supply voltage applied delay	1	-	ms

These specifications are recommendations and damage should not occur even if core supply is applied first for a brief period of time (< 1 ms). These conditions have not been tested since they are not expected to cause damage.

3.4.3.2 GoForce 4000 Rev B Power Sequencing

The power on and power-down sequences for the GoForce 4000 are given in Figure 3.5 and Figure 3.6, and reference the following voltage levels:

- CVDD maximum: 1.5 V
- VVDD, BVDD, FVDD, and SDVDD maximum: ranging from 1.71 to 3.6 V

Minimum: 0 V

Figure 3.5: GoForce 4000 Rev B Power Supply Sequence

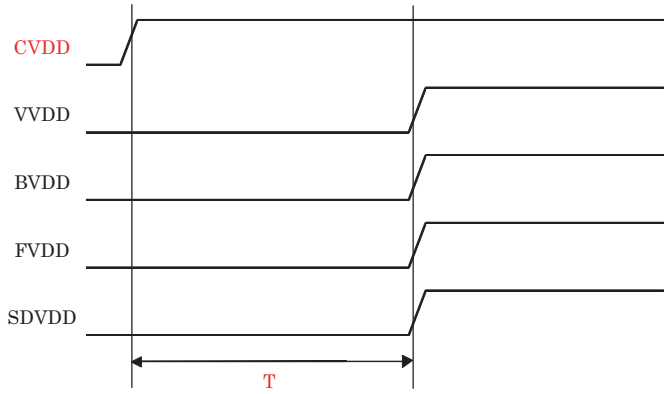


Figure 3.6: GoForce 4000 Rev B Power-off Sequence

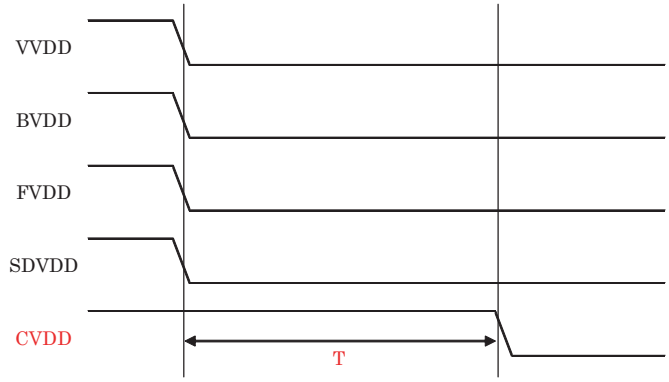
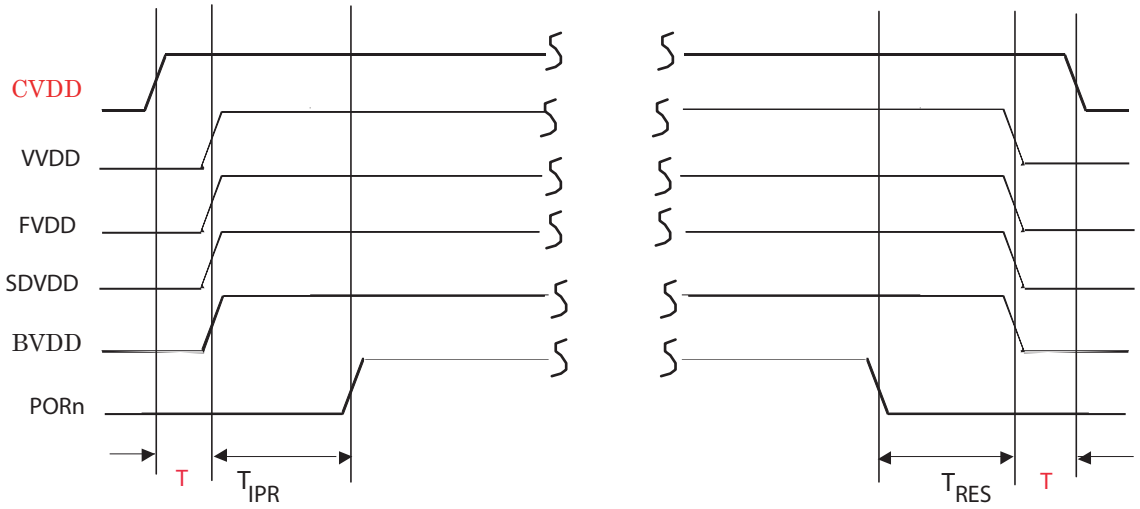


Table 3.10 GoForce 4000 Rev B Power Sequencing Timing

Symbol	Parameter	Min
T (T= T_{VVDD}, T_{BVDD}, T_{FVDD}, *or* T_{SDVDD})	T = Delay between application of Core Supply Voltage (CVDD) and I/O Supply Voltage (BVDD/VVDD/SDVDD/FVDD). T is the time between reaching 90% of the CVDD and power rail and 10% of the IO power rail.	1 ms

Note: T_{SDVDD}, T_{FVDD}, T_{VVDD}, and T_{BVDD} do not have to be equal to each other as long as they fall within the specification for T.

Figure 3.7: GoForce 4000 Rev B PORn Power On and Off Sequence with BVDD



Note: As shown in Figure 3.7, PORn (Power on Reset) must stay low until a time equal to T_{IPR} after all the power supplies have reached their normal operating voltage. Figure 3.7 implies no sequence requirements for VVDD, FVDD, SDVDD, or BVDD with respect to CVDD or each other.

If the regulators supplying the core and I/O power rails are sequenced when powering down, VVDD, FVDD, SDVDD, and BVDD must be turned off before the CVDD power is turned off.

The parameter T is already defined in Table 3.10.

Table 3.11 PORn Timing Parameters

Symbol	Parameter	Min	Max
T_{IPR}	Reset inactive from power stable	1 ms	---
T_{RES}	Reset to power off	100 µs	---

Note: T_{IPR} includes time for the internal voltage stabilization of all sections of the chip, start-up and stabilization of the internal clock, and setting of all internal logic to a known state.

3.4.4 Host Interface

Type A, Type B, and Type C Host interfaces each have a set of timing parameters and diagrams, detailed in the following three sections. In Table 3.10 all of the timing diagrams are listed and grouped according to Host Interface type. To go to a specific timing diagram, find the title under the appropriate host Interface type, go to the page number listed in the adjacent column (under Page), and click on the page number. It should take you directly to the chosen timing diagram.

Table 3.12 Type A, B, and C Host Interface Timing Diagrams List

Direct Addressing				Indirect Addressing	
8/16bit Host Bus Interface	**Page**	**32bit Host Bus Interface**	**Page**	**8/16bit Host Bus Interface**	**Page**
Type A Host Interface					
WRn-Controlled Write	3-10	WRn-Controlled Write	3-11	Register Write	3-20
CSn-controlled Write	3-12	CSn-controlled Write	3-13	Register Read	3-21
RDn-controlled Read	3-14	RDn-controlled Read	3-15	Memory Write	3-22
CSn-controlled Read	3-16	CSn-controlled Read	3-17	Memory Read	3-23
Page-Mode Read	3-18	Page-Mode Read	3-19	Register Burst Read	3-24
Register/Memory Burst Write	3-28	Register/Memory Burst Write	3-29	Memory Burst Read	3-25
Register/Memory Burst Read	3-30	Register/Memory Burst Read	3-31	Register Burst Write	3-26
				Memory Burst Write	3-27
Type B Host Interface					
CS-controlled Write	3-36	CS-controlled Write	3-37	Register Write	3-40
CS-controlled Read	3-38	CS-controlled Read	3-39	Register Read	3-41
Register/Memory Page Read	3-44	Register/Memory Page Read	3-45	Memory Write	3-42
				Memory Read	3-43
Type C Host Interface					
WEn-controlled Write	3-49	WEn-controlled Write	3-50	Register Write	3-59
CSn-controlled Write	3-51	CSn-controlled Write	3-52	Register Read	3-60
OEn-controlled Read	3-53	OEn-controlled Read	3-54	Memory Write	3-61
CSn-controlled Read	3-55	CSn-controlled Read	3-56	Memory Read	3-62
Page Mode Read	3-57	Page Mode Read	3-58	Register Burst Read	3-63
Register/Memory Burst Write	3-67	Register/Memory Burst Write	3-68	Memory Burst Read	3-64
Register/Memory Burst Read	3-69	Register/Memory Burst Read	3-70	Register Burst Write	3-65
				Memory Burst Write	3-66

3.4.4.1 Type A Host Interface

This section shows the timing characteristics for Type A Host Bus interface using both direct addressing and indirect addressing. The interface utilizes either an 8 bit, 16 bit, or 32-bit bus.

- Direct Addressing Read/Write Timing Diagrams
  Figure 3.8 through Figure 3.17
  Figure 3.28 through Figure 3.31

- Indirect Addressing Read/Write Timing Diagrams
  Figure 3.18 through Figure 3.27

All Type A Timing Diagrams refer to timing parameters in Table 3.22.

Note: The WAITn signal used in handshake mode, Burst, and Page writes and reads is tri-stated. Use either a pull-up or a pull-down resistor with this signal, according to the Host CPU specifications.

Note: For an 8bit Type A Host Interface tie BEn0 to ground. If it is already being driven in 8bit mode, tie it to the related host pin.

Table 3.13 Type A Byte-enable Signals for Different Size Host Busses

Type A Host Interface Signal Name	32bit Host Bus		16bit Host Bus		8bit Host Bus	
	Function	Signal	Function	Signal	Function	Signal
BEn0	Byte Enable 1 [7:0]	BEn0	Byte Enable 1 [7:0]	BEn0	Byte Enable 1 [7:0] (Tied low or to a related host pin.)	BEn0
BEn1	Byte Enable 2 [15:8]	BEn1	Byte Enable 2 [15:8]	BEn1	A[0]	A[0]
A1	Byte Enable 3 [23:16]	BEn2	A1	A1	A1	A1
BEn3	Byte Enable 4 [31:24]	BEn3	Not used: Tie low externally	N/A	Not used: Tie low externally	N/A

Figure 3.8: WRn-controlled Write, Type A Host Interface, 8bit and 16bit Direct Addressing

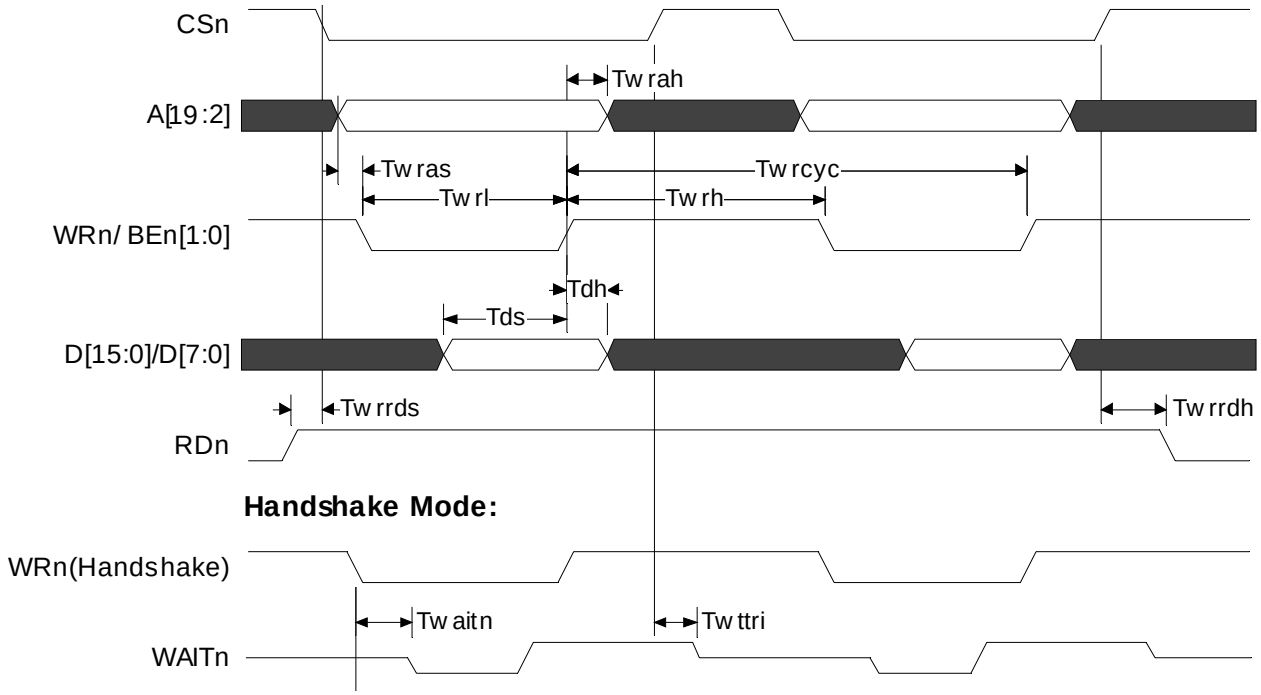


Figure 3.9: WRn-controlled Write, Type A Host Interface, 32bit Direct Addressing

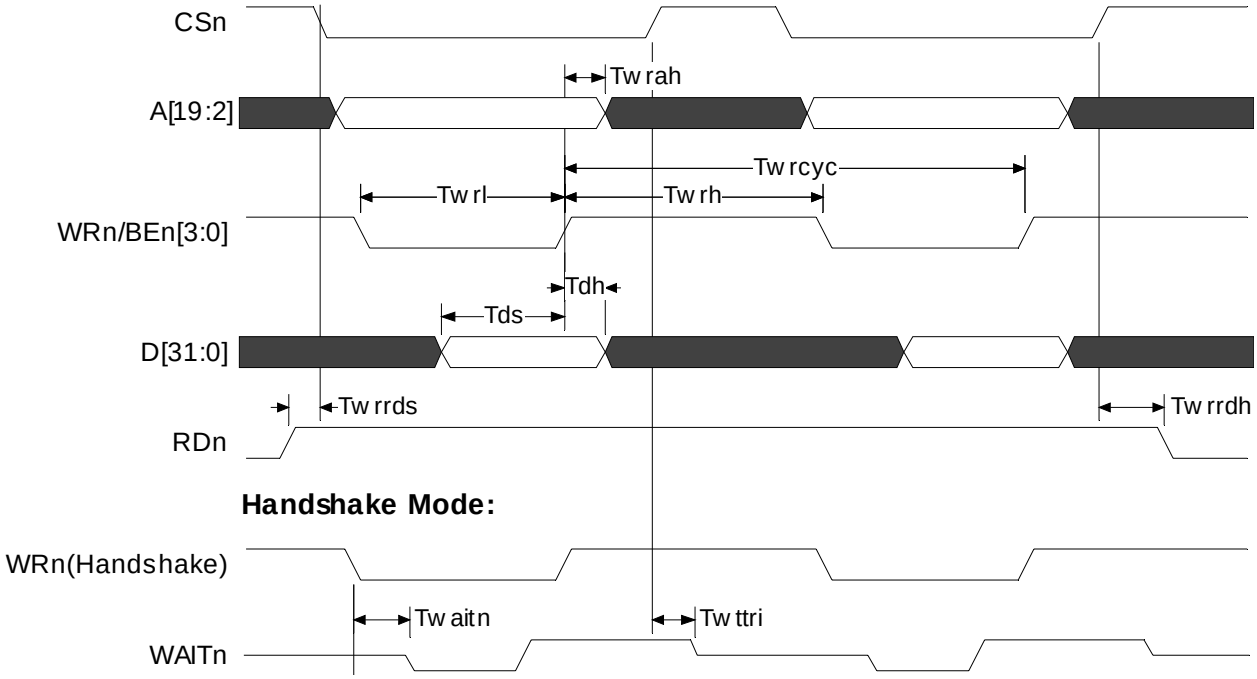


Figure 3.10: CSn-controlled Write, Type A Host Interface, 8bit and 16bit Direct Addressing

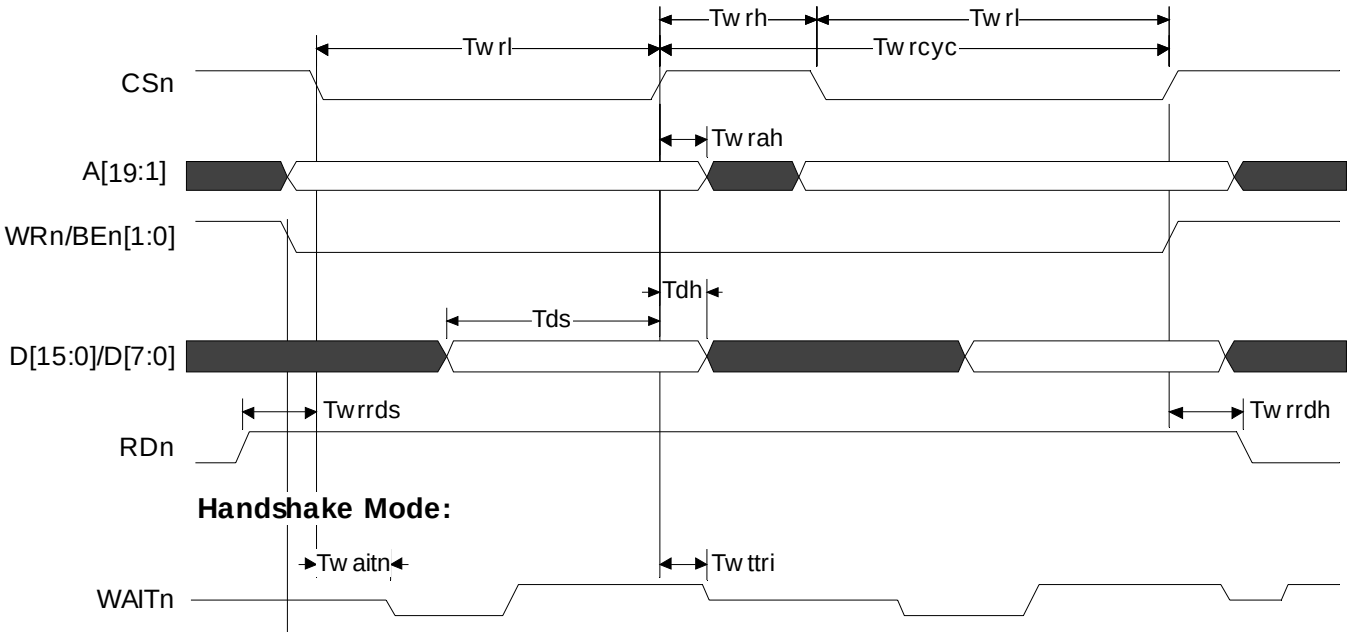


Figure 3.11: CSn-controlled Write, Type A Host Interface, 32bit Direct Addressing

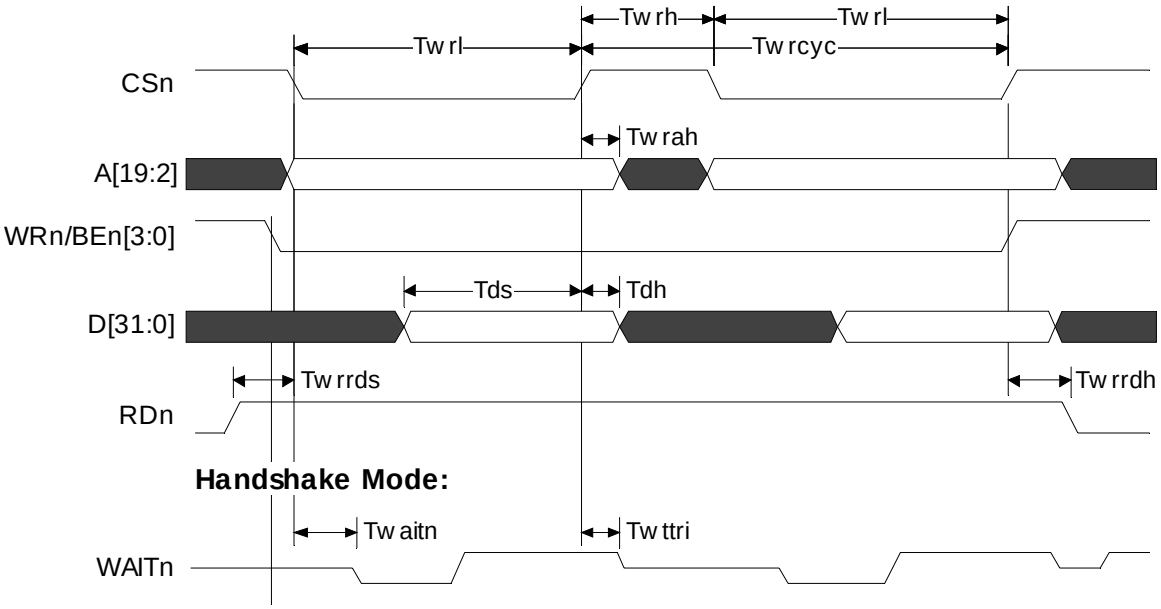


Figure 3.12: RDn-controlled Read, Type A Host Interface, 8bit and 16bit Direct Addressing

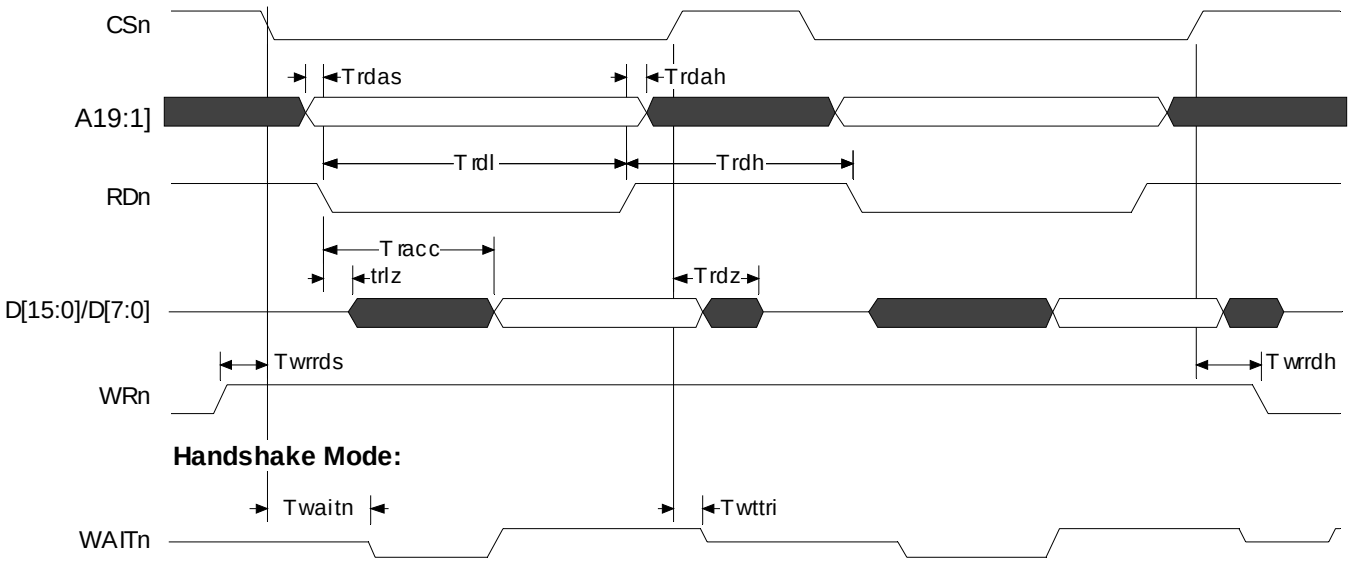


Figure 3.13: RDn-controlled Read, Type A Host Interface, 32bit Direct Addressing

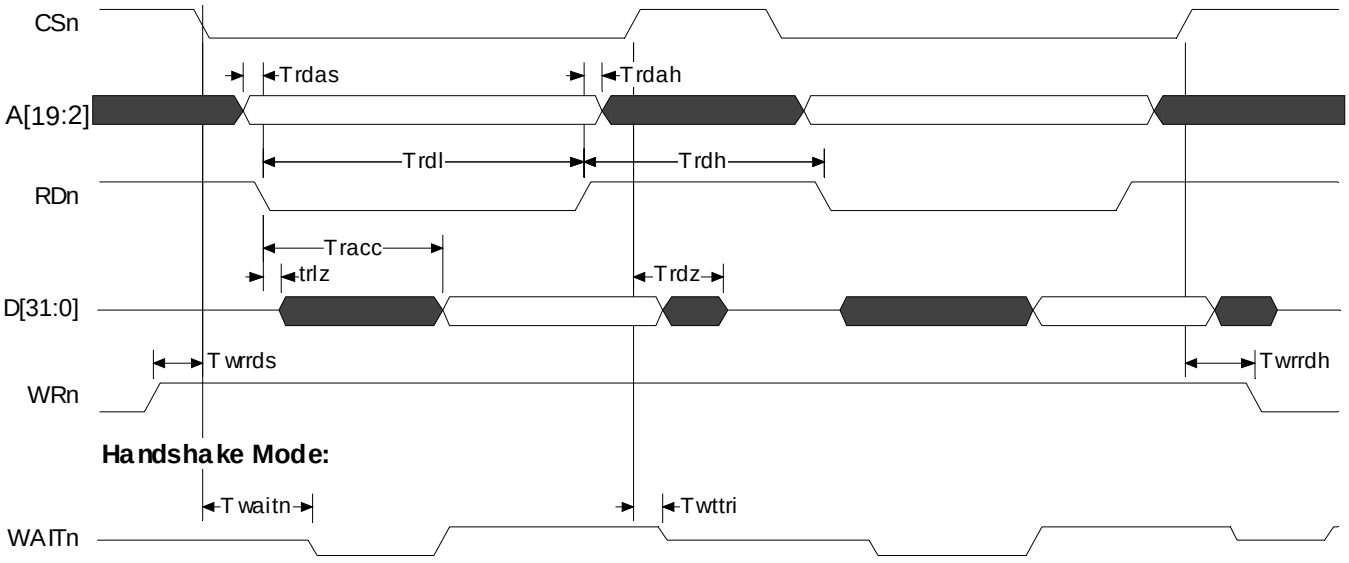


Figure 3.14: CSn-controlled Read, Type A Host Interface, 8bit and 16bit Direct Addressing

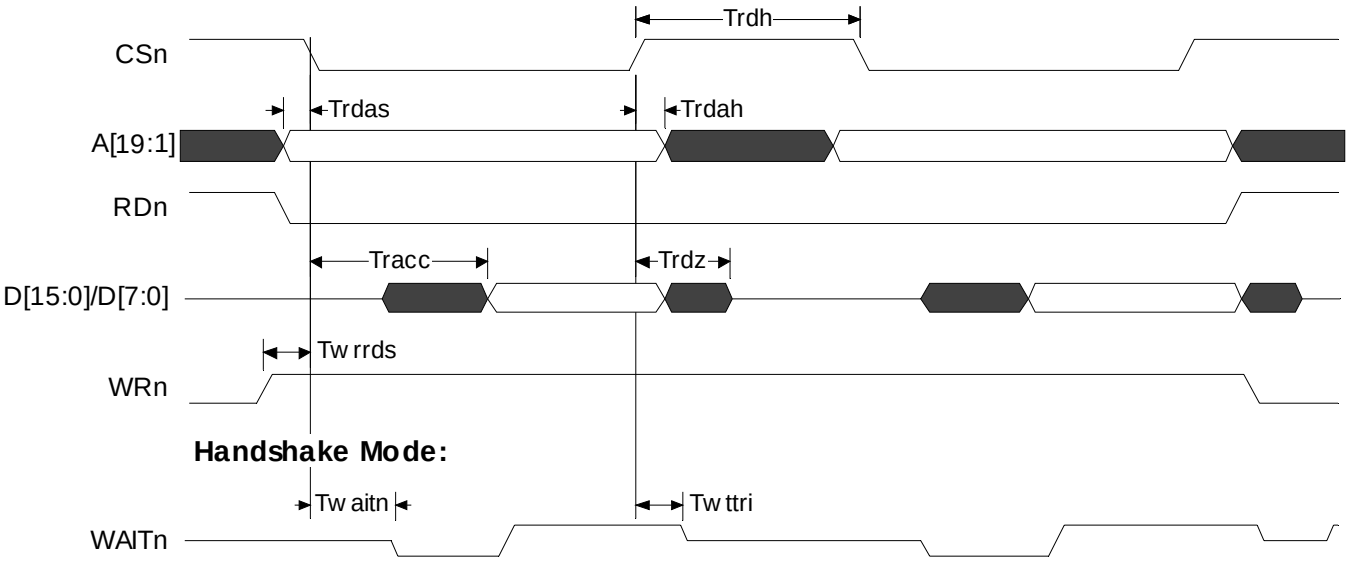


Figure 3.15: CSn-controlled Read, Type A Host Interface, 32bit Direct Addressing

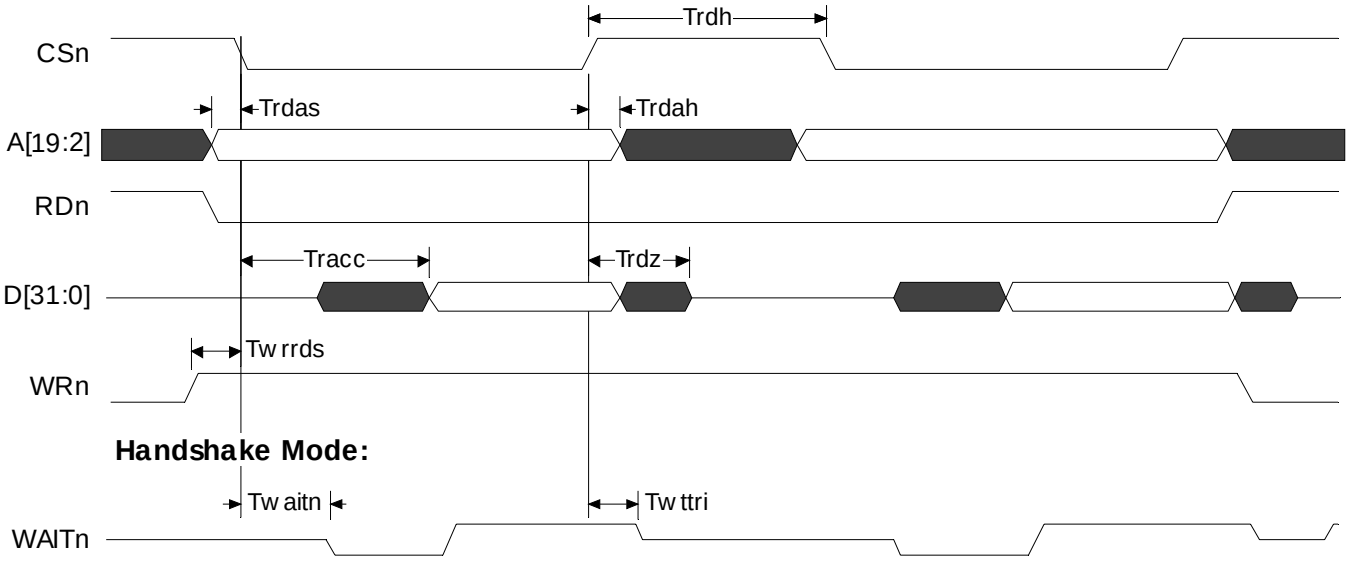
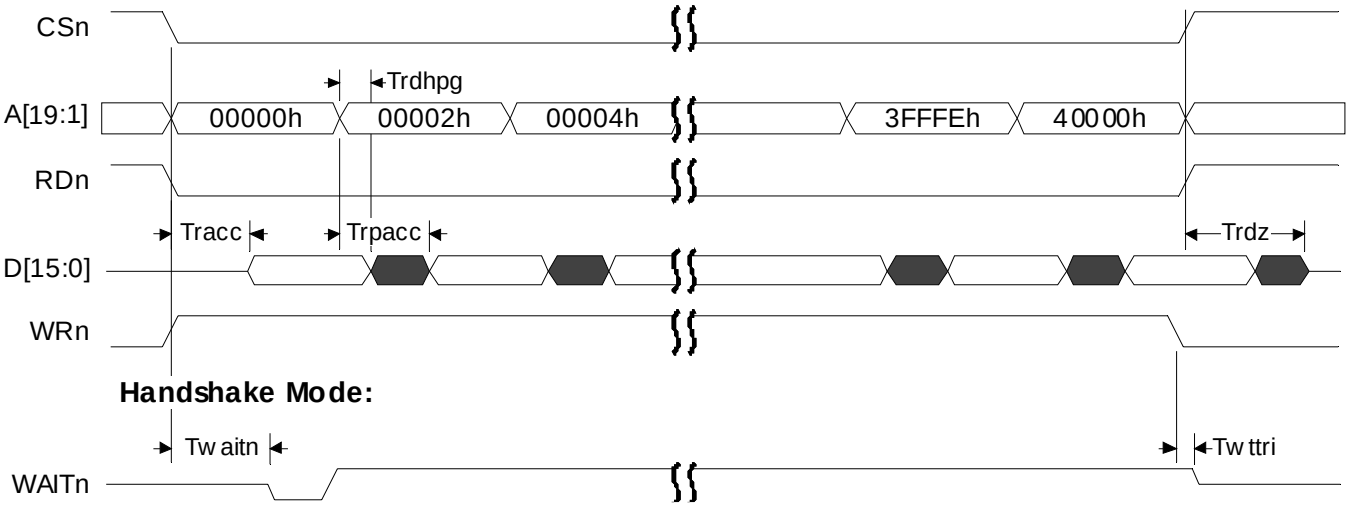
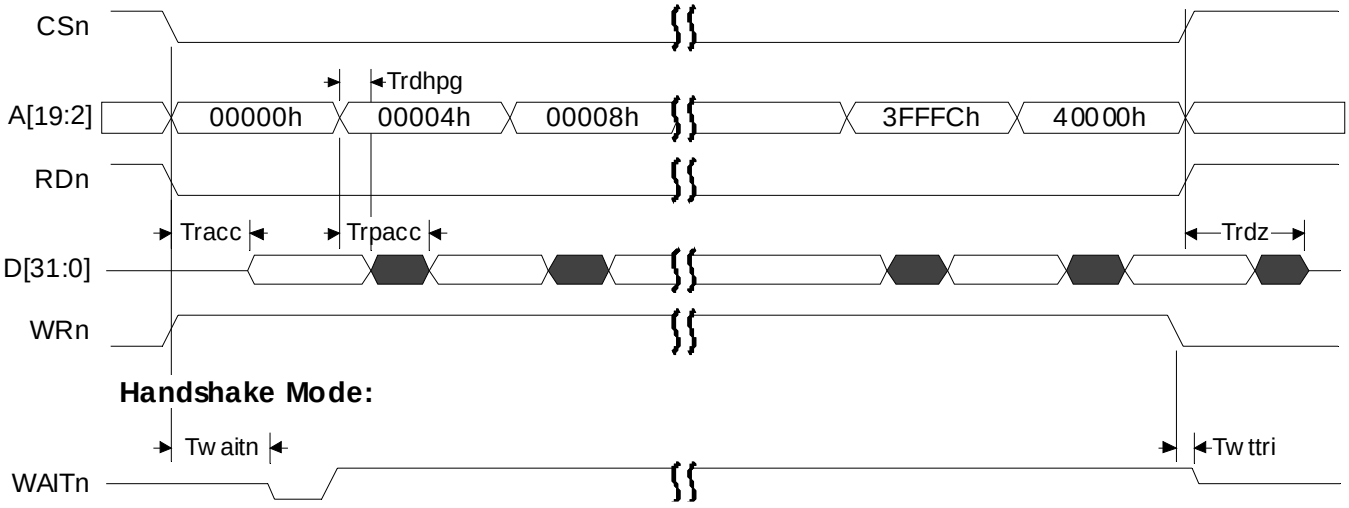


Figure 3.16: Page Mode Read, Type A Host Interface, 8bit and 16bit Direct Addressing



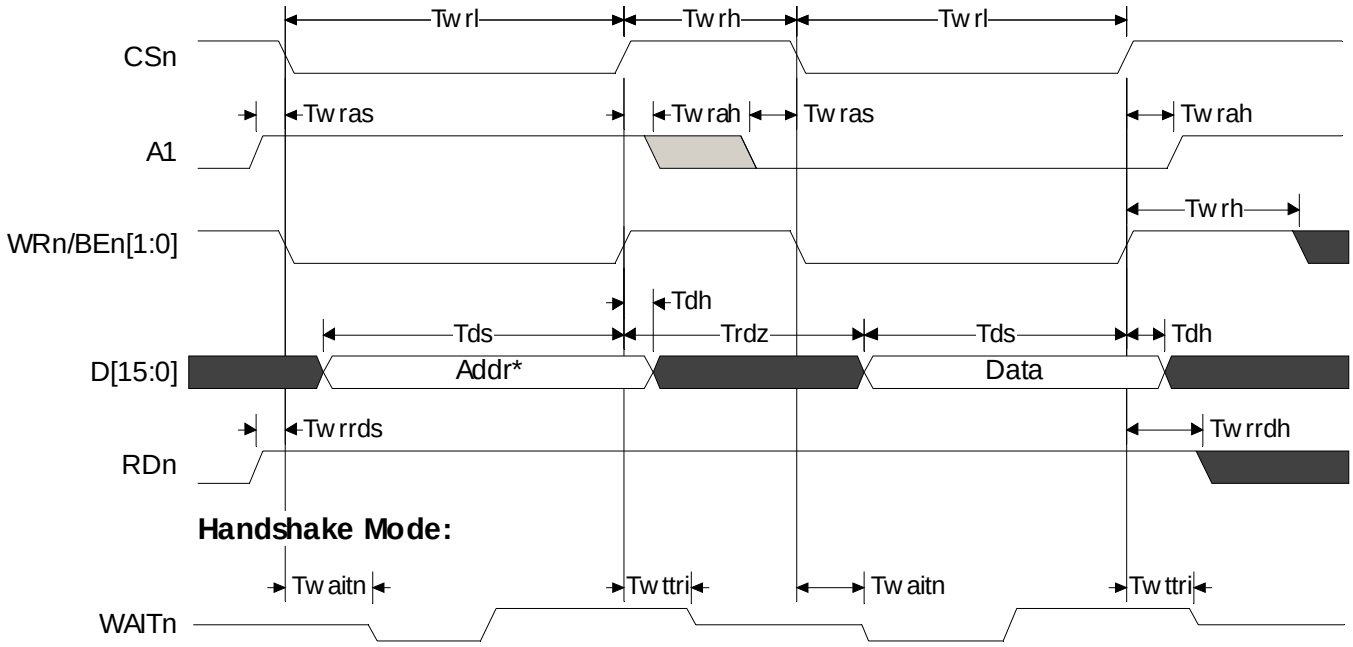
Note: There is no restriction on page length.

Figure 3.17: Page Mode Read, Type A Host Interface, 32bit Direct Addressing



Note: There is no restriction on page length.

Figure 3.18: Register Write, Type A Host Interface, Indirect Addressing

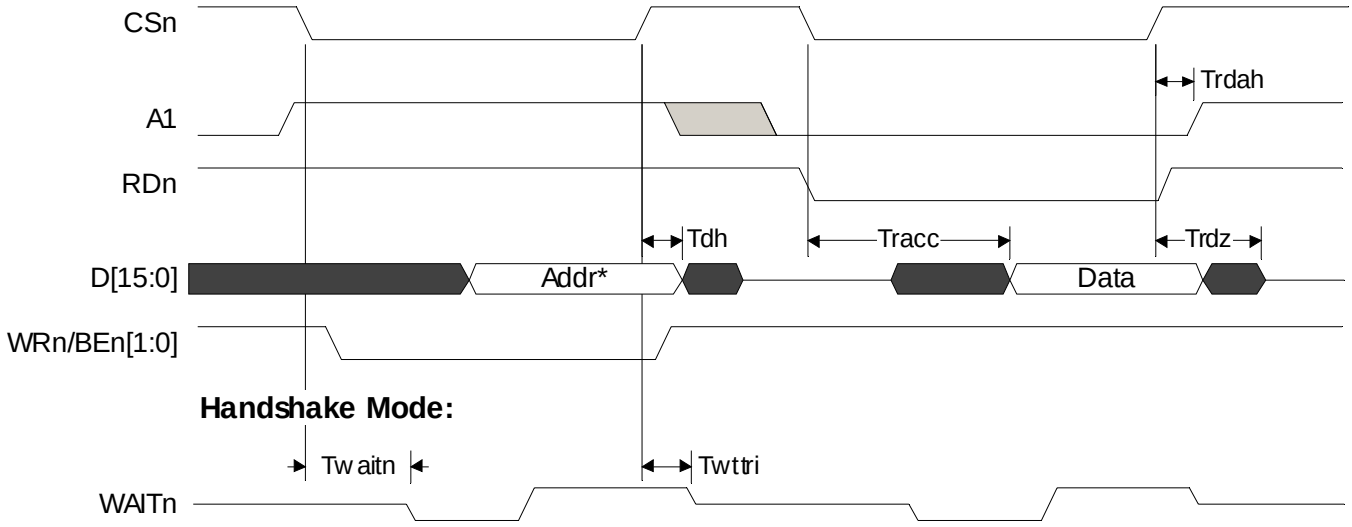


* See the following table for bit mappings.

Table 3.14 Register Write D[15:0] Bit Mapping for Addr* in Figure 3.18

Data Bus	Address Phase			
	16bit Host Bus	8bit Host Bus		
	Addr*	Addr*1	Addr*2	Addr*3
D[15]	x			
D[14]	x			
D[13]	A[12]			
D[12]	A[11]			
D[11]	A[10]			
D[10]	A[9]			
D[9]	A[8]			
D[8]	A[7]			
D[7]	A[6]	A[4]	A[9]	x
D[6]	A[5]	A[3]	A[8]	x
D[5]	A[4]	A[2]	A[7]	A[12]
D[4]	A[3]	A[1]	A[6]	A[11]
D[3]	A[2]	A[0]	A[5]	A[10]
D[2]	A[1]	0	1	0
D[1]	x	0	0	1
D[0]	1	1	1	1

Figure 3.19: Register Read, Type A Host Interface, Indirect Addressing

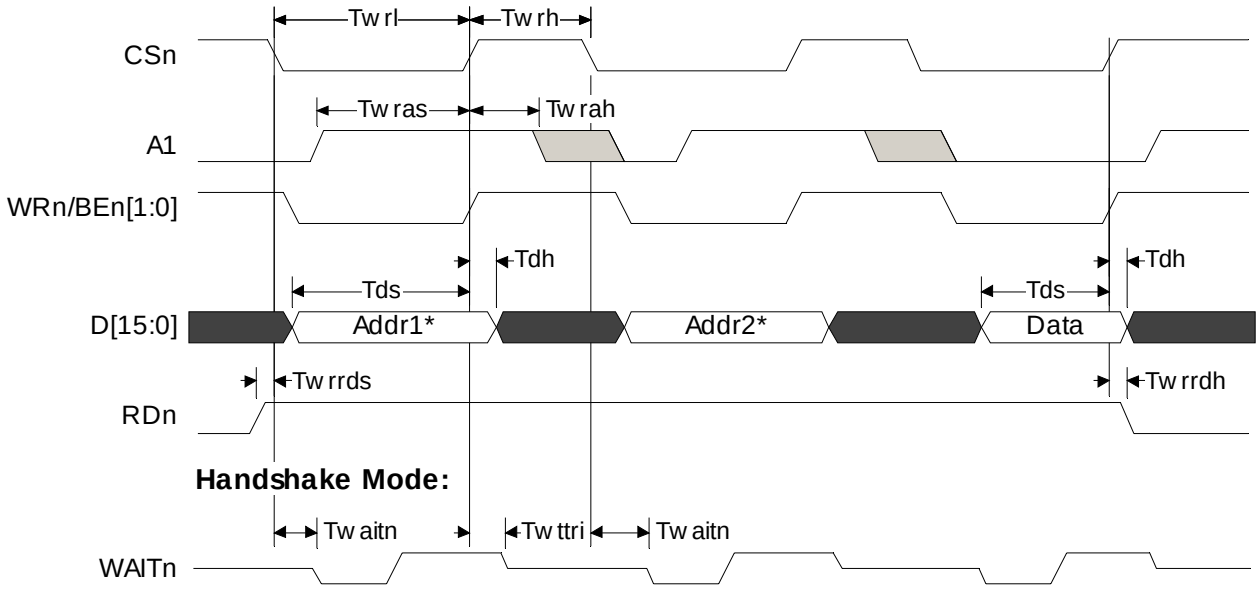


* See the following table for bit mappings.

Table 3.15 Register Read D[15:0] Bit Mapping for Addr* in Figure 3.19

Data Bus	Address Phase			
	16bit Host Bus	8bit Host Bus		
	Addr*	Addr*1	Addr*2	Addr*3
D[15]	x			
D[14]	x			
D[13]	A[12]			
D[12]	A[11]			
D[11]	A[10]			
D[10]	A[9]			
D[9]	A[8]			
D[8]	A[7]			
D[7]	A[6]	A[4]	A[9]	x
D[6]	A[5]	A[3]	A[8]	x
D[5]	A[4]	A[2]	A[7]	A[12]
D[4]	A[3]	A[1]	A[6]	A[11]
D[3]	A[2]	A[0]	A[5]	A[10]
D[2]	A[1]	0	1	0
D[1]	x	0	0	1
D[0]	1	1	1	1

Figure 3.20: Memory Write, Type A Host Interface, Indirect Addressing

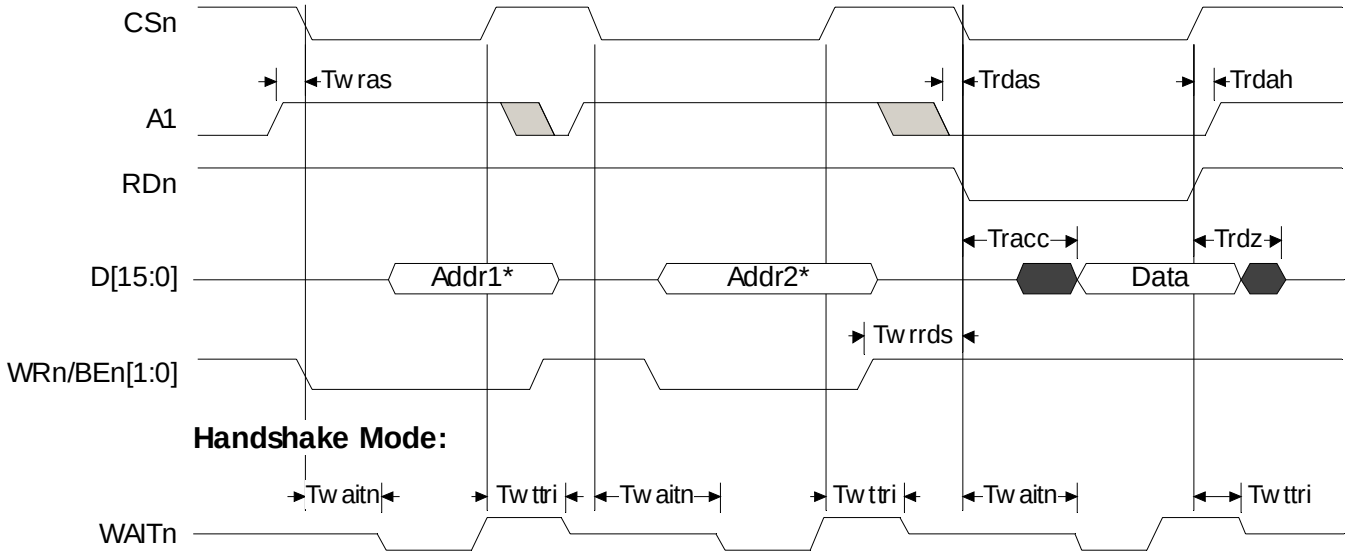


* See the following table for bit mappings.

Table 3.16 Memory Write D[15:0] Bit Mapping for Addr1* and Addr2* in Figure 3.20

Data Bus	Address Phase					
	16bit Host Bus		8bit Host Bus			
	Addr1	Addr2	Addr1	Addr2	Addr3	Addr4
D[15]	A[14]	x				
D[14]	A[13]	x				
D[13]	A[12]	x				
D[12]	A[11]	x				
D[11]	A[10]	x				
D[10]	A[9]	x				
D[9]	A[8]	x				
D[8]	A[7]	x				
D[7]	A[6]	x	A[4]	A[9]	A[14]	A[19]
D[6]	A[5]	A[19]	A[3]	A[8]	A[13]	A[18]
D[5]	A[4]	A[18]	A[2]	A[7]	A[12]	A[17]
D[4]	A[3]	A[17]	A[1]	A[6]	A[11]	A[16]
D[3]	A[2]	A[16]	A[0]	A[5]	A[10]	A[15]
D[2]	A[1]	A[15]	0	1	0	1
D[1]	0	1	0	0	1	1
D[0]	0	0	0	0	0	0

Figure 3.21: Memory Read, Type A Host Interface, Indirect Addressing

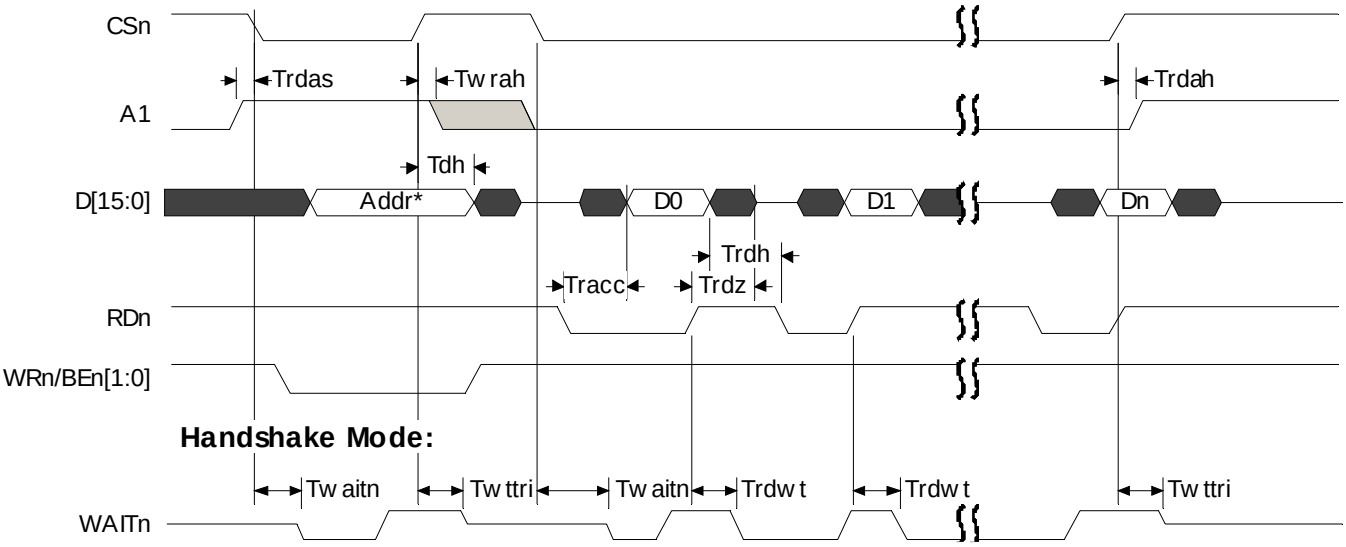


* See the following table for bit mappings.

Table 3.17 Memory Read D[15:0] Bit Mapping for Addr1*and Addr2* in Figure 3.21

Data Bus	Address Phase					
	16bit Host Bus		8bit Host Bus			
	Addr1	Addr2	Addr1	Addr2	Addr3	Addr4
D[15]	A[14]	x				
D[14]	A[13]	x				
D[13]	A[12]	x				
D[12]	A[11]	x				
D[11]	A[10]	x				
D[10]	A[9]	x				
D[9]	A[8]	x				
D[8]	A[7]	x				
D[7]	A[6]	x	A[4]	A[9]	A[14]	A[19]
D[6]	A[5]	A[19]	A[3]	A[8]	A[13]	A[18]
D[5]	A[4]	A[18]	A[2]	A[7]	A[12]	A[17]
D[4]	A[3]	A[17]	A[1]	A[6]	A[11]	A[16]
D[3]	A[2]	A[16]	A[0]	A[5]	A[10]	A[15]
D[2]	A[1]	A[15]	0	1	0	1
D[1]	0	1	0	0	1	1
D[0]	0	0	0	0	0	0

Figure 3.22: Register Burst Read, Type A Host Interface, Indirect Addressing



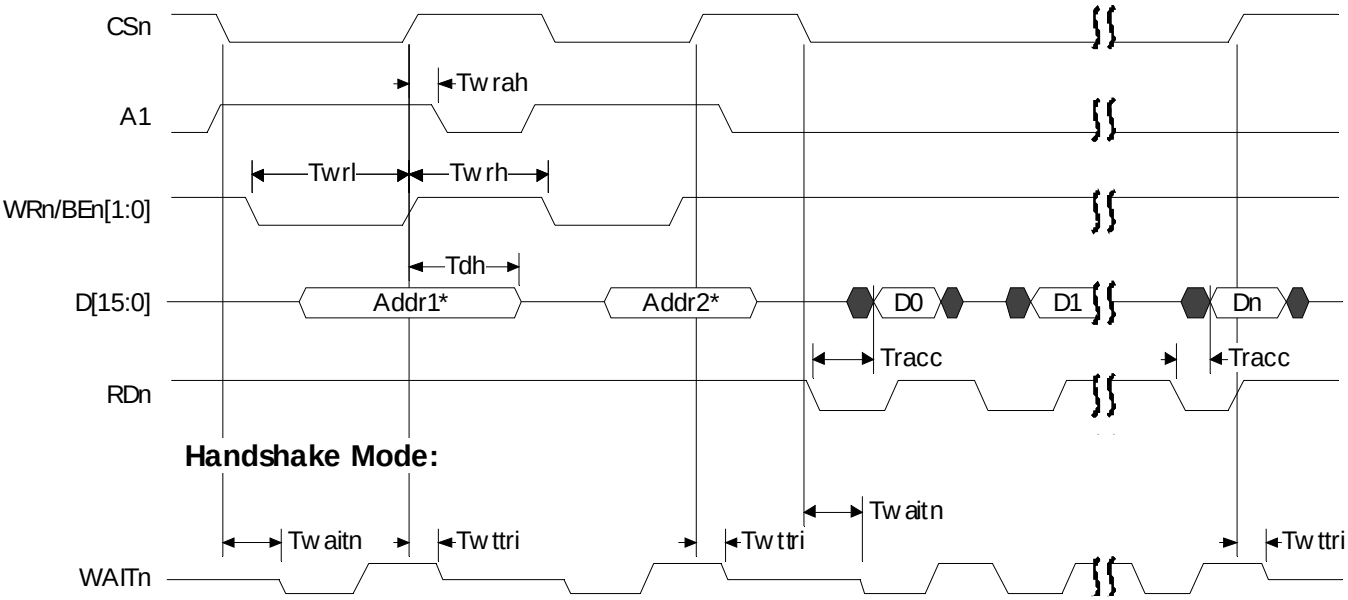
* See the following table for bit mappings.

Table 3.18 Register Read D[15:0] Bit Mapping for Addr* in Figure 3.22

Data Bus	Address Phase			
	16bit Host Bus	8bit Host Bus		
	Addr1	Addr1	Addr2	Addr3
D[15]	x			
D[14]	x			
D[13]	A[12]			
D[12]	A[11]			
D[11]	A[10]			
D[10]	A[9]			
D[9]	A[8]			
D[8]	A[7]			
D[7]	A[6]	A[4]	A[9]	x
D[6]	A[5]	A[3]	A[8]	x
D[5]	A[4]	A[2]	A[7]	A[12]
D[4]	A[3]	A[1]	A[6]	A[11]
D[3]	A[2]	A[0]	A[5]	A[10]
D[2]	A[1]	0	1	0
D[1]	x	0	0	1
D[0]	1	1	1	1

Note: To perform Burst Read operations, as shown in Figure 3.22, set DC01[8] = 1.

Figure 3.23: Memory Burst Read, Type A Host Interface, Indirect Addressing



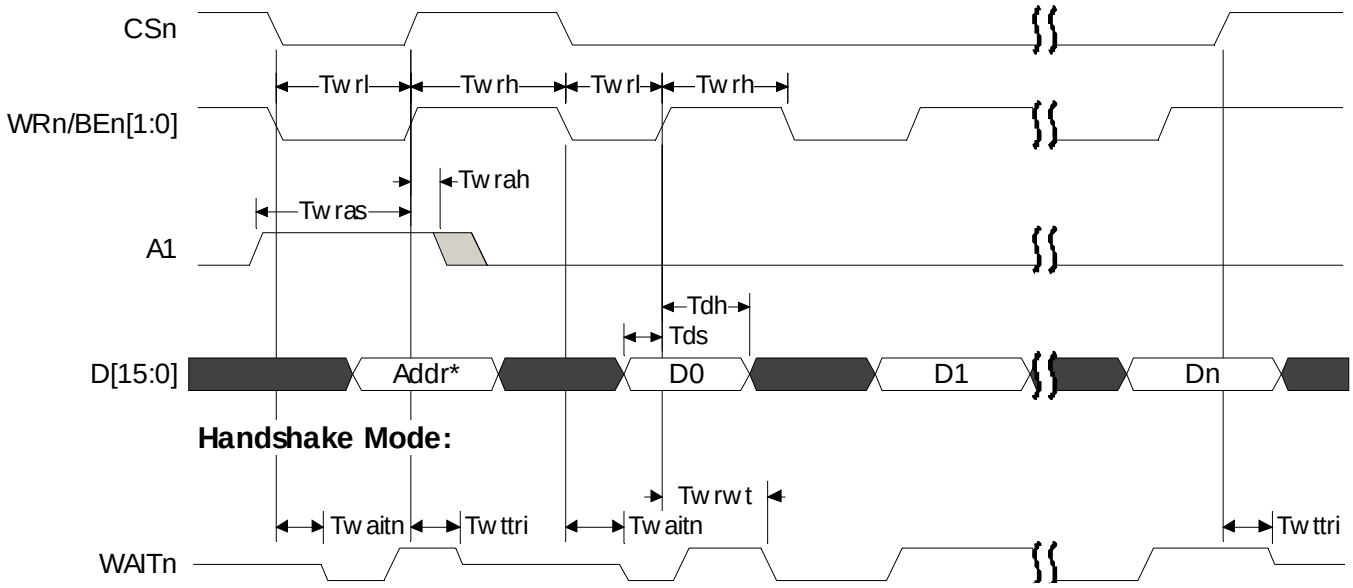
* See the following table for bit mappings.

Table 3.19 Memory Read D[15:0] Bit Mapping for Addr1* and Addr2* in Figure 3.23

Data Bus	Address Phase					
	16bit Host Bus		8bit Host Bus			
	Addr1	Addr2	Addr1	Addr2	Addr3	Addr4
D[15]	A[14]	x				
D[14]	A[13]	x				
D[13]	A[12]	x				
D[12]	A[11]	x				
D[11]	A[10]	x				
D[10]	A[9]	x				
D[9]	A[8]	x				
D[8]	A[7]	x				
D[7]	A[6]	x	A[4]	A[9]	A[14]	A[19]
D[6]	A[5]	A[19]	A[3]	A[8]	A[13]	A[18]
D[5]	A[4]	A[18]	A[2]	A[7]	A[12]	A[17]
D[4]	A[3]	A[17]	A[1]	A[6]	A[11]	A[16]
D[3]	A[2]	A[16]	A[0]	A[5]	A[10]	A[15]
D[2]	A[1]	A[15]	0	1	0	1
D[1]	0	1	0	0	1	1
D[0]	0	0	0	0	0	0

Note: To perform Burst Read operations, as shown in Figure 3.23 set DC01[8] = 1

Figure 3.24: Register Burst Write, Type A Host Interface, Indirect Addressing



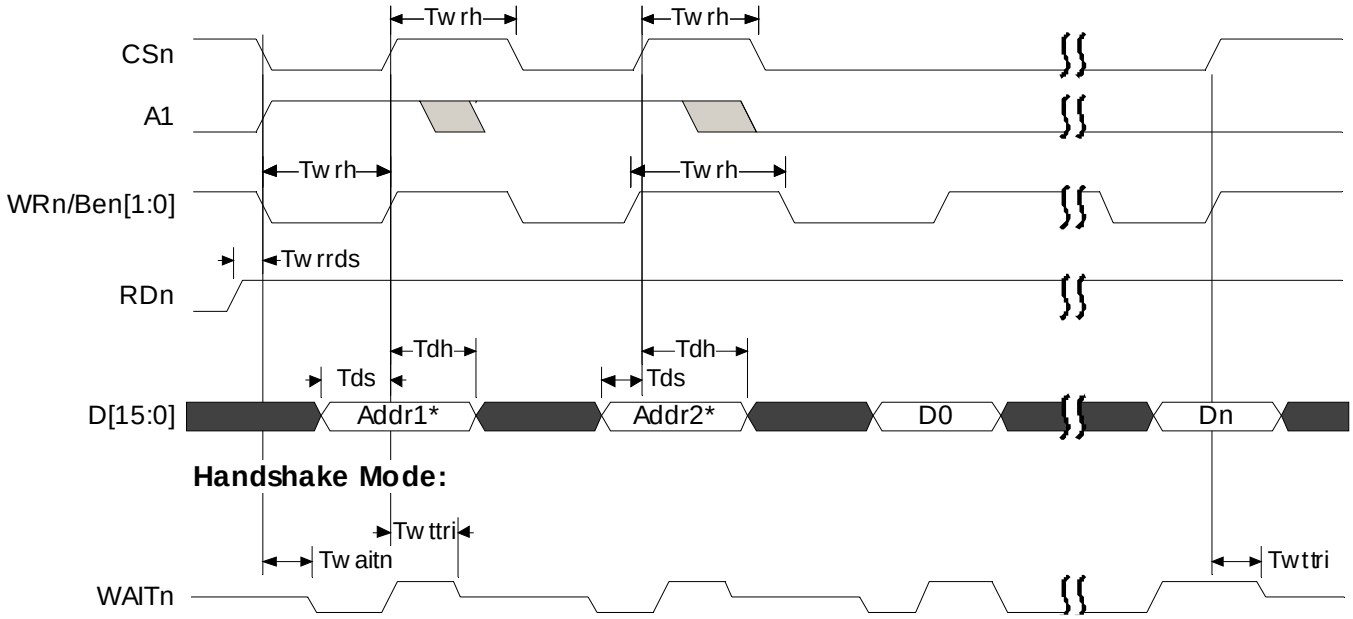
* See the following table for bit mappings.

Table 3.20 Register Burst Write D[15:0] Bit Mapping for Addr* in Figure 3.24

Data Bus	Address Phase			
	16bit Host Bus	8bit Host Bus		
	Addr1	Addr1	Addr2	Addr3
D[15]	x			
D[14]	x			
D[13]	A[12]			
D[12]	A[11]			
D[11]	A[10]			
D[10]	A[9]			
D[9]	A[8]			
D[8]	A[7]			
D[7]	A[6]	A[4]	A[9]	x
D[6]	A[5]	A[3]	A[8]	x
D[5]	A[4]	A[2]	A[7]	A[12]
D[4]	A[3]	A[1]	A[6]	A[11]
D[3]	A[2]	A[0]	A[5]	A[10]
D[2]	A[1]	0	1	0
D[1]	x	0	0	1
D[0]	1	1	1	1

Note: To perform Burst Write operations as shown in Figure 3.24 set DC01[9] = 1.

Figure 3.25: Memory Burst Write, Type A Host Interface, Indirect Addressing



* See the following table for bit mappings.

Table 3.21 Memory Write D[15:0] Bit Mapping for Addr1* and Addr2* in Figure 3.25

Data Bus	Address Phase					
	16bit Host Bus		8bit Host Bus			
	Addr1	Addr2	Addr1	Addr2	Addr3	Addr4
D[15]	A[14]	x				
D[14]	A[13]	x				
D[13]	A[12]	x				
D[12]	A[11]	x				
D[11]	A[10]	x				
D[10]	A[9]	x				
D[9]	A[8]	x				
D[8]	A[7]	x				
D[7]	A[6]	x	A[4]	A[9]	A[14]	A[19]
D[6]	A[5]	A[19]	A[3]	A[8]	A[13]	A[18]
D[5]	A[4]	A[18]	A[2]	A[7]	A[12]	A[17]
D[4]	A[3]	A[17]	A[1]	A[6]	A[11]	A[16]
D[3]	A[2]	A[16]	A[0]	A[5]	A[10]	A[15]
D[2]	A[1]	A[15]	0	1	0	1
D[1]	0	1	0	0	1	1
D[0]	0	0	0	0	0	0

Note: To perform Burst Write operations as shown in Figure 3.25 set DC01[9] = 1.

Figure 3.26: Register/Memory Burst Write, Type A Host Interface, 8bit and 16bit Direct Addressing

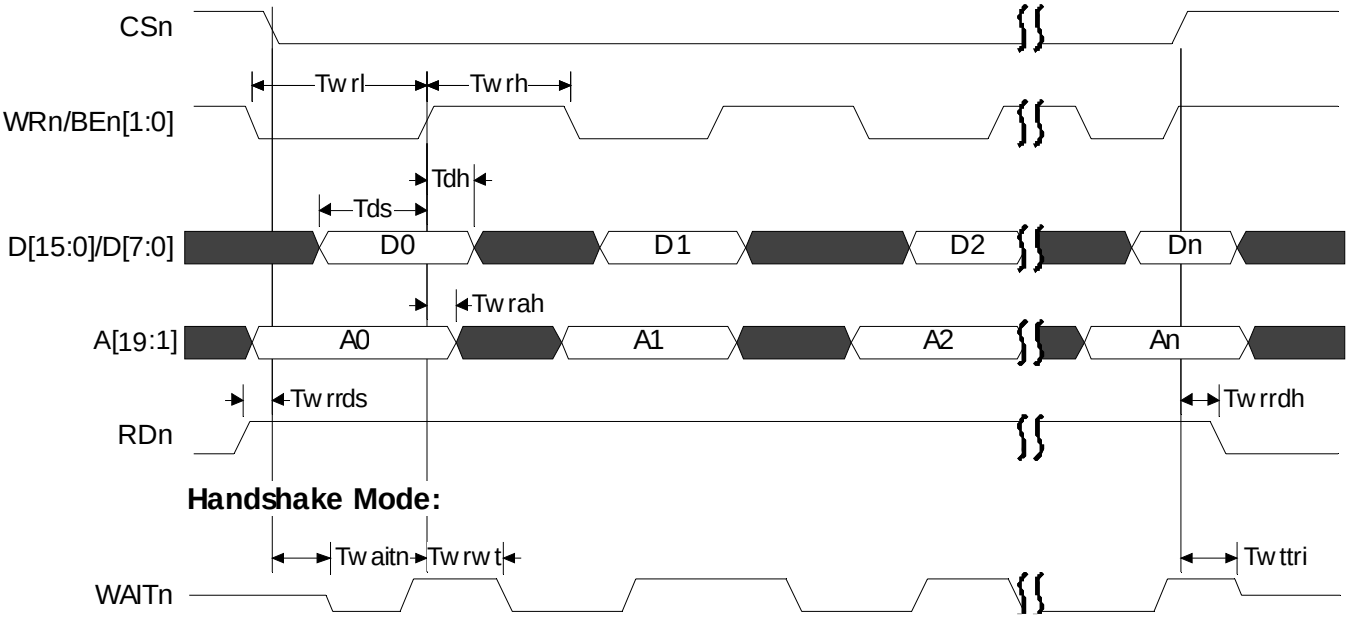


Figure 3.27: Register/Memory Burst Write, Type A Host Interface, 32bit Direct Addressing

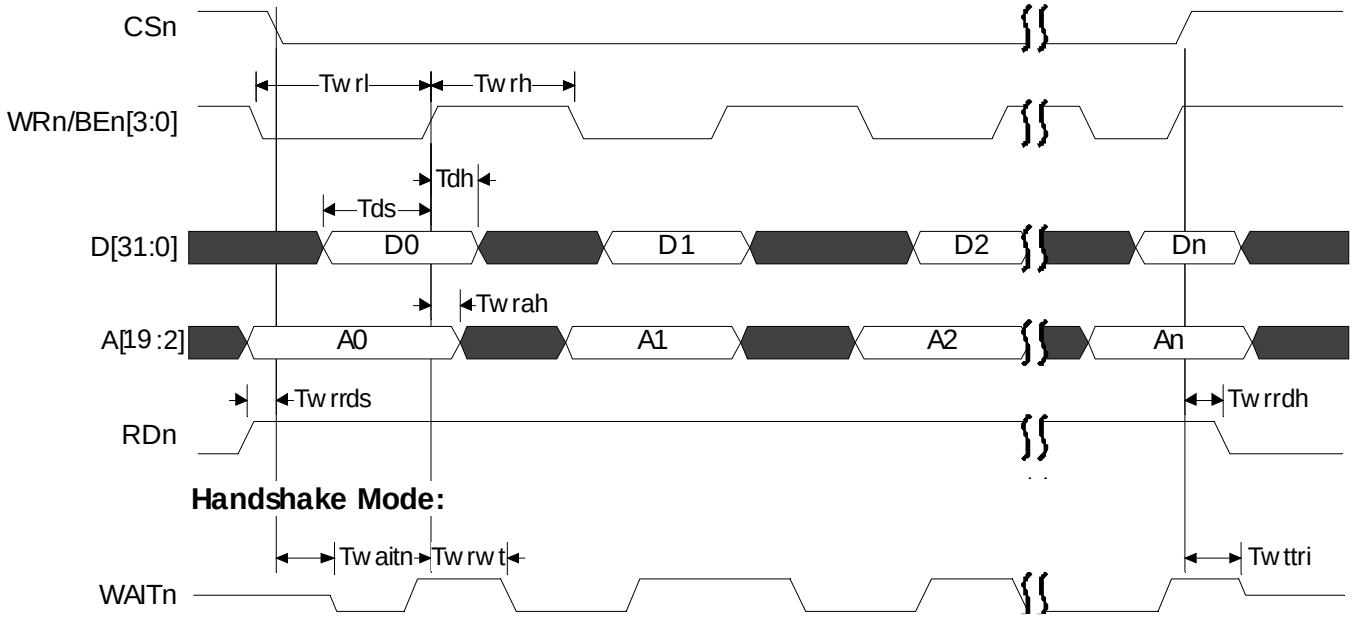


Figure 3.28: Register/Memory Burst Read, Type A Host Interface, 16bit and 8bit, Direct Addressing

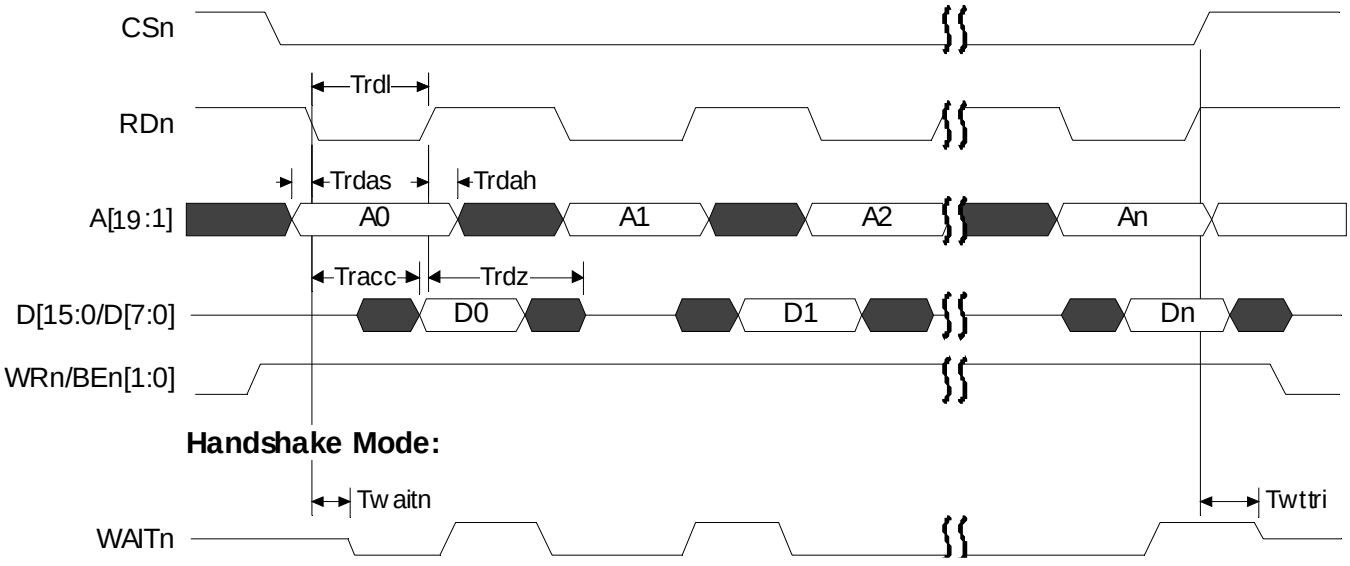
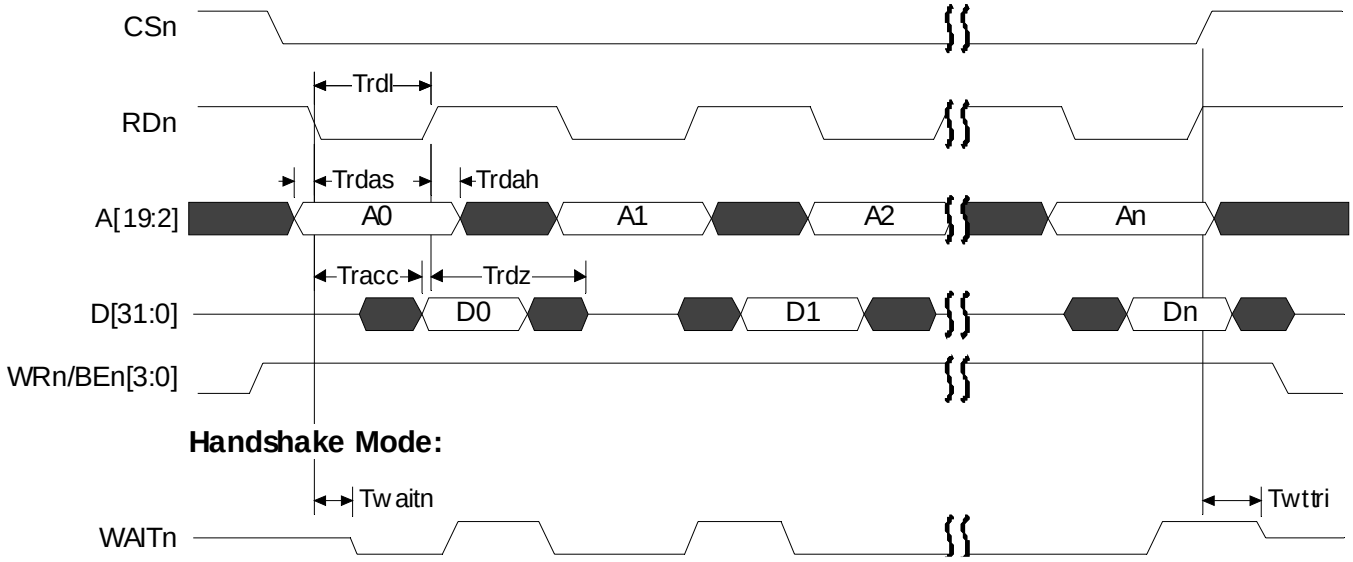


Figure 3.29: Register/Memory Burst Read, Type A Host Interface, 32bit, Direct Addressing



3.4.4.2 Type A Host Interface Timing Parameters

Table 3.19 provides the AC timing parameters for the preceding Type A host interface timing diagrams (Figures 3.8 through 3.29.)

Note: TM is the memory clock period in ns, and TF is the FIFO clock period in ns.

Note: Some timing values vary according to BVDD (1.71 V or 2.4 V) and are listed accordingly.

Table 3.22: Type A Host Interface Timing Parameters

Symbol	Description	Min (ns): Time and Conditions		Max (ns): Time and Conditions	
Tdh	**Write cycles:** Data hold time from rising edge of WRn/CSn, whichever comes first	0		N/A	
Tds	**Write cycles:** Data setup time to rising edge of WRn/CSn whichever comes first.	20		N/A	
Tracc	**Read cycles:** Maximum read access time from the beginning of the read cycle to the first valid data access.	N/A		**2.4 V < BVDD ≤ 3.6 V**	
				4*TM + 35	Memory
				2.5*TF + 30	FIFO Status Registers
				47	Register and JPEG Read DMA FIFO
				1.7 V ≤ BVDD < 2.4	
				4*TM + 50	Memory
				2.5*TF + 50	FIFO Status Registers
				69	Register and JPEG Read DMA FIFO
Trlz	**Read cycles:** Time from RDn low to Data Low-Z for an RDn-controlled read.	0		N/A	
Trdah	**Read cycles:** Address hold time from rising edge of CSn/RDn, whichever comes first.	-0.6		N/A	
Trdas	**Read cycles:** Address setup time to falling edge of CSn/RDn, whichever comes last.	0		N/A	
Trdh	**Read cycles:** Read enable Inactive time measured from the end of one read cycle to the beginning of the next read cycle.	5	No handshake	N/A	
		26	Handshake		
Trdhpg	**Read cycles:** Data hold time from beginning of valid Address access in page mode	N/A		7	
Trdl	**Read cycles:** Read enable active low time. CSn-controlled read cycles:CSn low time RDn-controlled read cycles:RDn low time	**2.4 V < BVDD ≤ 3.6 V**		N/A	
		4*TM + 35	Memory		
		47	Register + JPEG Read DMA FIFO		
		1.7 V ≤ BVDD < 2.4			
		4*TM + 50	Memory		
		69	Register + JPEG Read DMA FIFO		

Table 3.22: Type A Host Interface Timing Parameters

Symbol	Description	Min (ns): Time and Conditions		Max (ns): Time and Conditions	
Trdwt	Time from rising edge of RDn to falling edge of WAITn	N/A		**2.4 V < BVDD ≤ 3.6 V**	
				17	Memory
				31	Register
				1.7 V ≤ BVDD < 2.4	
				27	Memory
				42	Register
Trdz	Time from rising edge of CSn to data bus floating state	6		15	
Trpacc	**Page Mode access:** Maximum read access time *following* the first access of a page.	N/A		**2.4 V < BVDD ≤ 3.6 V**	
				30	Memory
				32	Register and Read DMA FIFO
				1.7 V ≤ BVDD < 2.4	
				45	Memory
				45	Register and Read DMA FIFO
Twaitn	WAITn/RDYn assertion time from the falling edge of WRn/CSn, whichever comes last.	N/A		**2.4 V < BVDD ≤ 3.6 V** 17	
				1.7 V ≤ BVDD < 2.4 40	
Twrah	**Write cycles:** Address hold time from the edge of CSn/WRn, whichever comes first.	0		N/A	
Twras	**Write cycles:** Address valid setup time to the falling edge of CSn/WRn, whichever comes first.	0		N/A	
Twrcyc	**Write cycle time requirement:** Time from the beginning of one write cycle to the beginning of the next write cycle.	$T_{WRL} + T_{WRH}$ **OR** 1.5*TM + 4 (Whichever is longer)		N/A	
Twrh	**Write Enable Inactive Time:** Time from the end of one write cycle to the beginning of the next write cycle.	10	No handshake	N/A	
		26	Handshake		
Twrl	**Write Enable Active time:** CSn-controlled write cycle: CSn active time WRn-controlled write cycle: WRn active time	**2.4 V < BVDD ≤ 3.6 V** 30		N/A	
		1.7 V ≤ BVDD < 2.4 45			
Twrrdh	**Write cycles:** Time from the end of one read cycle to WRn assertion Time from CSn rising edge to WRn falling edge	5	No Handshake	N/A	
		26	Handshake		
	Read cycles: Time from the end of one read cycle to RDn assertion Time from CSn rising edge to RDn falling edge	5	No Handshake	N/A	
		26	Handshake		

Table 3.22: Type A Host Interface Timing Parameters

Symbol	Description	Min (ns): Time and Conditions		Max (ns): Time and Conditions
Twrrds	**Write cycles:** Time the RDn is high before a write cycle: Time from RDn rising edge to WRn falling edge.	5	No handshake	N/A
		26	Handshake	
	Read cycles: Time the WRn is high before a read cycle: Time from WRn rising edge to RDn falling edge.	5	No handshake	
		26	Handshake	
Twrwt	Time from WRn rising edge until WAITn falling edge	N/A		**2.4 V < BVDD ≤ 3.6 V** 17
				1.7 V ≤ BVDD < 2.4 26
Twttri	Time from rising edge of CSn to beginning of tri-state condition of WAITn	N/A		29

3.4.4.3 Type B Host Interface

This section shows the timing characteristics for a Type B Host Bus interface using both direct addressing and indirect addressing.

- Direct Addressing Read/Write Timing Diagrams
  Figure 3.30 through Figure 3.33

- Indirect Addressing Read/Write Timing Diagrams
  Figure 3.34 through Figure 3.37

All Type B Timing Diagrams refer to the timing parameters in Table 3.28.

Note: The WAITn signal used in handshake mode and Page mode writes and reads is tri-stated. Use either a pull-up or a pull-down resistor with this signal, according to the Host CPU specifications.

Note: For an 8bit Type B Host Interface tie DSn0 to ground. If it is already being driven in 8bit mode, tie it to the related host pin.

Table 3.23 Type B Data Strobe (Byte Enable) Signals for Different Size Host Busses

Type B Host Interface Signal Name	32bit Host Bus		16bit Host Bus		8bit Host Bus	
	Function	Signal	Function	Signal	Function	Signal
DSn0	Data Strobe 1 [7:0]	DSn0	Data Strobe 1 [7:0]	DSn0	Data Strobe 1 [7:0] (Tied low or to a related host pin.)	DSn0
DSn1	Data Strobe 2 [15:8]	DSn1	Data Strobe 2 [15:8]	DSn1	A[0]	A[0]
DSn2	Data Strobe 3 [23:16]	DSn2	A1	A1	A1	A1
DSn3	Data Strobe 4 [31:24]	DSn3	Not used: Tie low externally	N/A	Not used: Tie low externally	N/A

Figure 3.30: CS-controlled Write, Type B 8bit and 16bit Host Interface, Direct Addressing

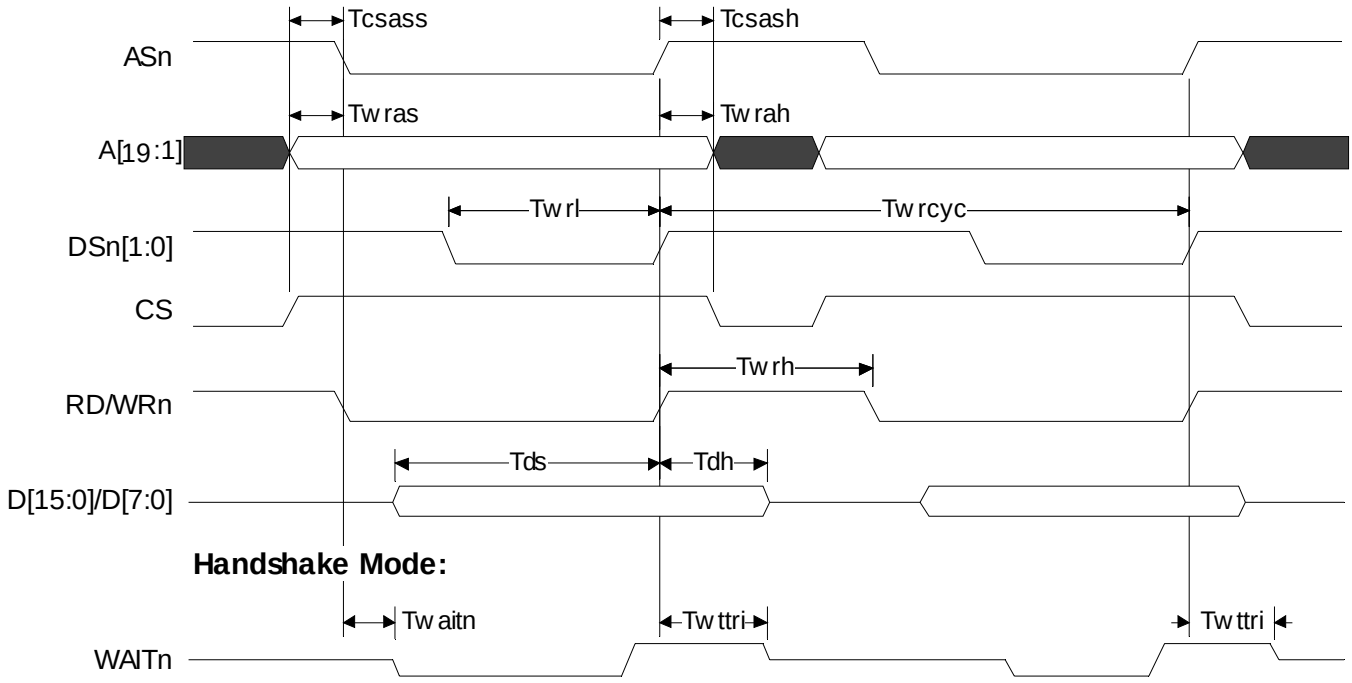


Figure 3.31: CS-controlled Write Operation, Type B 32bit Host Interface, Direct Addressing

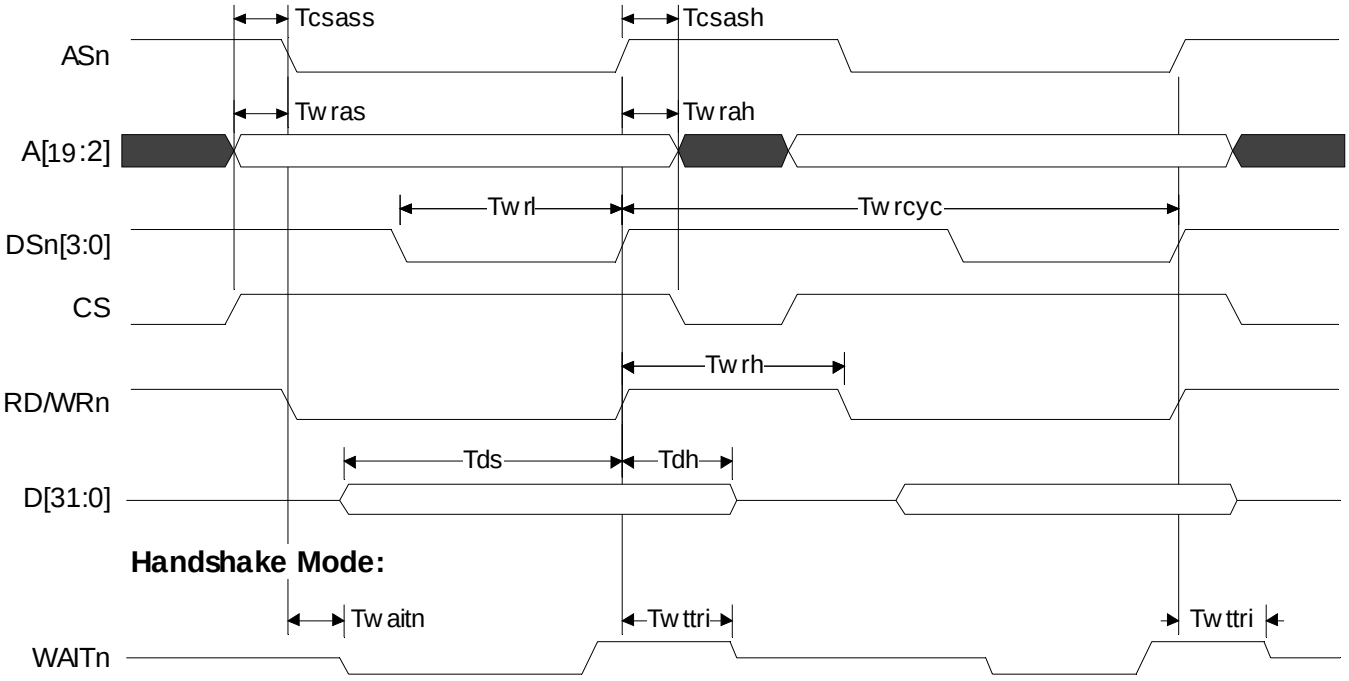


Figure 3.32: CS-controlled Read, Type B 8bit and 16bit Host Interface, Direct Addressing

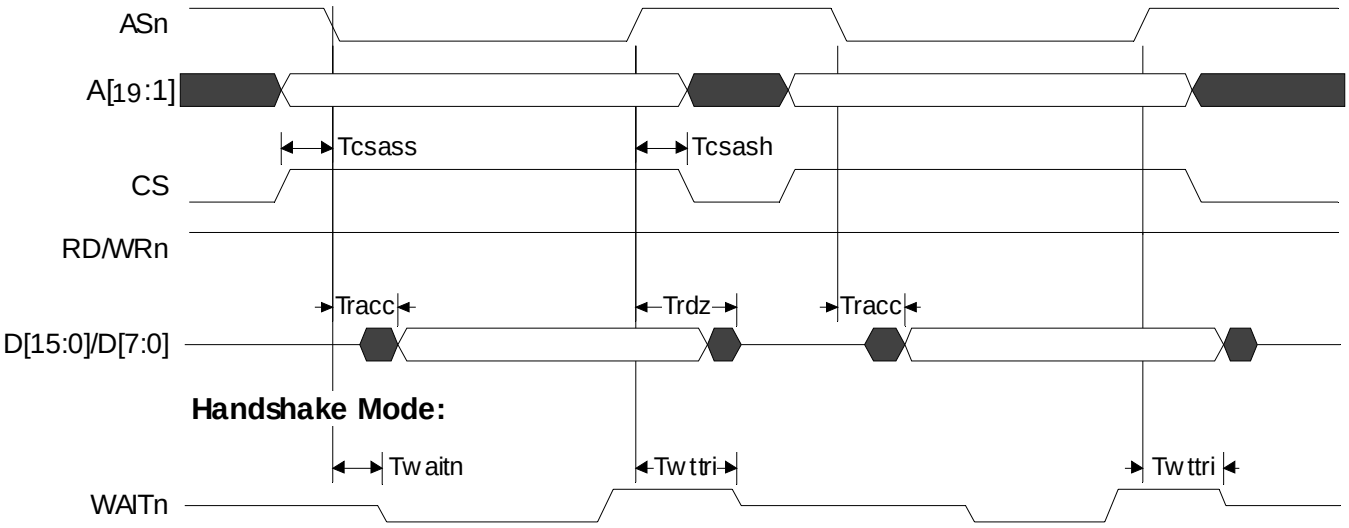


Figure 3.33: CS-controlled Read, Type B 32bit Host Interface, Direct Addressing

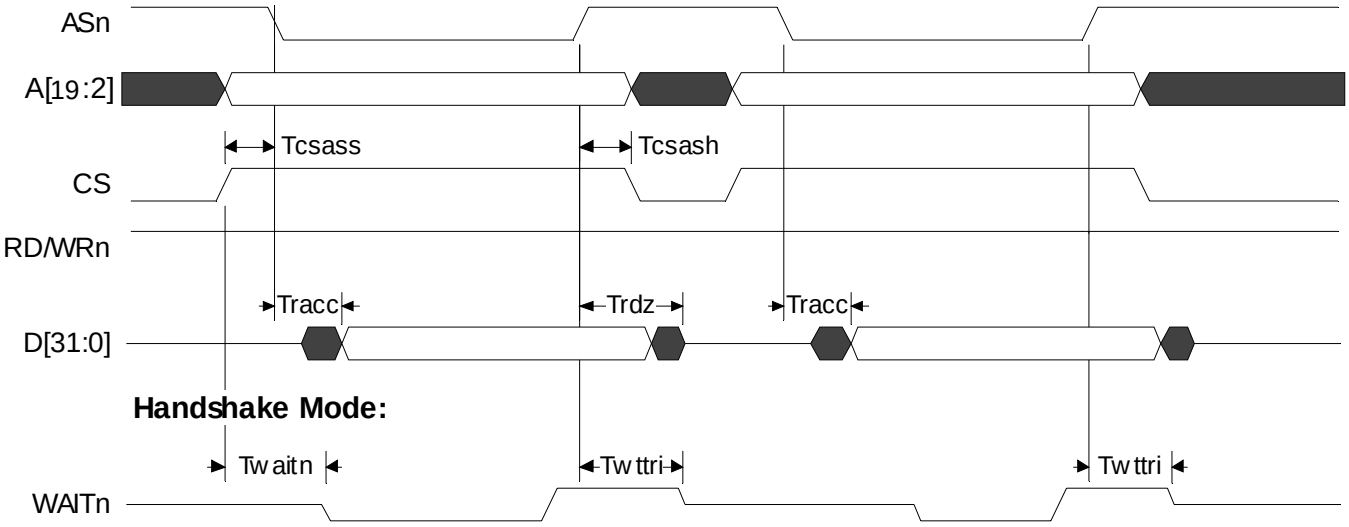
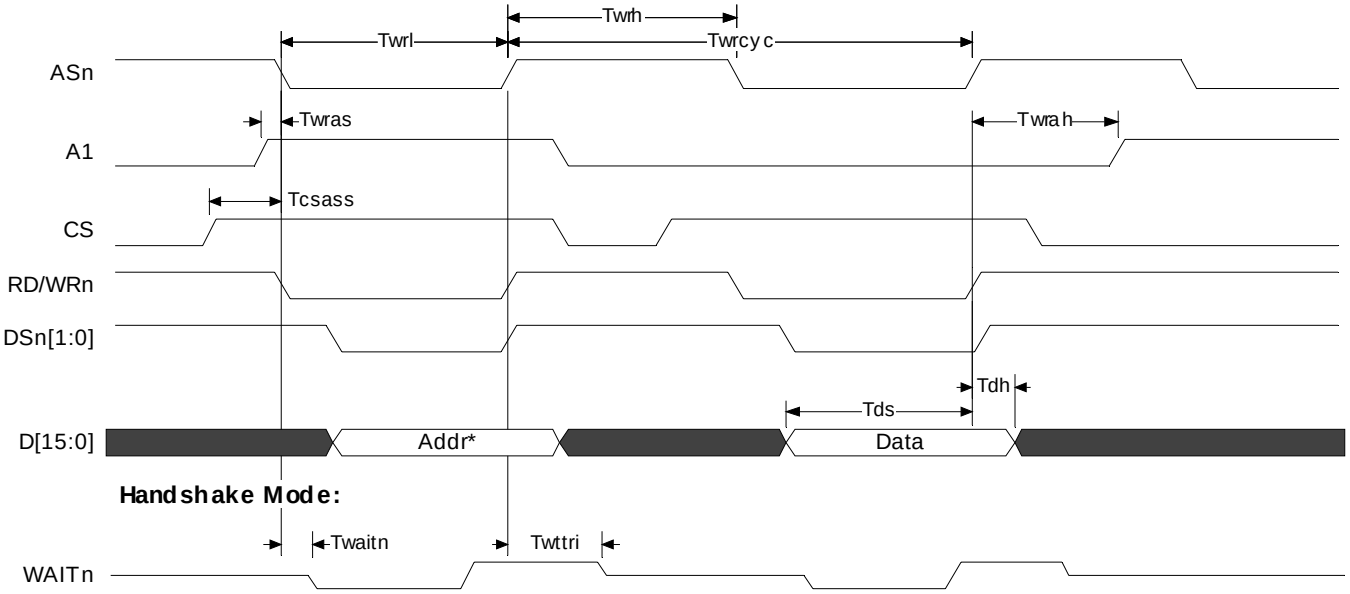


Figure 3.34: Register Write, Type B Host Interface, Indirect Addressing

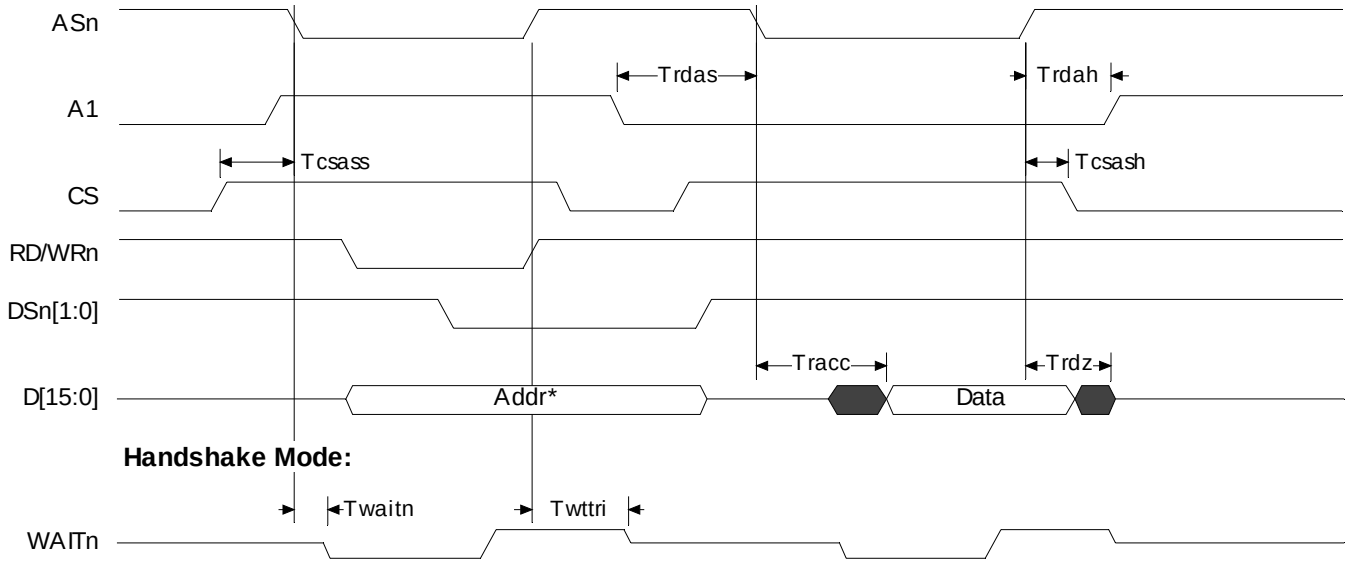


* See the following table for bit mappings.

Table 3.24 Register Write D[15:0] Bit Mapping for Addr* in Figure 3.34

Data Bus	Address Phase			
	16bit Host Bus	8bit Host Bus		
	Addr*	Addr*1	Addr*2	Addr*3
D[15]	x			
D[14]	x			
D[13]	A[12]			
D[12]	A[11]			
D[11]	A[10]			
D[10]	A[9]			
D[9]	A[8]			
D[8]	A[7]			
D[7]	A[6]	A[4]	A[9]	x
D[6]	A[5]	A[3]	A[8]	x
D[5]	A[4]	A[2]	A[7]	A[12]
D[4]	A[3]	A[1]	A[6]	A[11]
D[3]	A[2]	A[0]	A[5]	A[10]
D[2]	A[1]	0	1	0
D[1]	x	0	0	1
D[0]	1	1	1	1

Figure 3.35: Register Read, Type B Host Interface, Indirect Addressing

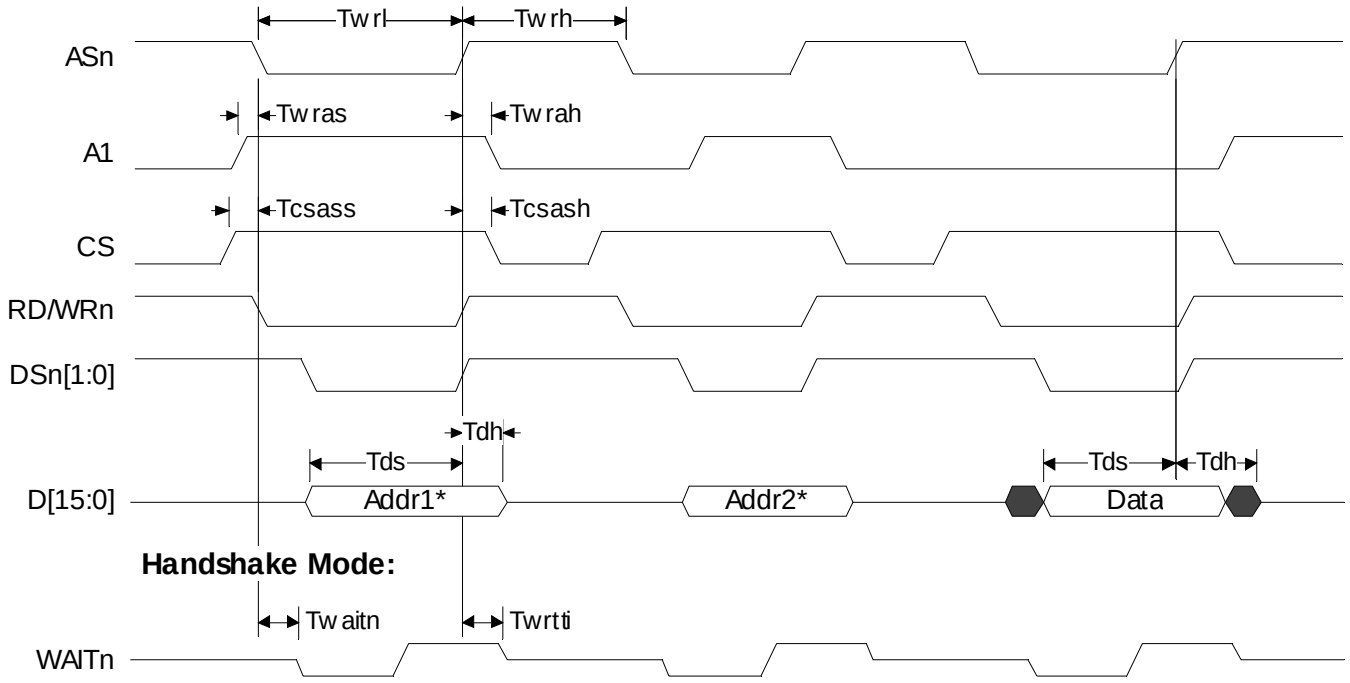


* See the following table for bit mappings.

Table 3.25 Register Read D[15:0] Bit Mapping for Addr* in Figure 3.35

Data Bus	Address Phase			
	16bit Host Bus	8bit Host Bus		
	Addr*	Addr*1	Addr*2	Addr*3
D[15]	x			
D[14]	x			
D[13]	A[12]			
D[12]	A[11]			
D[11]	A[10]			
D[10]	A[9]			
D[9]	A[8]			
D[8]	A[7]			
D[7]	A[6]	A[4]	A[9]	x
D[6]	A[5]	A[3]	A[8]	x
D[5]	A[4]	A[2]	A[7]	A[12]
D[4]	A[3]	A[1]	A[6]	A[11]
D[3]	A[2]	A[0]	A[5]	A[10]
D[2]	A[1]	0	1	0
D[1]	x	0	0	1
D[0]	1	1	1	1

Figure 3.36: Memory Write, Type B Host Interface, Indirect Addressing

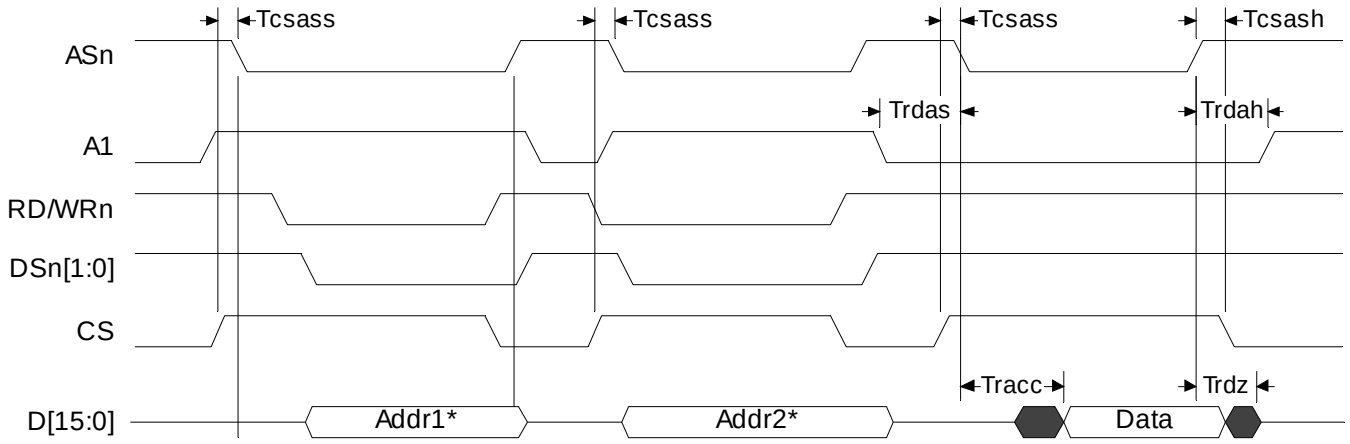


* See the following table for bit mappings.

Table 3.26 Memory Write D[15:0] Bit Mapping for Addr1* and Addr2* in Figure 3.36

Data Bus	Address Phase					
	16bit Host Bus		8bit Host Bus			
	Addr1	Addr2	Addr1	Addr2	Addr3	Addr4
D[15]	A[14]	x				
D[14]	A[13]	x				
D[13]	A[12]	x				
D[12]	A[11]	x				
D[11]	A[10]	x				
D[10]	A[9]	x				
D[9]	A[8]	x				
D[8]	A[7]	x				
D[7]	A[6]		A[4]	A[9]	A[14]	A[19]
D[6]	A[5]	A[19]	A[3]	A[8]	A[13]	A[18]
D[5]	A[4]	A[18]	A[2]	A[7]	A[12]	A[17]
D[4]	A[3]	A[17]	A[1]	A[6]	A[11]	A[16]
D[3]	A[2]	A[16]	A[0]	A[5]	A[10]	A[15]
D[2]	A[1]	A[15]	0	1	0	1
D[1]	0	1	0	0	1	1
D[0]	0	0	0	0	0	0

Figure 3.37: Memory Read, Type B Host Interface, Indirect Addressing



* See the following table for bit mappings.

Table 3.27 Memory Read D[15:0] Bit Mapping for Addr1* and Addr2* in Figure 3.37

Data Bus	Address Phase					
	16bit Host Bus		8bit Host Bus			
	Addr1	Addr2	Addr1	Addr2	Addr3	Addr4
D[15]	A[14]	x				
D[14]	A[13]	x				
D[13]	A[12]	x				
D[12]	A[11]	x				
D[11]	A[10]	x				
D[10]	A[9]	x				
D[9]	A[8]	x				
D[8]	A[7]	x				
D[7]	A[6]	x	A[4]	A[9]	A[14]	A[19]
D[6]	A[5]	A[19]	A[3]	A[8]	A[13]	A[18]
D[5]	A[4]	A[18]	A[2]	A[7]	A[12]	A[17]
D[4]	A[3]	A[17]	A[1]	A[6]	A[11]	A[16]
D[3]	A[2]	A[16]	A[0]	A[5]	A[10]	A[15]
D[2]	A[1]	A[15]	0	1	0	1
D[1]	0	1	0	0	1	1
D[0]	0	0	0	0	0	0

Figure 3.38: Register/Memory Page Read, Type B 8bit and 16bit Host Interface, Direct Addressing

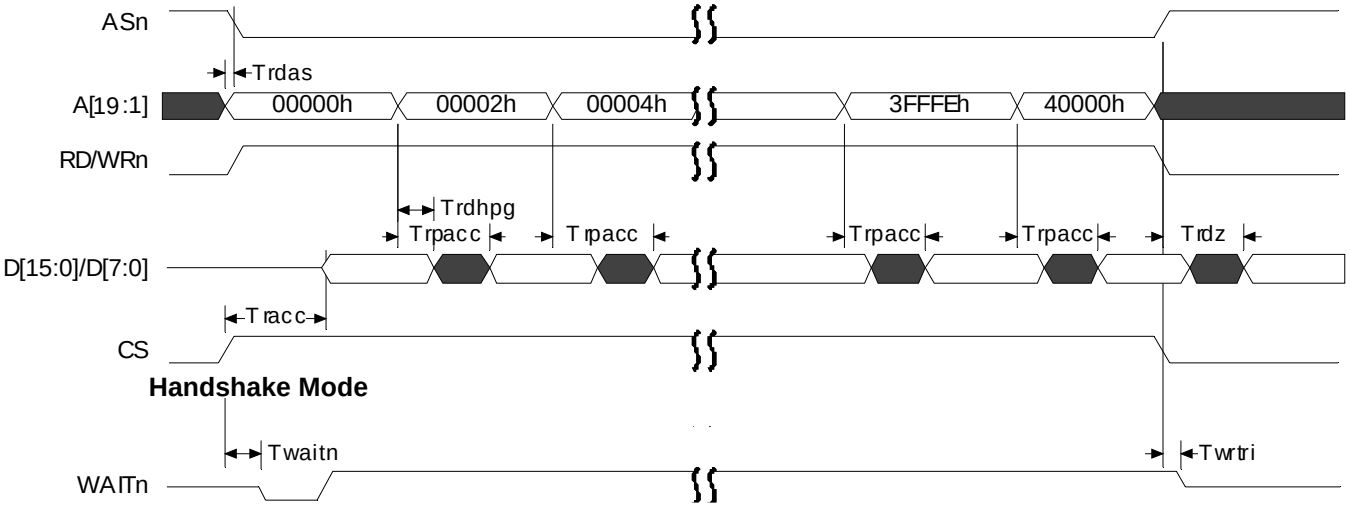
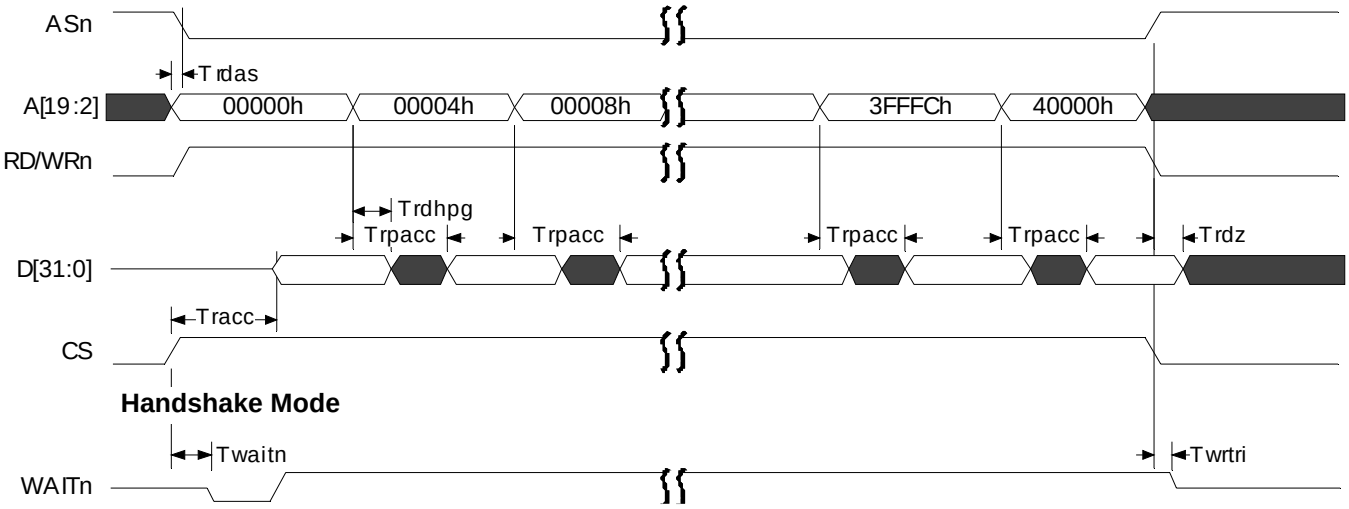


Figure 3.39: Register/Memory Page Read, Type B 32bit Host Interface, Direct Addressing



3.4.4.4 Type B Host Interface Timing Parameters

Table 3.29 provides the AC timing parameters for the preceding Type B-style host interface timing diagrams in Figure 3.30 through Figure 3.39.

Note: TM is the memory clock period in ns. TF is the FIFO clock period.

Table 3.28 Type B Host Interface Timing Parameters

Symbol	Description	Min (ns): Time and Conditions		Max (ns): Time and Conditions	
Tcsash	**CSn Hold** CS hold time from rising edge of ASn	0		N/A	
Tcsass	**CS Setup** CS setup time to falling edge of ASn	0		N/A	
Tdh	**Write cycles:** Data hold time from rising edge of WRn/ASn, or falling edge of RD, whichever comes first	0		N/A	
Tds	**Write cycles:** Data setup time to rising edge of WRn/ASn, whichever comes first.	20		N/A	
Tracc	**Read cycles:** Maximum read access time from the beginning of the read cycle to the first valid data access.	N/A		**2.4 V < BVDD ≤ 3.6 V**	
				4*TM + 35	Memory
				2.5*TF + 30	FIFO Status Registers
				47	Registers and JPEG Read DMA FIFO
				1.7 V ≤ BVDD < 2.4 V	
				4*TM + 50	Memory
				2.5*TF + 50	FIFO Status Registers
				69	Registers and JPEG Read DMA FIFO
Trdah	**Read cycles:** Address hold time from rising edge of ASn/WRn, whichever comes first.	0		N/A	
Trdas	**Read cycles:** Address setup time to falling edge of ASn/WRn, whichever is asserted last.	0		N/A	
Trdh	**Read cycles:** Read enable Inactive time from the end of one read cycle to the beginning of the next read cycle.	5	No handshake	N/A	
		26	Handshake		
Trdhpg	Data Hold TIme in Page Mode Read	N/A		7	
Trdl	**Read enable active low time.** ASn-controlled read cycles: ASn low time Rd/WRn-controlled read cycles:RD/WRn high time	**2.4 V < BVDD ≤ 3.6 V**		N/A	
		4*TM + 35	Memory		
		47	Register and JPEG Read DMA FIFO		
		1.7 V ≤ BVDD < 2.4 V			
		4*TM + 50	Memory		
		69	Register + JPEG Read DMA FIFO		
Trdz	Time from rising edge of ASn to data bus floating state	6		15	

Symbol	Description	Min (ns): Time and Conditions		Max (ns): Time and Conditions	
Trpacc	**Page Mode access:** Maximum read access time *following* the first access of a page.	N/A		**2.4 V < BVDD ≤ 3.6 V**	
				30	Memory
				32	Register and JPEG Read DMA FIFO
				1.7 V ≤ BVDD < 2.4 V	
				45	Memory
				45	Register and JPEG Read DMA FIFO
Twaitn	WAITn/RDYn assertion time from the falling edge of WRn/CSn, whichever comes last.	N/A		**2.4 V < BVDD ≤ 3.6 V** 17	
				1.7 V ≤ BVDD < 2.4 V 40	
Twrah	**Write cycles:** Address hold time from the rising edge of ASn/WRn, whichever comes first.	0		N/A	
Twras	**Write cycles:** Address setup time from the edge of ASn/WRn, whichever comes first.	0		N/A	
Twrcyc	**Write cycle time requirement:** Time from the beginning of one write cycle to the beginning of the next write cycle.	1.5*TM +4 OR $T_{WRL} + T_{WRH}$ (Whichever comes first)		N/A	
Twrh	**Write Enable Active Time:** Time from the end of one write cycle to the beginning of the next write cycle	10	No handshake	N/A	
		26	Handshake		
Twrl	**Write Enable Active time:** ASn-controlled write cycle: ASn active time RD/WRn-controlled write cycle: RD/WRn active time	**2.4 V < BVDD ≤ 3.6 V** 30		N/A	
		1.7 V ≤ BVDD < 2.4 V 45			
Twrrds	**Write cycles:** Time the RDn is high before a write cycle: Time from RDn rising edge to ASn falling edge.	5	No handshake	N/A	
		26	Handshake		
	Read cycles: Time the WRn is low before a read cycle:	5	No handshake		
		26	Handshake		
Twrwt	Time from WRn rising edge until WAITn falling edge	N/A		**2.4 V < BVDD ≤ 3.6 V** 17	
				1.7 V ≤ BVDD < 2.4 V 26	
Twttri	Time from rising edge of ASn to beginning of tri-state condition of WAITn	N/A		29	

3.4.4.5 Type C Host Interface

This section shows the timing characteristics for a Type C Host Bus interface using both direct addressing and indirect addressing.

- Direct Addressing Read/Write Timing Diagrams
  Figure 3.42 through Figure 3.53
  Figure 3.60 through Figure 3.63

- Indirect Addressing Read/Write Timing Diagrams
  Figure 3.52 through Figure 3.59

All Type C Timing Diagrams refer to the timing parameters in Table 3.38.

Note: The WAITn signal used in handshake mode, Burst mode, and Page mode writes and reads is tri-stated. Use either a pull-up or a pull-down resistor with this signal, according to the Host CPU specifications.

Note: For an 8bit Type C Host Interface tie WEn to ground or to the related host pin.

Table 3.29 Type C Byte-enable Signals for Different Size Host Busses

Type C Host Interface Signal Name	Function		
	32bit Host Bus	16bit Host Bus	8bit Host Bus
WEn0	Write Enable 1 [7:0]	Write Enable 1 [7:0]	Write Enable 1 [7:0]
WEn1	Write Enable 2 [15:8]	Write Enable 2 [15:8]	A[0]
WEn2	Write Enable 3 [23:16]	A[1]	A[1]
WEn3	Write Enable 4 [31:24]	Not used: Tie low externally	Not used: Tie low externally

Figure 3.40: WEn-controlled Write, Type C 8bit and 16bit Host Interface, Direct Addressing

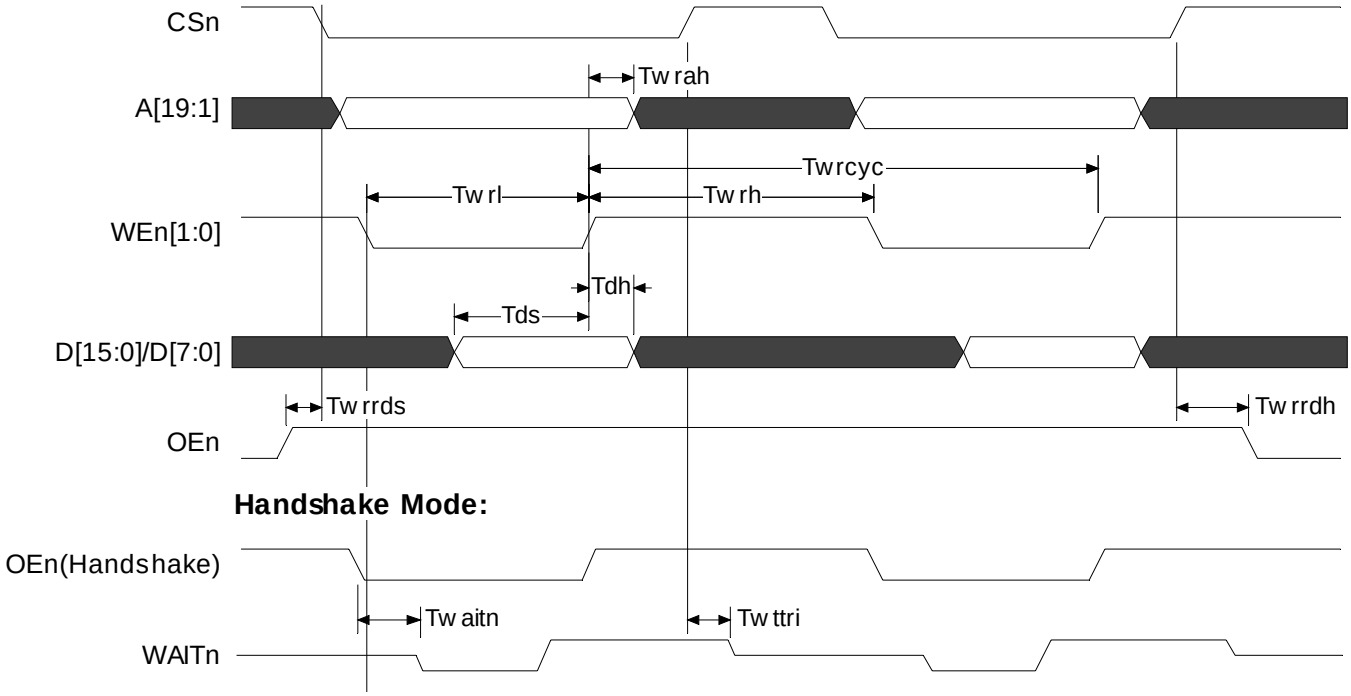


Figure 3.41: WEn-controlled Write, Type C 32bit Host Interface, Direct Addressing

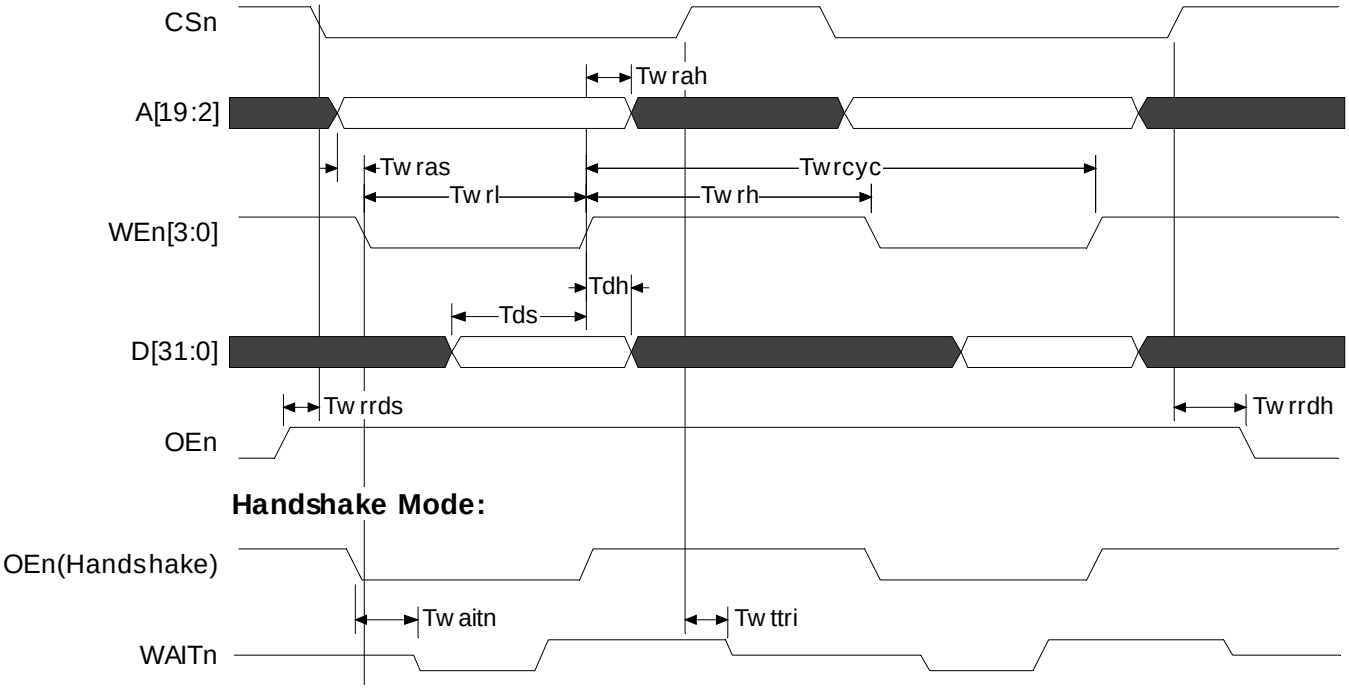


Figure 3.42: CSn-controlled Write, Type C 8bit and 16bit Host Interface, Direct Addressing

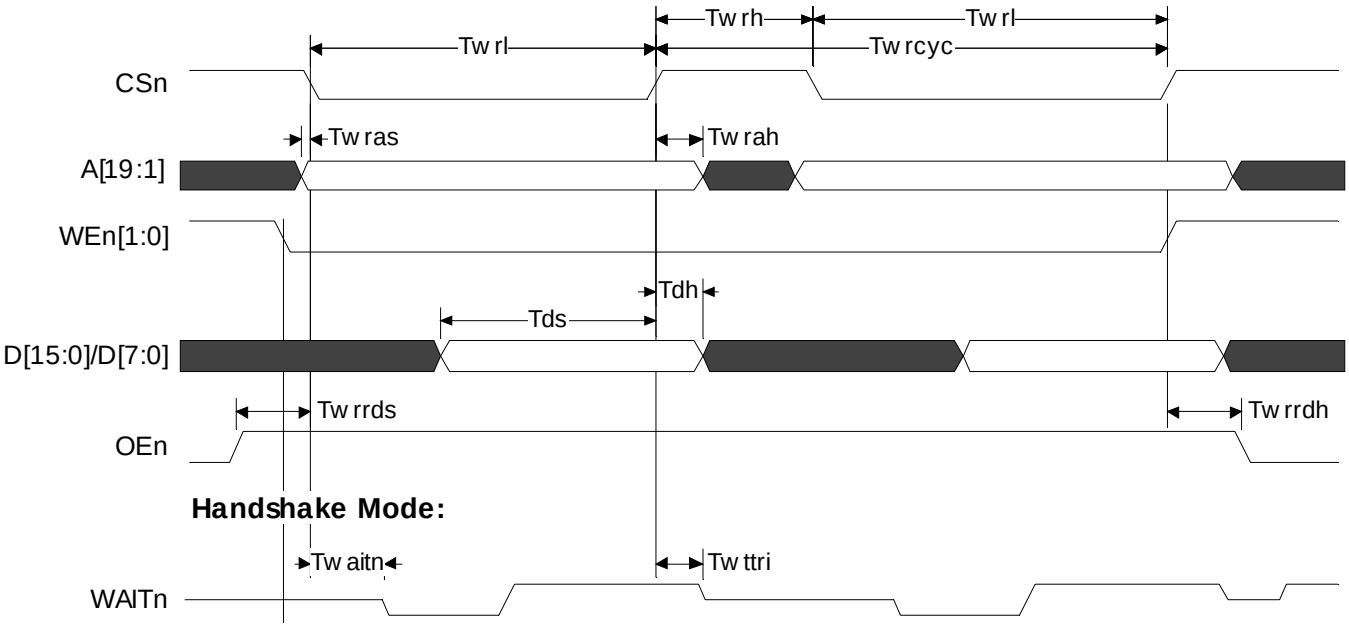


Figure 3.43: CSn-controlled Write, Type C 32bit Host Interface, Direct Addressing

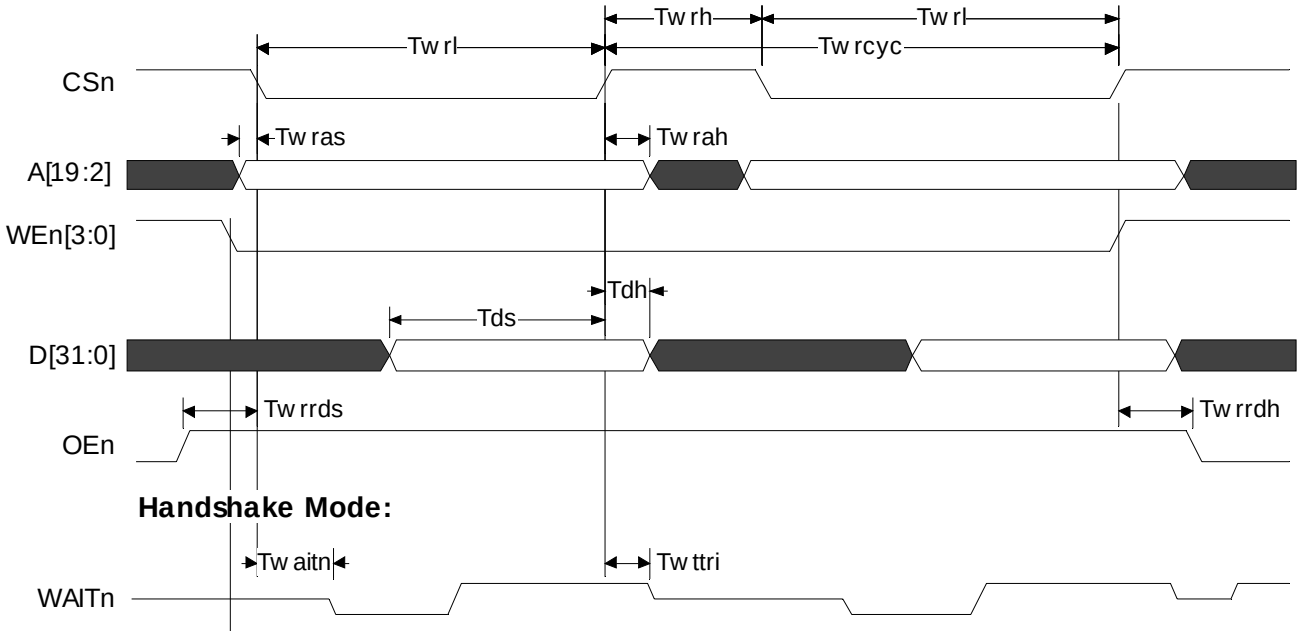


Figure 3.44: OEn-controlled Read, Type C 8bit and 16bit Host Interface, Direct Addressing

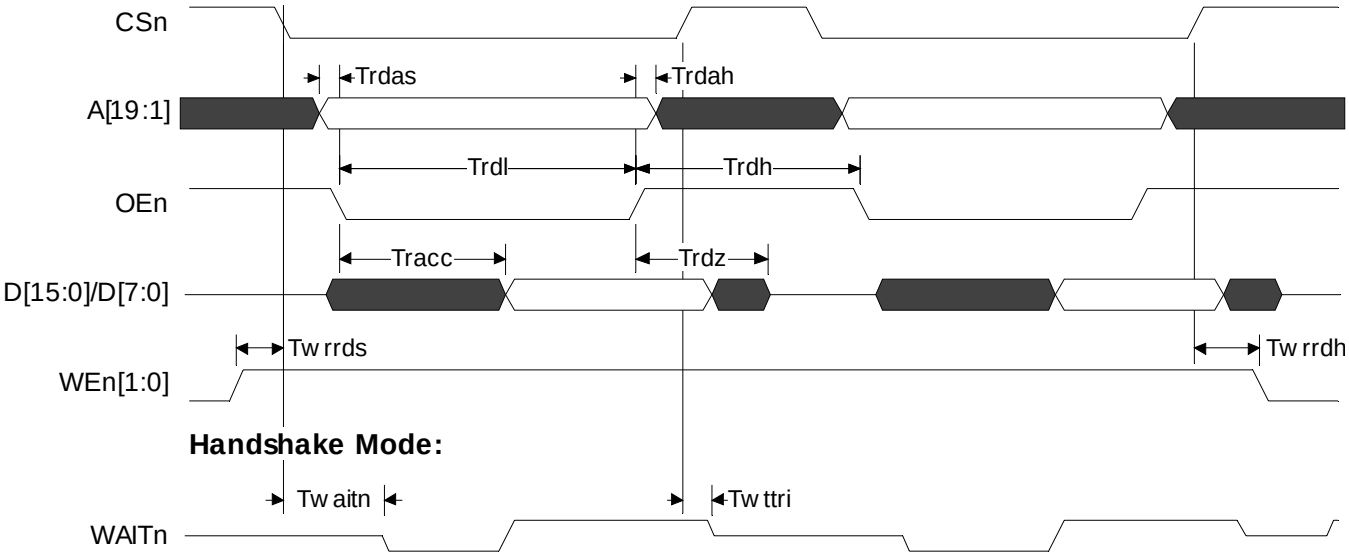


Figure 3.45: OEn-controlled Read, Type C 32bit Host Interface, Direct Addressing

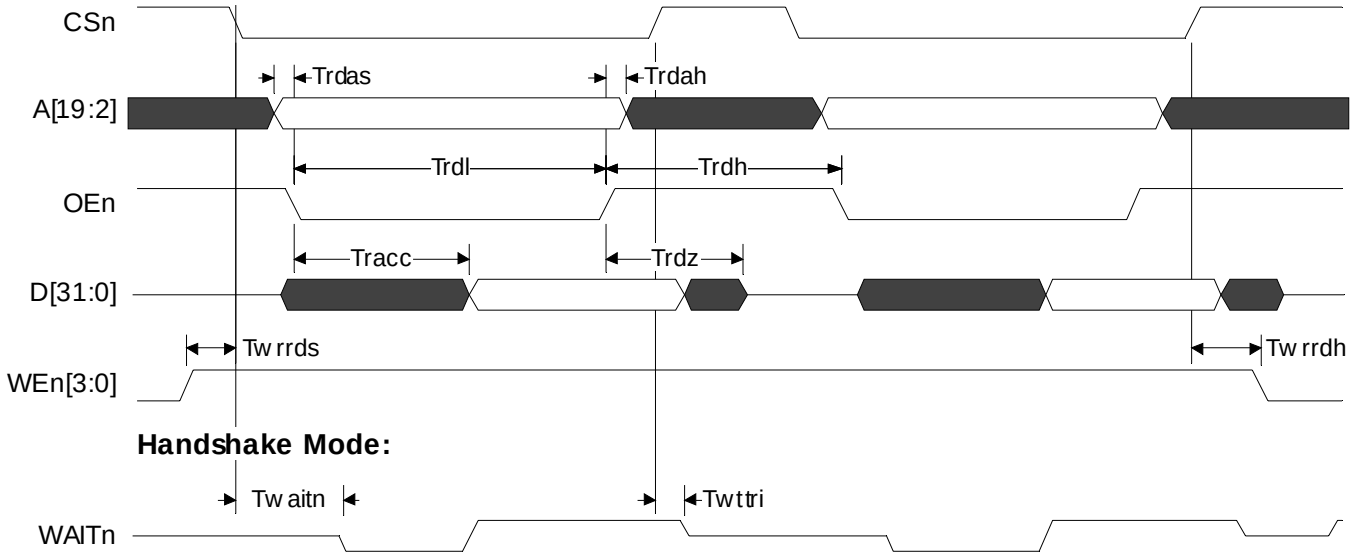


Figure 3.46: CSn-controlled Read, Type C 8bit and 16bit Host Interface, Direct Addressing

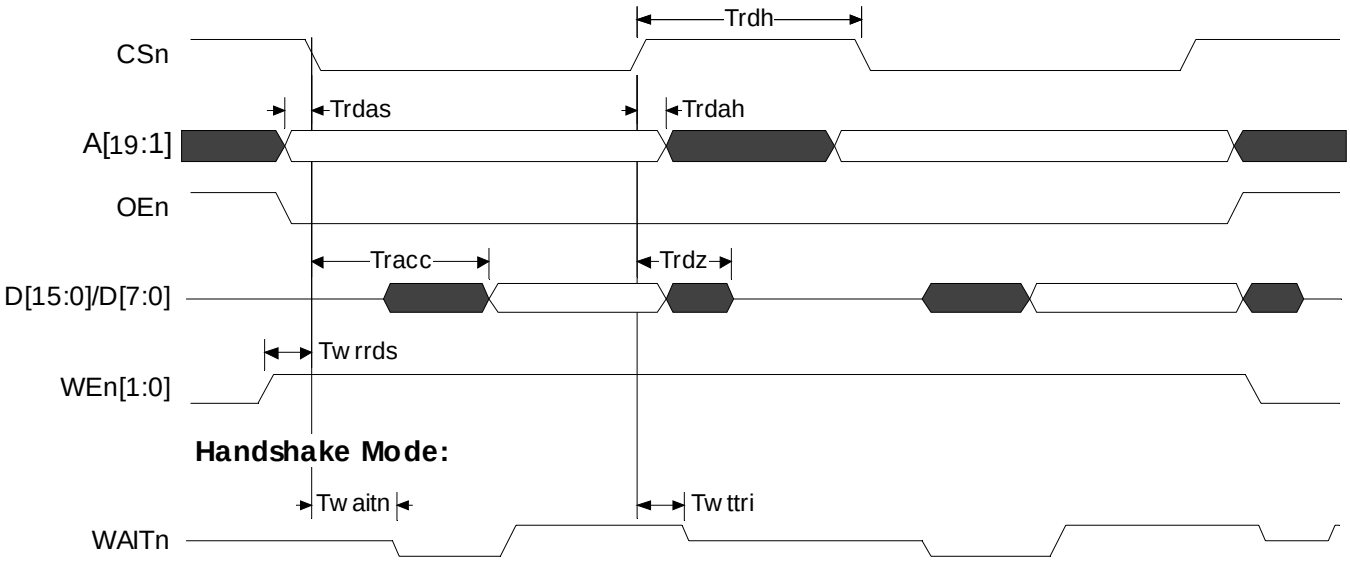


Figure 3.47: CSn-controlled Read, Type C 32bit Host Interface, Direct Addressing

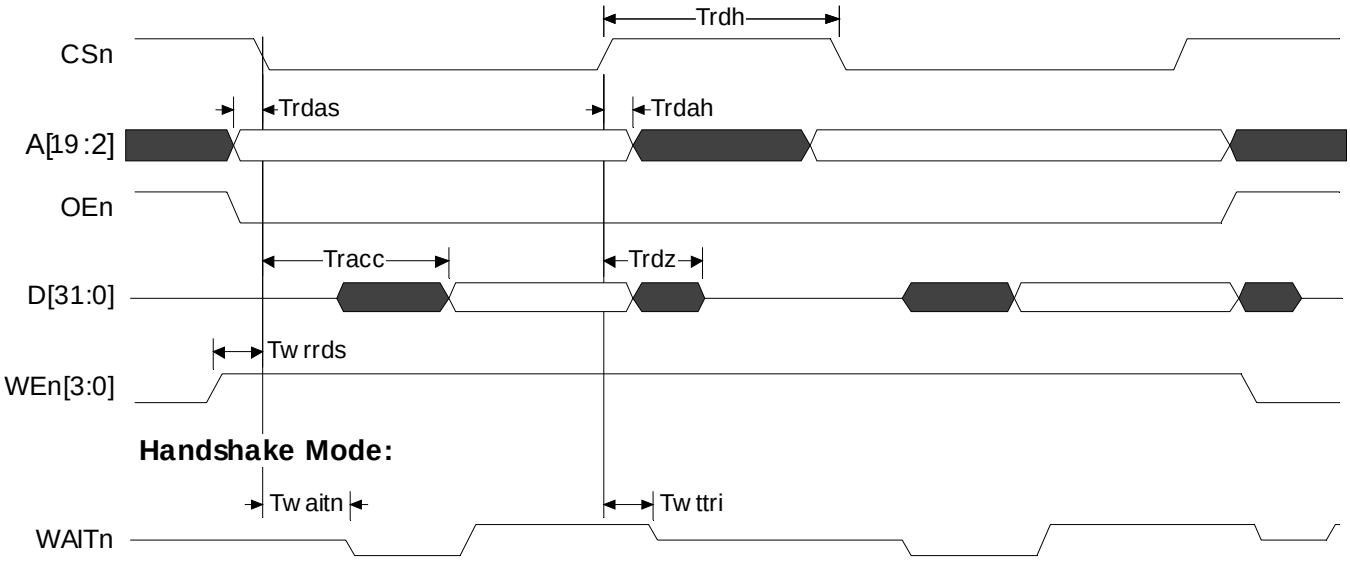
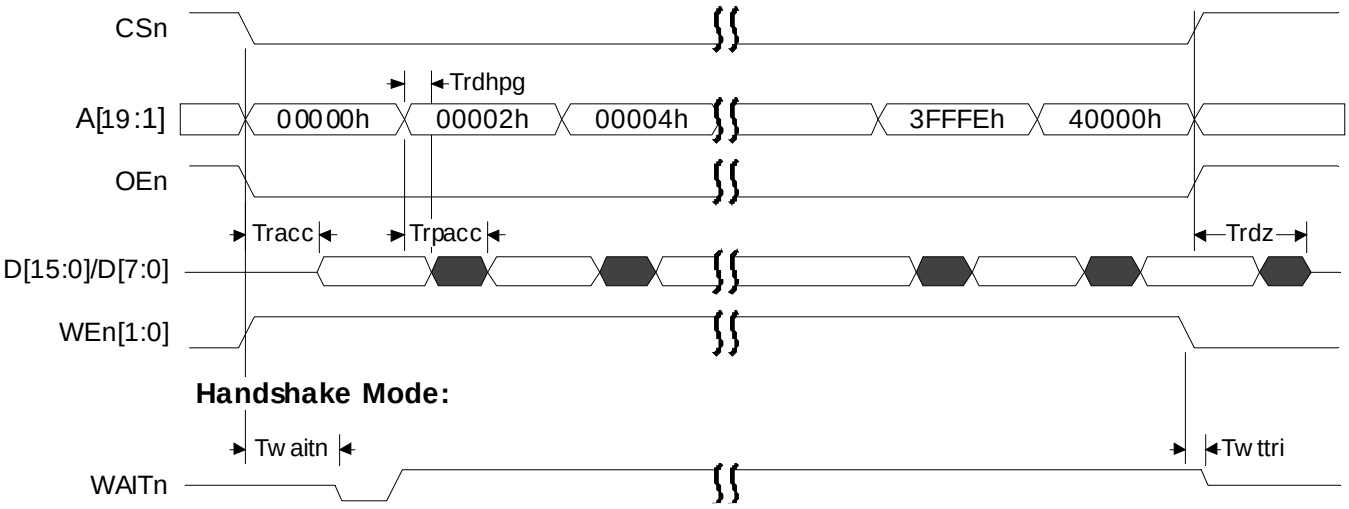
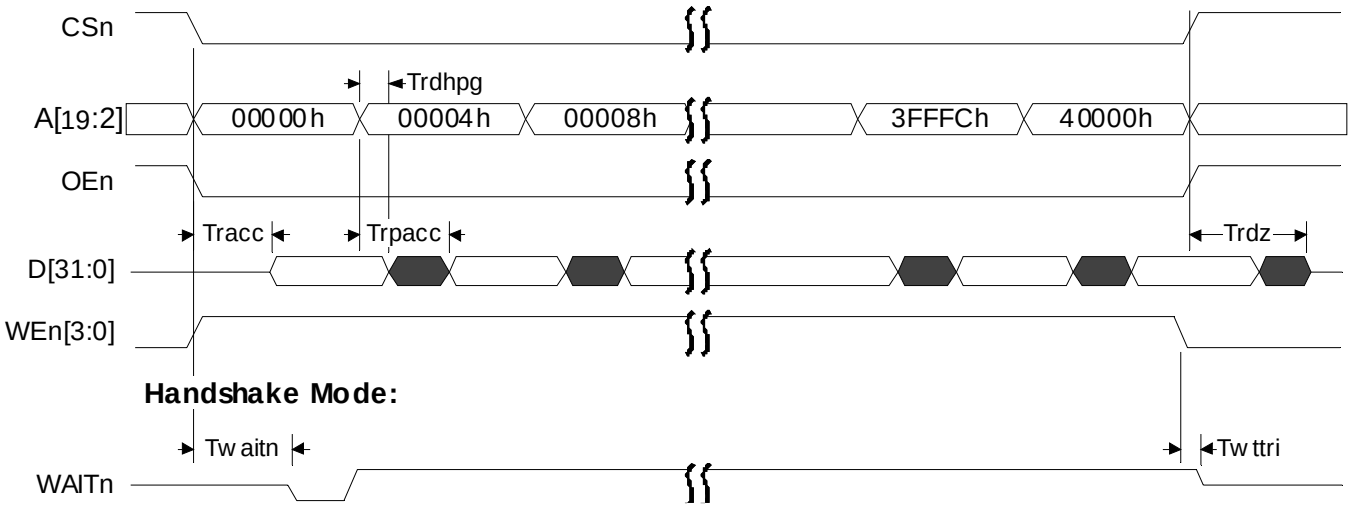


Figure 3.48: Page-Mode Read, Type C 8bit and 16bit Host Interface, Direct Addressing



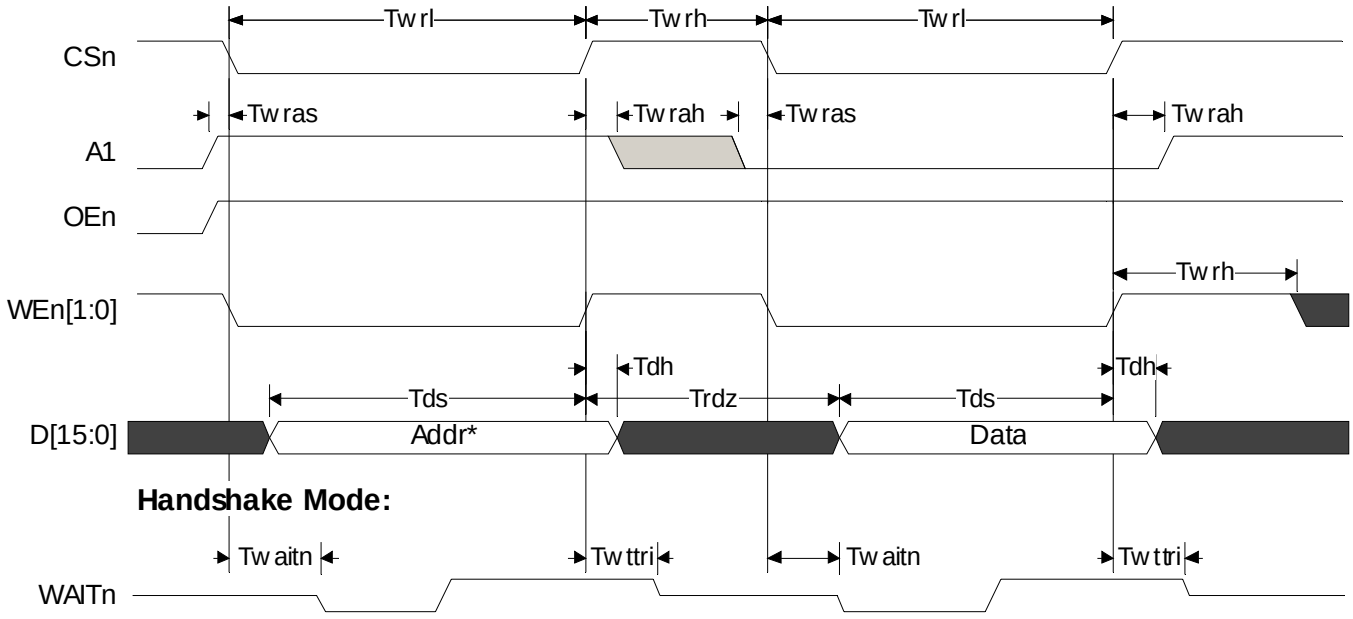
Note: There is no restriction on the page length.

Figure 3.49: Page-Mode Read, Type C 32bit Host Interface, Direct Addressing



Note: There is no restriction on page length.

Figure 3.50: Register Write, Type C Host Interface, Indirect Addressing

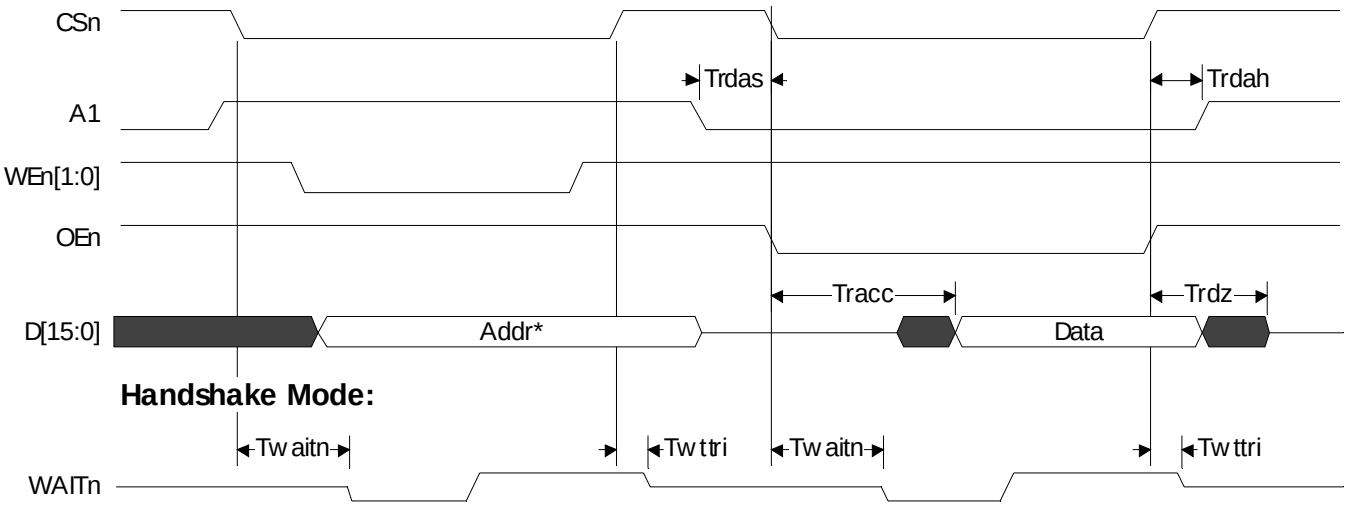


* See the following table for bit mappings.

Table 3.30 Register Write D[15:0] Bit Mapping for Addr* in Figure 3.50

Data Bus	Address Phase			
	16bit Host Bus	8bit Host Bus		
	Addr*	Addr*1	Addr*2	Addr*3
D[15]	x			
D[14]	x			
D[13]	A[12]			
D[12]	A[11]			
D[11]	A[10]			
D[10]	A[9]			
D[9]	A[8]			
D[8]	A[7]			
D[7]	A[6]	A[4]	A[9]	x
D[6]	A[5]	A[3]	A[8]	x
D[5]	A[4]	A[2]	A[7]	A[12]
D[4]	A[3]	A[1]	A[6]	A[11]
D[3]	A[2]	A[0]	A[5]	A[10]
D[2]	A[1]	0	1	0
D[1]	x	0	0	1
D[0]	1	1	1	1

Figure 3.51: Register Read Operation, Type C Host Interface, Indirect Addressing

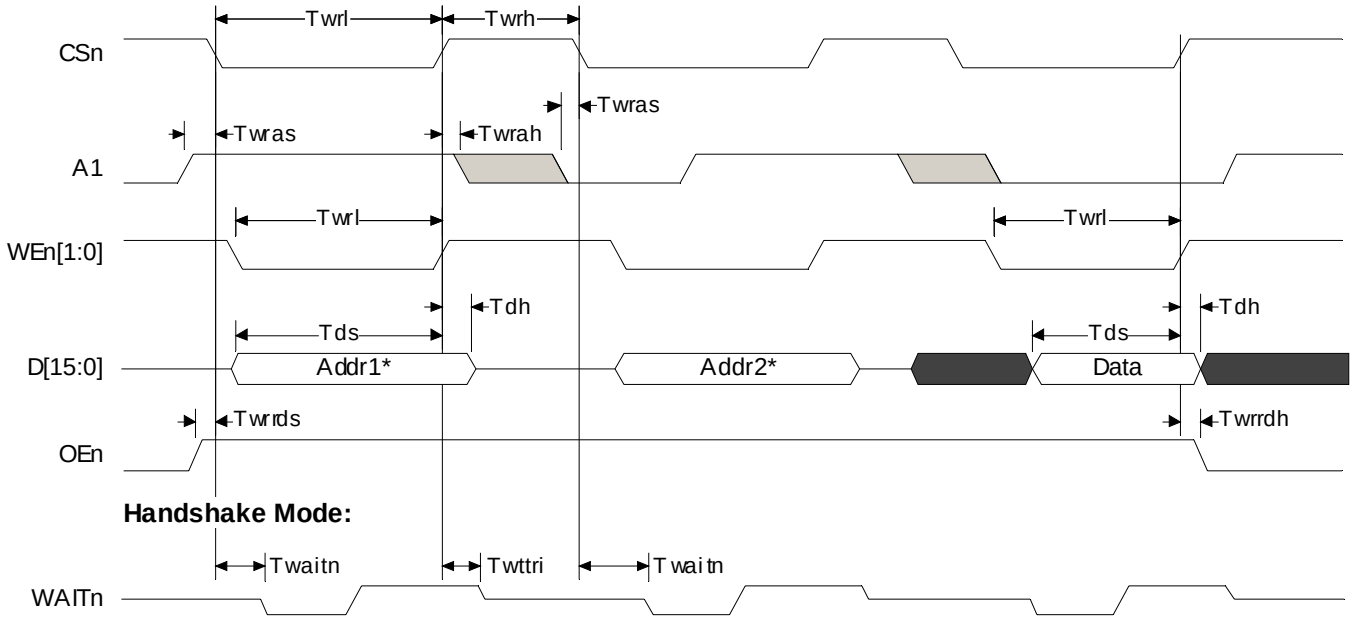


* See the following table for bit mappings.

Table 3.31 Register Read D[15:0] Bit Mapping for Addr* in Figure 3.54

Data Bus	Address Phase			
	16bit Host Bus	8bit Host Bus		
	Addr*	Addr*1	Addr*2	Addr*3
D[15]	x			
D[14]	x			
D[13]	A[12]			
D[12]	A[11]			
D[11]	A[10]			
D[10]	A[9]			
D[9]	A[8]			
D[8]	A[7]			
D[7]	A[6]	A[4]	A[9]	x
D[6]	A[5]	A[3]	A[8]	x
D[5]	A[4]	A[2]	A[7]	A[12]
D[4]	A[3]	A[1]	A[6]	A[11]
D[3]	A[2]	A[0]	A[5]	A[10]
D[2]	A[1]	0	1	0
D[1]	x	0	0	1
D[0]	1	1	1	1

Figure 3.52: Memory Write, Type C Host Interface, Indirect Addressing

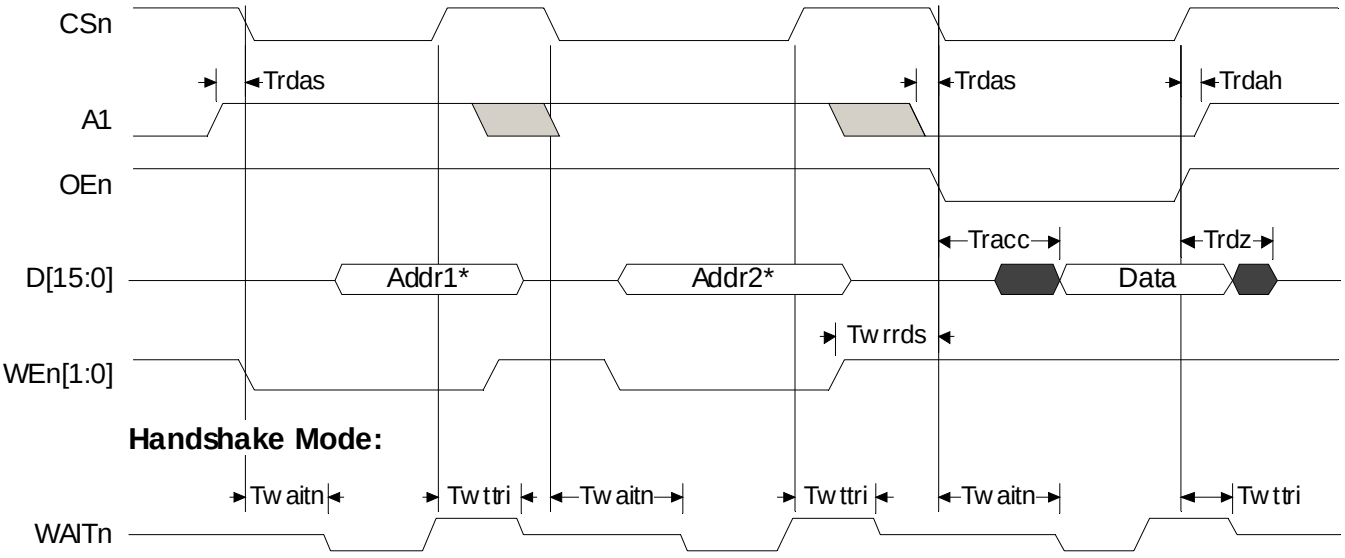


* See the following table for bit mappings.

Table 3.32 Memory Write D[15:0] Bit Mapping for Addr1* and Addr2* in Figure 3.52

Data Bus	Address Phase					
	16bit Host Bus		8bit Host Bus			
	Addr1	Addr2	Addr1	Addr2	Addr3	Addr4
D[15]	A[14]	x				
D[14]	A[13]	x				
D[13]	A[12]	x				
D[12]	A[11]	x				
D[11]	A[10]	x				
D[10]	A[9]	x				
D[9]	A[8]	x				
D[8]	A[7]	x				
D[7]	A[6]	x	A[4]	A[9]	A[14]	A[19]
D[6]	A[5]	A[19]	A[3]	A[8]	A[13]	A[18]
D[5]	A[4]	A[18]	A[2]	A[7]	A[12]	A[17]
D[4]	A[3]	A[17]	A[1]	A[6]	A[11]	A[16]
D[3]	A[2]	A[16]	A[0]	A[5]	A[10]	A[15]
D[2]	A[1]	A[15]	0	1	0	1
D[1]	0	1	0	0	1	1
D[0]	0	0	0	0	0	0

Figure 3.53: Memory Read, Type C Host Interface, Indirect Addressing

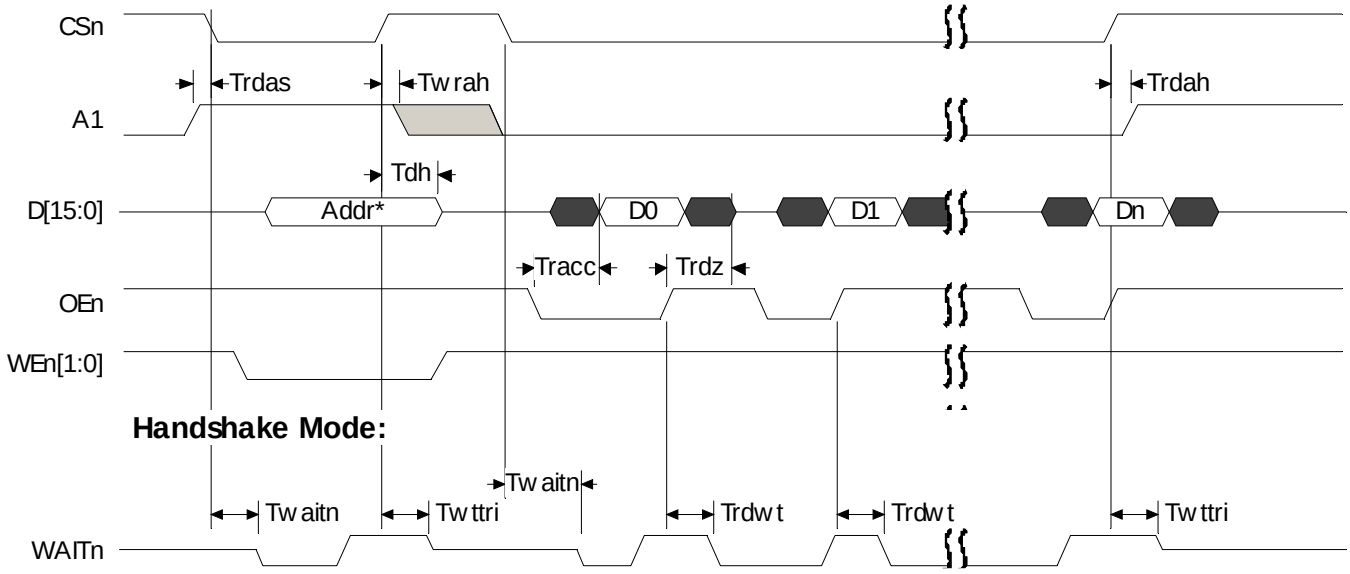


* See the following table for bit mappings.

Table 3.33 Memory Read D[15:0] Bit Mapping for Addr1* and Addr2* in Figure 3.53

Data Bus	Address Phase					
	16bit Host Bus		8bit Host Bus			
	Addr1	Addr2	Addr1	Addr2	Addr3	Addr4
D[15]	A[14]	x				
D[14]	A[13]	x				
D[13]	A[12]	x				
D[12]	A[11]	x				
D[11]	A[10]	x				
D[10]	A[9]	x				
D[9]	A[8]	x				
D[8]	A[7]	x				
D[7]	A[6]	x	A[4]	A[9]	A[14]	A[19]
D[6]	A[5]	A[19]	A[3]	A[8]	A[13]	A[18]
D[5]	A[4]	A[18]	A[2]	A[7]	A[12]	A[17]
D[4]	A[3]	A[17]	A[1]	A[6]	A[11]	A[16]
D[3]	A[2]	A[16]	A[0]	A[5]	A[10]	A[15]
D[2]	A[1]	A[15]	0	1	0	1
D[1]	0	1	0	0	1	1
D[0]	0	0	0	0	0	0

Figure 3.54: Register Burst Read, Type C Host Interface, Indirect Addressing



* See the following table for bit mappings.

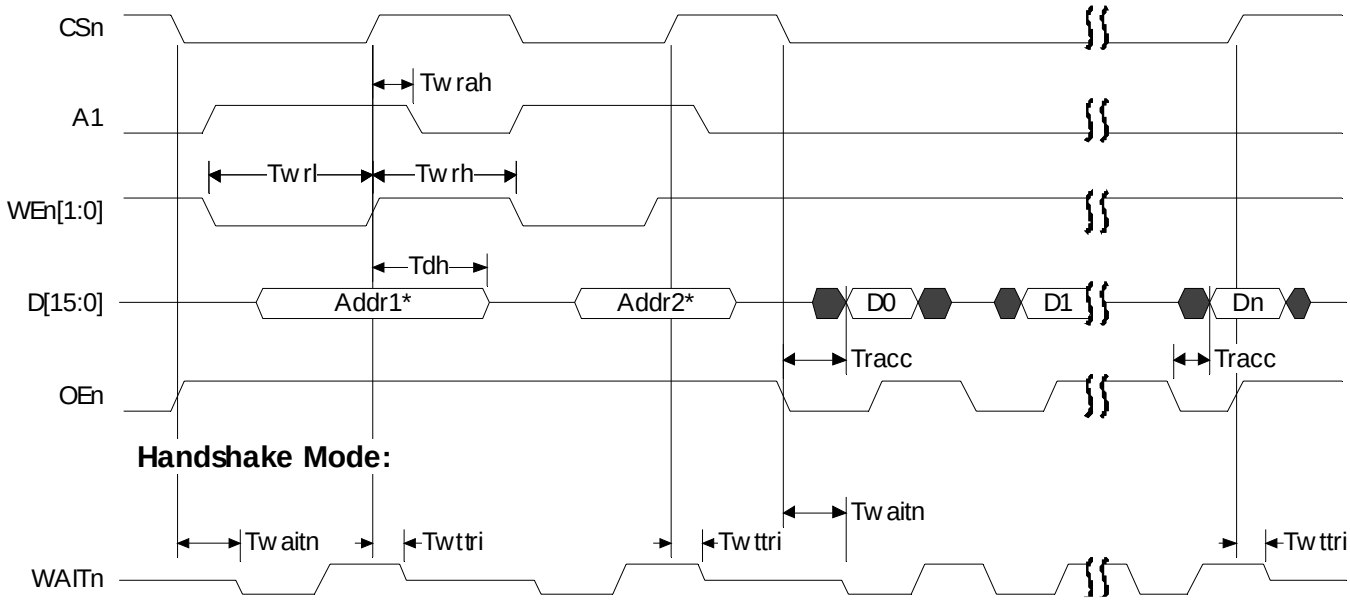
Table 3.34 Register Read D[15:0] Bit Mapping for Addr* in Figure 3.54

Data Bus	Address Phase			
	16bit Host Bus	8bit Host Bus		
	Addr*	Addr*1	Addr*2	Addr*3
D[15]	x			
D[14]	x			
D[13]	A[12]			
D[12]	A[11]			
D[11]	A[10]			
D[10]	A[9]			
D[9]	A[8]			
D[8]	A[7]			
D[7]	A[6]	A[4]	A[9]	x
D[6]	A[5]	A[3]	A[8]	x
D[5]	A[4]	A[2]	A[7]	A[12]
D[4]	A[3]	A[1]	A[6]	A[11]
D[3]	A[2]	A[0]	A[5]	A[10]
D[2]	A[1]	0	1	0
D[1]	x	0	0	1
D[0]	1	1	1	1

Note: Tie WRn low.

Note: To perform Burst Read operations as shown in Figure 3.54 set DC01[8] = 1.

Figure 3.55: Memory Burst Read, Type C Host Interface, Indirect Addressing



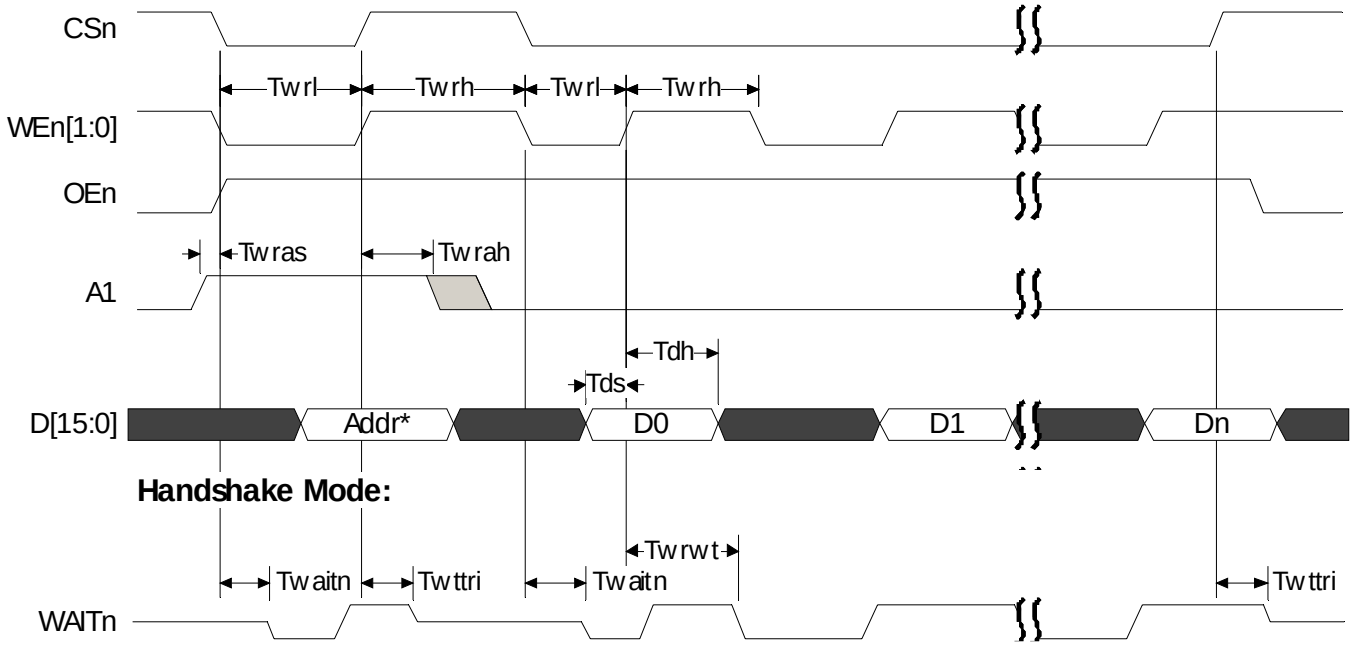
* See the following table for bit mappings.

Table 3.35 Memory Read D[15:0] Bit Mapping for Addr1* and Addr2* in Figure 3.55

Data Bus	Address Phase					
	16bit Host Bus		8bit Host Bus			
	Addr1	Addr2	Addr1	Addr2	Addr3	Addr4
D[15]	A[14]	x				
D[14]	A[13]	x				
D[13]	A[12]	x				
D[12]	A[11]	x				
D[11]	A[10]	x				
D[10]	A[9]	x				
D[9]	A[8]	x				
D[8]	A[7]	x				
D[7]	A[6]	x	A[4]	A[9]	A[14]	A[19]
D[6]	A[5]	A[19]	A[3]	A[8]	A[13]	A[18]
D[5]	A[4]	A[18]	A[2]	A[7]	A[12]	A[17]
D[4]	A[3]	A[17]	A[1]	A[6]	A[11]	A[16]
D[3]	A[2]	A[16]	A[0]	A[5]	A[10]	A[15]
D[2]	A[1]	A[15]	0	1	0	1
D[1]	0	1	0	0	1	1
D[0]	0	0	0	0	0	0

Note: To perform Burst Read operations as shown in Figure 3.55 set DC01[8] = 1.

Figure 3.56: Register Burst Write, Type C Host Interface, Indirect Addressing



* See the following table for bit mappings.

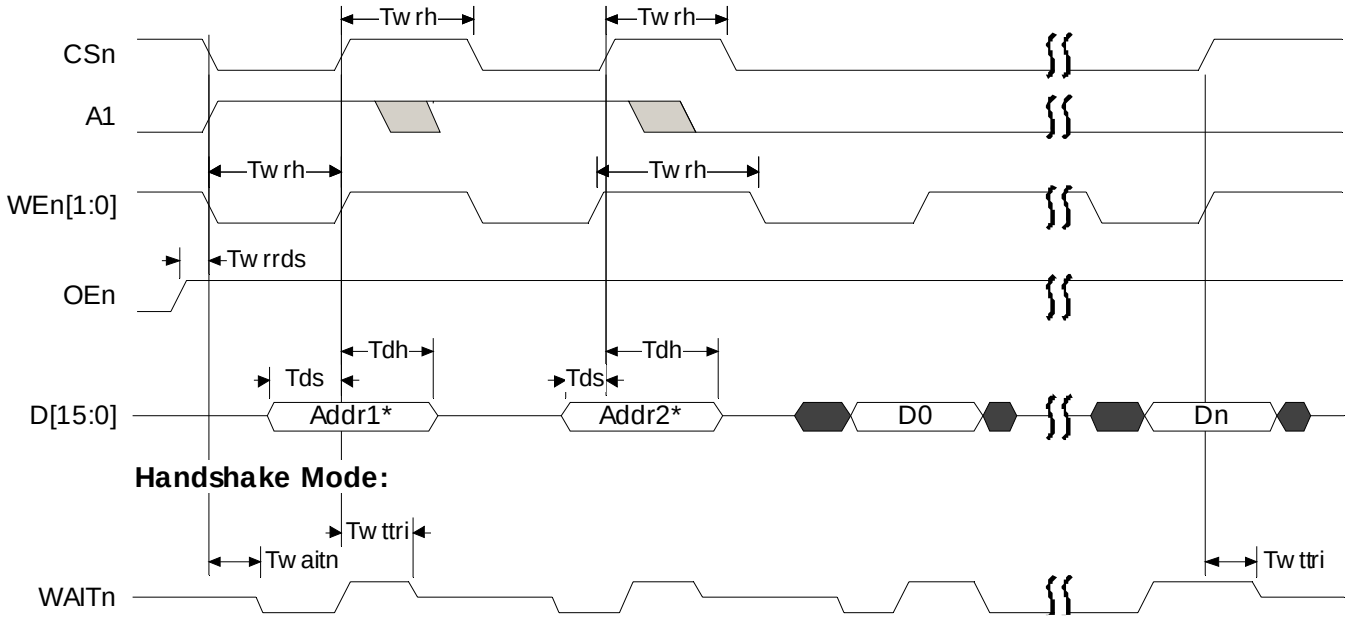
Table 3.36 Register Write D[15:0] Bit Mapping for Addr* in Figure 3.56

Data Bus	Address Phase			
	16bit Host Bus	8bit Host Bus		
	Addr*	Addr*1	Addr*2	Addr*3
D[15]	x			
D[14]	x			
D[13]	A[12]			
D[12]	A[11]			
D[11]	A[10]			
D[10]	A[9]			
D[9]	A[8]			
D[8]	A[7]			
D[7]	A[6]	A[4]	A[9]	x
D[6]	A[5]	A[3]	A[8]	x
D[5]	A[4]	A[2]	A[7]	A[12]
D[4]	A[3]	A[1]	A[6]	A[11]
D[3]	A[2]	A[0]	A[5]	A[10]
D[2]	A[1]	0	1	0
D[1]	x	0	0	1
D[0]	1	1	1	1

Note: Tie WRn low.

Note: To perform Burst Write operations as shown in Figure 3.56 set DC01[9] = 1.

Figure 3.57: Memory Burst Write, Type C Host Interface, Indirect Addressing



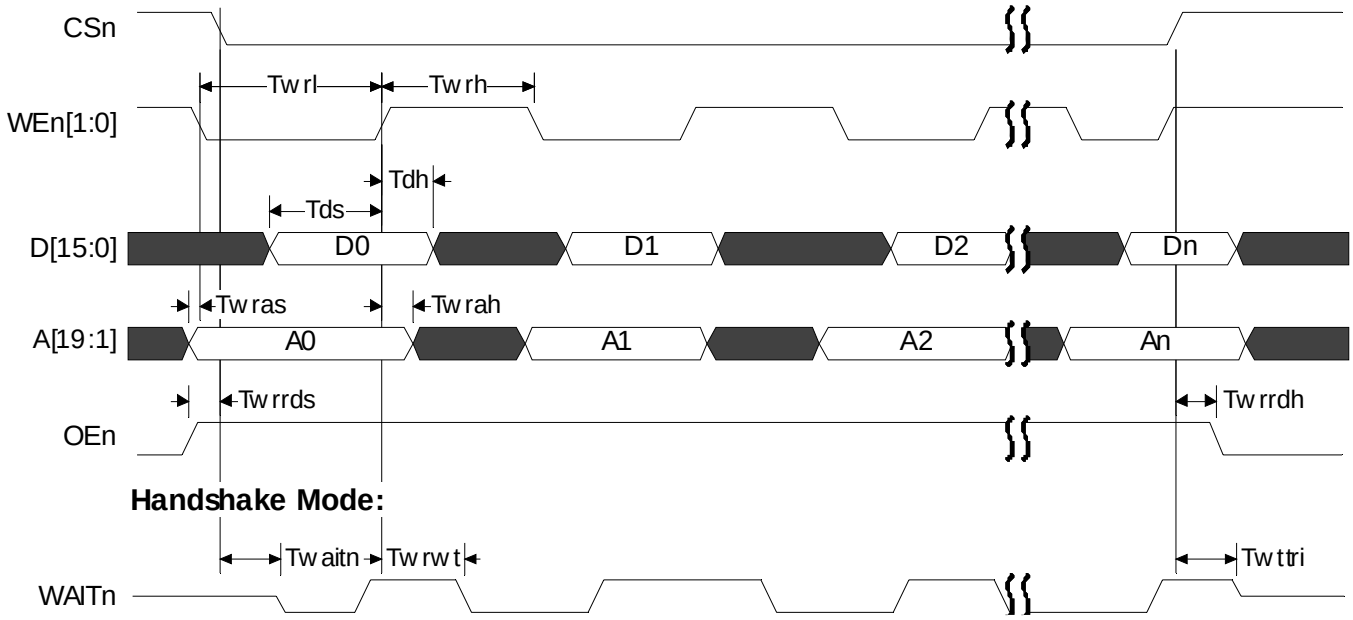
* See the following table for bit mappings.

Table 3.37 Memory Write D[15:0] Bit Mapping for Addr1* and Addr2* in Figure 3.57

Data Bus	Address Phase					
	16bit Host Bus		8bit Host Bus			
	Addr1	Addr2	Addr1	Addr2	Addr3	Addr4
D[15]	A[14]	x				
D[14]	A[13]	x				
D[13]	A[12]	x				
D[12]	A[11]	x				
D[11]	A[10]	x				
D[10]	A[9]	x				
D[9]	A[8]	x				
D[8]	A[7]	x				
D[7]	A[6]	x	A[4]	A[9]	A[14]	A[19]
D[6]	A[5]	A[19]	A[3]	A[8]	A[13]	A[18]
D[5]	A[4]	A[18]	A[2]	A[7]	A[12]	A[17]
D[4]	A[3]	A[17]	A[1]	A[6]	A[11]	A[16]
D[3]	A[2]	A[16]	A[0]	A[5]	A[10]	A[15]
D[2]	A[1]	A[15]	0	1	0	1
D[1]	0	1	0	0	1	1
D[0]	0	0	0	0	0	0

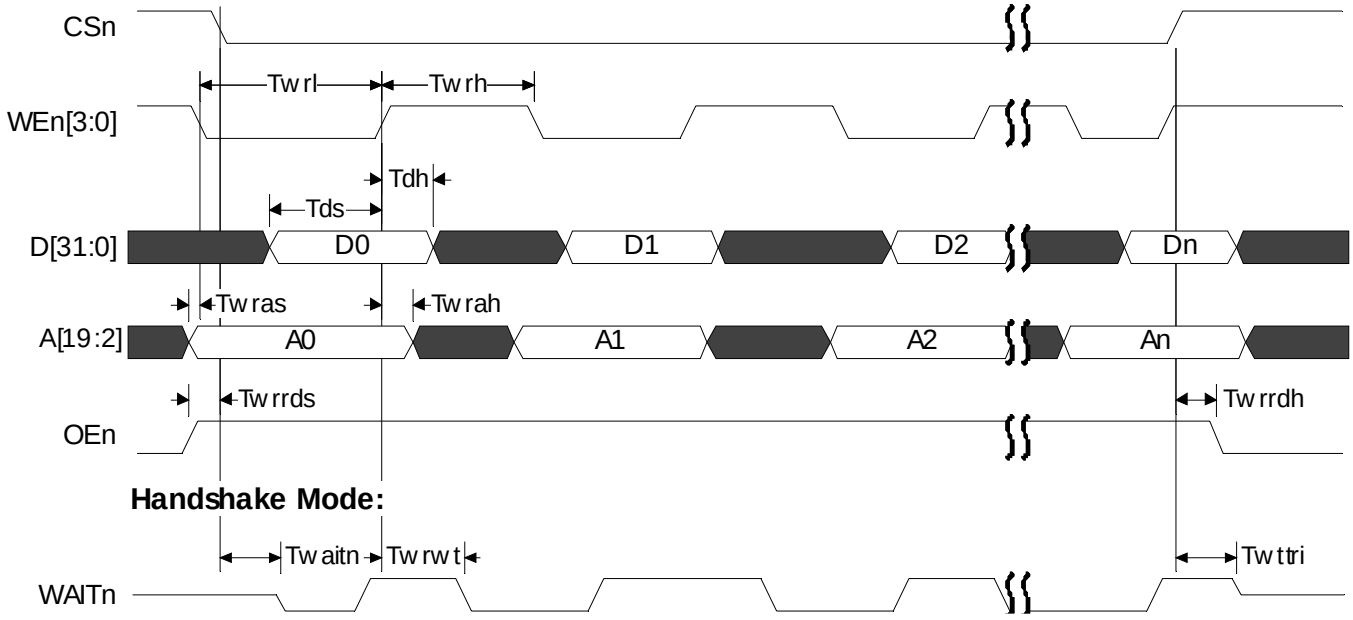
Note: Tie WRn low. To perform Burst Write operations as shown in Figure 3.54, set DC01[9] = 1

Figure 3.58: Register/Memory Burst Write, Type C Host 8bit and 16bit Interface, Direct Addressing



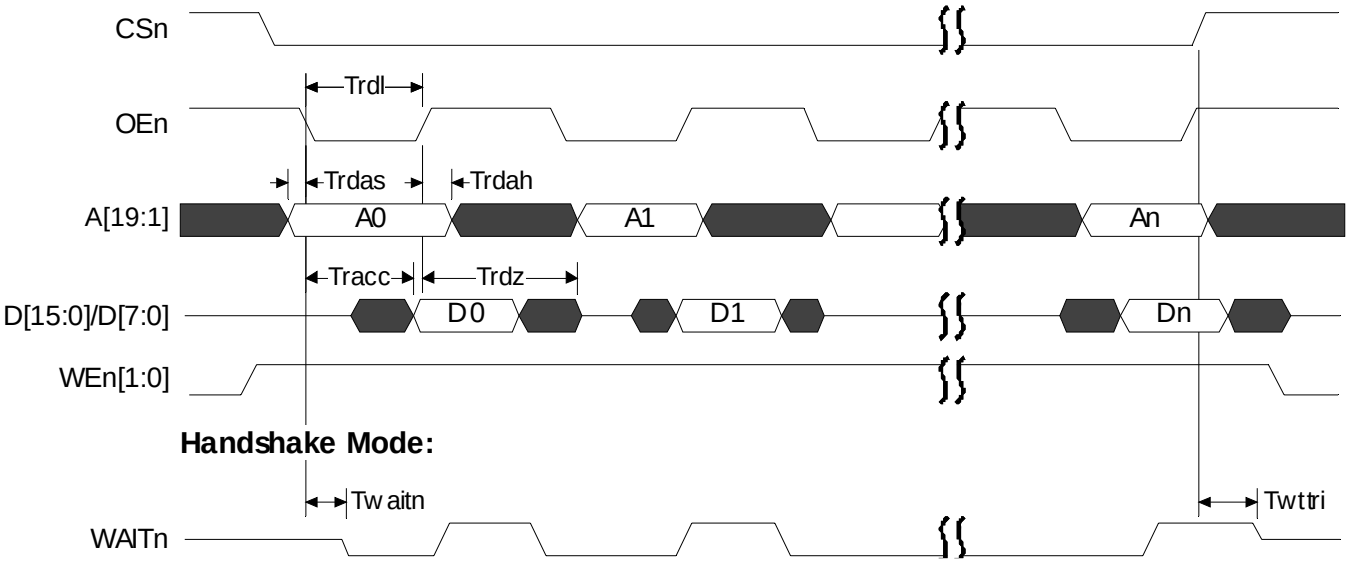
Note: Tie WRn low.

Figure 3.59: Register/Memory Burst Write, Type C Host 32bit Interface, Direct Addressing



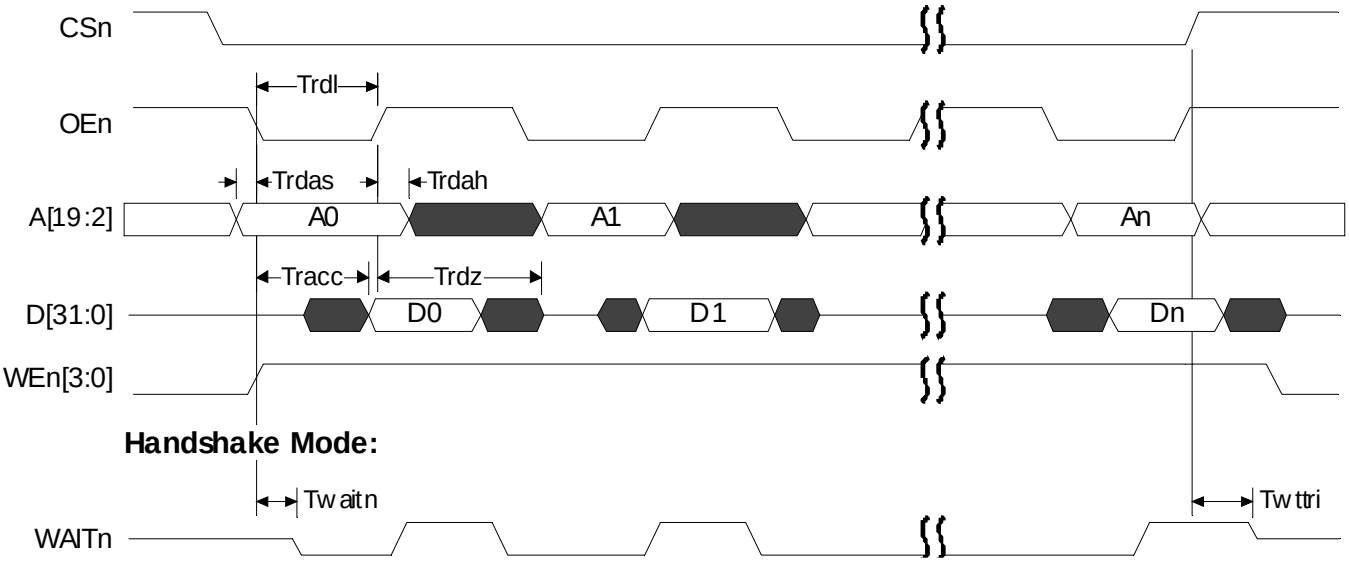
Note: Tie WRn low.

Figure 3.60: Register/Memory Burst Read, Type C 8bit and 16bit Host Interface, Direct Addressing



Note: Tie WRn low.

Figure 3.61: Register Memory Burst Read, Type C 32bit Host Interface, Direct Addressing



Note: Tie WRn low.

3.4.4.6 Type C Host Interface Timing Parameters

Table3.39 provides the AC timing parameters for the preceding Type C-style host interface timing diagrams in Figure 3.40 through Figure 3.61.

Note: TM is the memory clock period in ns. TF is the FIFO clock period.

Table 3.38 Type C Host Interface Timing Parameters

Symbol	Description	Min (ns): Time and Conditions		Max (ns): Time and Conditions	
Tdh	**Write cycles:** Data hold time from rising edge of CSn	0		N/A	
Tds	**Write cycles:** Data setup time to rising edge of CSn.	20		N/A	
Tracc	**Read cycles:** Maximum read access time from the beginning of the read cycle to the first valid data access.	N/A		**2.4 V < BVDD ≤ 3.6 V**	
				4*TM + 35	Memory
				2.5*TF + 30	FIFO Status Registers
				47	Register and JPEG Read DMA FIFO
				1.7 V ≤ BVDD < 2.4	
				4*TM + 50	Memory
				2.5*TF + 50	FIFO Status Registers
				69	Register and JPEG Read DMA FIFO
Trdah	**Read cycles:** Address hold time from rising edge of CSn or WEn, whichever comes first.	0		N/A	
Trdas	**Read cycles:** Address setup time to falling edge of CSn or WEn, whichever comes last.	0		N/A	
Trdh	**Read cycles:** Read enable Inactive time measured from the end of one read cycle to the beginning of the next read cycle.	5	No handshake	N/A	
		26	Handshake		
Trdhpg	**Data Hold Time in page mode read**	N/A		7	
Trdl	**Write cycles:** Read enable active low time. CSn-controlled write cycles:CSn low time OEn-controlled write cycles:OEn low time	**2.4 V < BVDD ≤ 3.6 V**		N/A	
		4*TM + 35	Memory		
		47	Register and JPEG Read DMA FIFO		
		1.7 V ≤ BVDD < 2.4			
		4*TM + 50	Memory		
		69	Register and JPEG Read DMA FIFO		
Trdwt	Time from rising edge of OEn to falling edge of WAITn	N/A		**2.4 V < BVDD ≤ 3.6 V**	
				17	Memory
				31	Register
				1.7 V ≤ BVDD < 2.4	
				27	Memory
				42	Register
Trdz	Time from rising edge of CSn to data bus floating state	6		15	

Symbol	Description	Min (ns): Time and Conditions		Max (ns): Time and Conditions	
Trpacc	**Page Mode access:** Maximum read access time *following* the first access of a page.	N/A		**2.4 V < BVDD ≤ 3.6 V**	
				30	Memory
				32	Register and JPEG Read DMA FIFO
				1.7 V ≤ BVDD < 2.4	
				45	Memory
				45	Register and JPEG Read DMA FIFO
Twaitn	WAITn/RDYn assertion time from the falling edge of CSn.	N/A		**2.4 V < BVDD ≤ 3.6 V** 17	
				1.7 V ≤ BVDD < 2.4 40	
Twrah	**Write cycles:** Address hold time from the rising edge of CSn or WEn, whichever comes first.	0		N/A	
Twras	**Write cycles:** Address setup time from the edge of CSn or WEn, whichever comes first.	0		N/A	
Twrcyc	**Write cycle time requirement:** Time from the beginning of one write cycle to the beginning of the next write cycle.	$T_{wrl} + T_{wrH}$ **OR** 1.5*Tm + 4 (Whichever is longer)		N/A	
Twrh	**Write Enable Inactive Time:** Time from the end of one write cycle to the beginning of the next write cycle	10	No handshake	N/A	
		26	Handshake		
Twrl	**Write Enable Active time:** CSn-controlled write cycle: CSn active time WRn-controlled write cycle: WRn active time	**2.4 V < BVDD ≤ 3.6 V** 30		N/A	
		1.7 V ≤ BVDD < 2.4 45			
Twrrdh	**WEn Assertion time** Immediately after a read cycle: Time from CSn rising edge to WEn falling edge	5	No handshake	N/A	
		26	Handshake		
	OEn Assertion time Immediately following a write cycle: Time from CSn rising edge to OEn falling edge	5	No handshake		
		26	Handshake		
Twrrds	**Time for OEn to be de-asserted** Before a write cycle: Time from rising edge of OEn to falling edge of CSn for write cycles	5	No handshake	N/A	
		26	Handshake		
	Time for WEn to be de-asserted Before a read cycle: Time from rising edge of WEn to falling edge of CSn for read cycles	5	No handshake		
		26	Handshake		
Twttri	Time from rising edge of CSn to beginning of tri-state condition of WAITn	N/A		29	

3.4.5 Flat Panel Interface

Figure 3.62: Flat Panel Output Timing

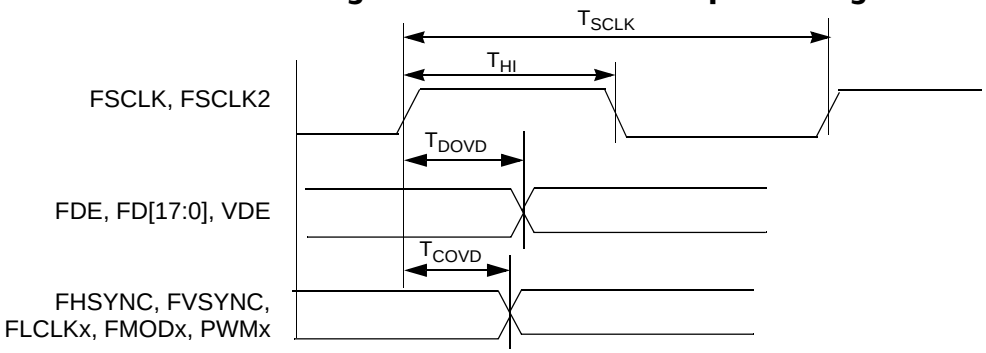


Table 3.39: AC Timing Characteristics - Panel Output Timing

Symbol	Parameter	Min	Max	Units
T_{SCLK}	Shift clock cycle time, CPU Interface	20	-	ns
	Shift clock cycle time, Direct Parallel Interface	125	-	ns
T_{DOVD}	Data signals output valid time	–3	4	ns
T_{COVD}	Control signals output valid time	–3	3	ns
T_{HI}/T_{SCLK}	Shift clock duty cycle	40	60	%

Note: AC Timing is specified with output loading = 25 pF.

3.4.6 Video Input Interface

Figure 3.63: Video Parallel Input Clock Timing

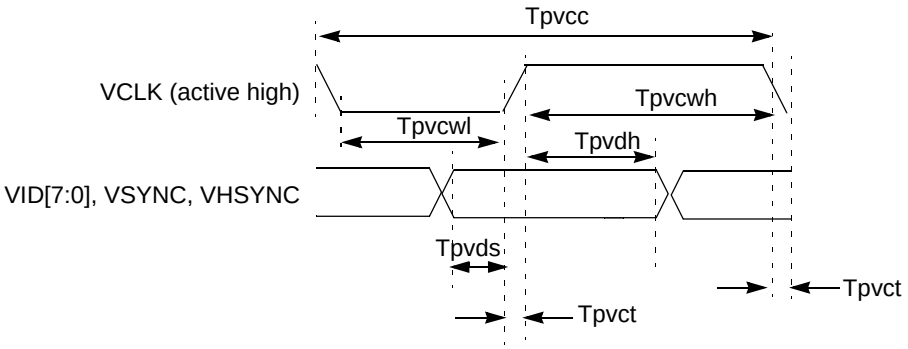


Table 3.40: Video Parallel Input Clock Timing

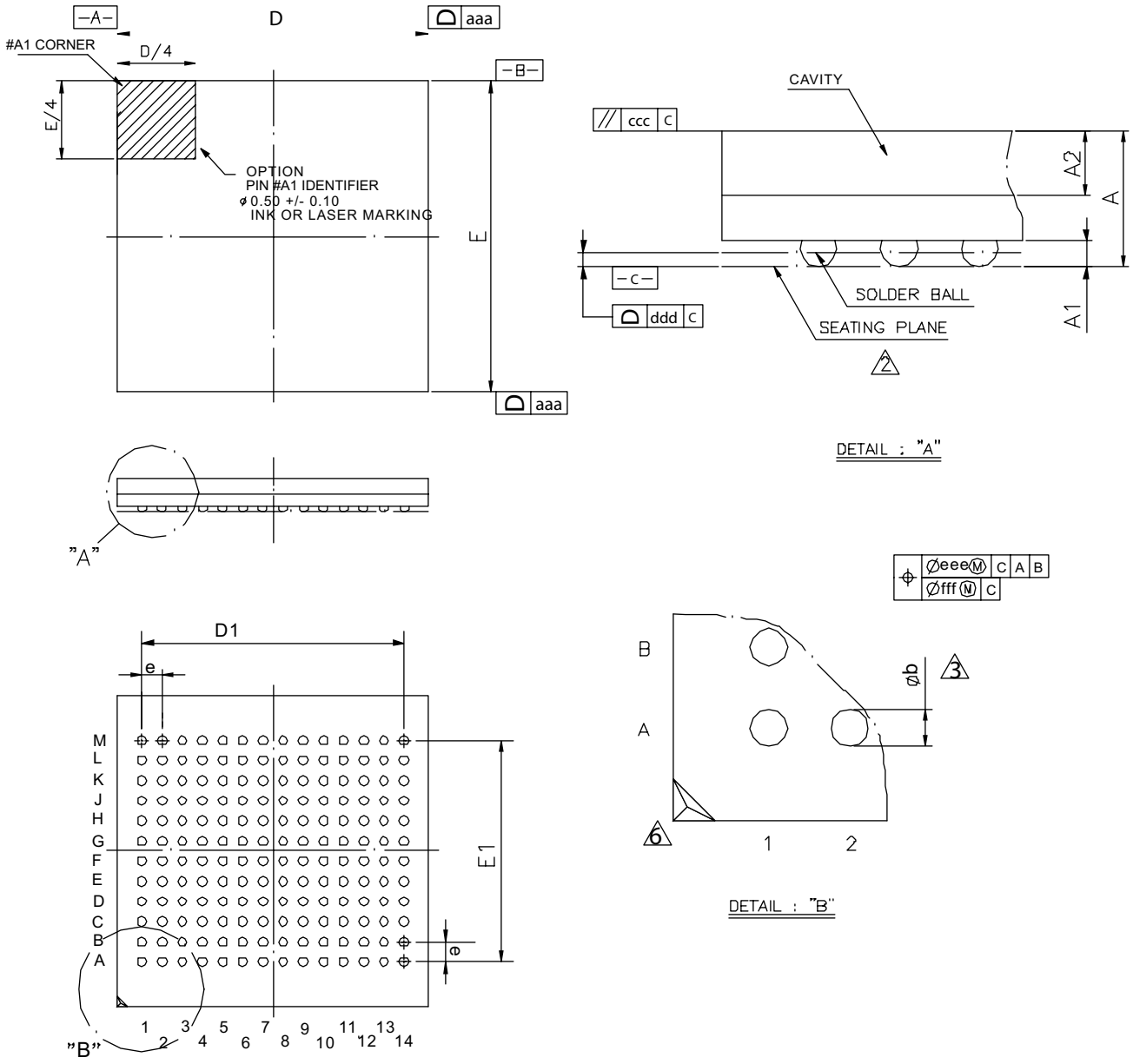
Symbol	Parameter	Rev: A or B	Min	Max	Unit
T_{pvcc}	VCLK cycle time	Rev B	13.8	–	ns
		Rev A	18.5	–	
T_{pvcwl}	VCLK low pulse width	Rev B	4.5	–	ns
		Rev A	6	–	
T_{PVCWH}	VCLK high pulse width	Rev B	7.7	–	ns
		Rev A	10.5	–	
T_{pvds}	VID[7:0] data setup time		5	–	ns
T_{pvdh}	VID[7:0] data hold time		4	–	ns
T_{PVCT}	VCLK Rise/fall transition time		-	**	ns

** T_{PVCT} can have any period as long as the remaining Video Parallel Input Clock setup and hold times are within the NVIDIA specifications given here.

3.5 Package Specifications

3.5.1 Mechanical Drawings

Figure 3.64: GoForce 4000 10 x 10 mm Package Mechanical Drawing



NOTE:

1. CONTROLLING DIMENSIONS: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.50mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERENCE DOCUMENT: JEDEC MO-207.
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
7. DRAWING NOT TO SCALE.

Table 3.41 Symbol and Dimension Call Outs

Symbol	DImension in mm			DImension in inches		
	MIN	Nominal	MAX	MIN	Nominal	MAX
A	1.10	1.15	1.20	0.043	0.045	0.047
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.40	0.45	0.50	0.019	0.018	0.020
ϕ b (diameter b)	0.25	0.30	0.35	0.010	0.012	0.014
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D1	8.45 BASIC			0.333 BASIC		
E1	7.15 BASIC			0.281 BASIC		
e	0.65 BASIC			0.026 BASIC		
aaa	0.15			0.006		
ccc	0.20			0.008		
ddd	0.10			0.004		
eee	0.15			0.006		
fff	0.10			0.004		
MD/ME*	14/12					
Total Number of Balls: 168						

* MD/ME = (Number of balls in row)/(number of balls in column)

Note:

Parameters for aaa, bbb, ccc, ddd, eee, and fff are measured according to JEDEC specification MO-207. The diameters of eee and fff are specified for worst case material conditions, with respect to datum C. The diameter of eee is also measured with respect to datums A and B.

3.5.2 Ball Map

The GoForce 4000 package is a 10 x 10 mm 168-pin chip-scale BGA package. It is ball-compatible with the GoForce 3000 (which is in a 8 x 10 mm package). Relative to GoForce 3000, GoForce 4000 contains an additional row of 14 balls on one edge of the package. Figure 3.65 shows the GoForce 4000 ball map. Differences with GoForce 3000 are shaded in red.

Figure 3.65: GoForce 4000 Ball Map

TOP VIEW
168 Pin Array

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	A17	A16	A11	A9	MD1	A19	VVSYNC	VGP2	VGP0	VD0	VHSYNC	VGP4	VGP3	VGP1	A
B	A15	A14	A18	A7	BGP0	BEn3	VID7	VID5	VID3	VID1	VID6	VID4	VID2	VCLK	B
C	A12	A10	A13	A5	MD2	TRST	TMS	TD0	FCLK1	FCLK0	ENVEE	ENCTL	ENVDD	VVDD	C
D	A6	A4	A8	A3	BVDD	CVDD	TCK	TDI	FD13	FVSYNC	FMOD0	FVDD	FFCLK	FHSYNC	D
E	OSCFI	A1	A2	BVDD	CVDD	MD0	GND	GND	CVDD	FD9	FDE	FD1	FD0	FSCLK	E
F	OSCFO	OSCR	RDYn	BEn1	CVDD	GND	GND	GND	CVDD	FD7	FD5	FD4	FD2	FD3	F
G	INTRn	WRn	D14	BEn0	CVDD	GND	GND	GND	FD15	FD11	FD6	FD12	FD8	FD10	G
H	D9	D5	D3	RDn	PORn	GND	SDD1	FGP0	FGP2	FGP5	FD14	FVDD	FD16	FD17	H
J	D7	D1	D6	D15	CSn	SDVDD	SDD3	SDCLK	SDD2	FGP7	FGP9	FMOD1	FGP3	FGP1	J
K	D0	D4	D8	D13	D22	GND	D27	SDD0	SDCMD	SDGP1	FGP11	FGP4	FGP8	FGP6	K
L	D12	D2	D10	D11	D21	D24	D26	D29	D31	SDGP0	FGP12	FGP10	FGP13	FGP14	L
M	D16	D17	D18	D19	D20	D23	D25	D28	D30	BVDD	NC	NC	NC	NC	M
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

3.5.2.1 Alphabetic Signal to Ball Mapping

Table 3.42 Alphabetic Signal to Ball Mapping

Signal Name	Ball #		Signal Name	Ball #		Signal Name	Ball #		Signal Name	Ball #
A1	E2		D9	H1		FD16	H13		NC	M11
A2	E3		D10	L3		FD17	H14		NC	M12
A3	D4		D11	L4		FDE	E11		NC	M13
A4	D2		D12	L1		FFCLK	D13		NC	M14
A5	C4		D13	K4		FGP0	H8		OSCFI	E1
A6	D1		D14	G3		FGP1	J14		OSCFO	F1
A7	B4		D15	J4		FGP2	H9		OSCR	F2
A8	D3		D16	M1		FGP3	J13		PORn	H5
A9	A4		D17	M2		FGP4	K12		RDn	H4
A10	C2		D18	M3		FGP5	H10		RDYn	F3
A11	A3		D19	M4		FGP6	K14		SDCLK	J8
A12	C1		D20	M5		FGP7	J10		SDCMD	K9
A13	C3		D21	L5		FGP8	K13		SDD0	K8
A14	B2		D22	K5		FGP9	J11		SDD1	H7
A15	B1		D23	M6		FGP10	L12		SDD2	J9
A16	A2		D24	L6		FGP11	K11		SDD3	J7
A17	A1		D25	M7		FGP12	L11		SDGP0	L10
A18	B3		D26	L7		FGP13	L13		SDGP1	K10
A19	A6		D27	K7		FGP14	L14		SDVDD	J6
BEn0	G4		D28	M8		FHSYNC	D14		TCK	D7
BEn1	F4		D29	L8		FLCLK0	C10		TD0	C8
BEn3	B6		D30	M9		FLCLK1	C9		TD1	D8
BGP0	B5		D31	L9		FMOD0	D11		TMS	C7
BVDD	D5		ENCTL	C12		FMOD1	J12		TRST	C6
BVDD	E4		ENVDD	C13		FSCLK	E14		VCLK	B14
BVDD	M10		ENVEE	C11		FVDD	H12		VGP0	A9
CSn	J5		FD0	E13		FVDD	D12		VGP1	A14
CVDD	D6		FD1	E12		FVSYNC	D10		VGP2	A8
CVDD	E5		FD2	F13		GND	E7		VGP3	A13
CVDD	G5		FD3	F14		GND	E8		VGP4	A12
CVDD	F9		FD4	F12		GND	F6		VHSYNC	A11
CVDD	F5		FD5	F11		GND	F7		VID0	A10
CVDD	E9		FD6	G11		GND	F8		VID1	B10
D0	K1		FD7	F10		GND	G6		VID2	B13
D1	J2		FD8	G13		GND	G7		VID3	B9
D2	L2		FD9	E10		GND	G8		VID4	B12
D3	H3		FD10	G14		GND	H6		VID5	B8
D4	K2		FD11	G10		GND	K6		VID6	B11
D5	H2		FD12	G12		INTRn	G1		VID7	B7
D6	J3		FD13	D9		MD0	E6		VVDD	C14
D7	J1		FD14	H11		MD1	A5		VVSYNC	A7
D8	K3		FD15	G9		MD2	C5		WRn	G2

3.5.2.2 Alphabetic Ball to Signal Mapping

Table 3.43 Alphabetic Ball to Signal Mapping

Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name	Ball #	Signal Name
A1	A17	D1	A6	G1	INTRn	K1	D0
A2	A16	D2	A4	G2	WRn	K2	D4
A3	A11	D3	A8	G3	D14	K3	D8
A4	A9	D4	A3	G4	BEn0	K4	D13
A5	MD1	D5	BVDD	G5	CVDD	K5	D22
A6	A19	D6	CVDD	G6	GND	K6	GND
A7	VVSYNC	D7	TCK	G7	GND	K7	D27
A8	VGP2	D8	TD1	G8	GND	K8	SDD0
A9	VGP0	D9	FD13	G9	FD15	K9	SDCMD
A10	VID0	D10	FVSYNC	G10	FD11	K10	SDGP1
A11	VHSYNC	D11	FMOD0	G11	FD6	K11	FGP11
A12	VGP4	D12	FVDD	G12	FD12	K12	FGP4
A13	VGP3	D13	FFCLK	G13	FD8	K13	FGP8
A14	VGP1	D14	FHSYNC	G14	FD10	K14	FGP6
B1	A15	E1	OSCFI	H1	D9	L1	D12
B2	A14	E2	A1	H2	D5	L2	D2
B3	A18	E3	A2	H3	D3	L3	D10
B4	A7	E4	BVDD	H4	RDn	L4	D11
B5	BGP0	E5	CVDD	H5	PORn	L5	D21
B6	BEn3	E6	MD0	H6	GND	L6	D24
B7	VID7	E7	GND	H7	SDD1	L7	D26
B8	VID5	E8	GND	H8	FGP0	L8	D29
B9	VID3	E9	CVDD	H9	FGP2	L9	D31
B10	VID1	E10	FD9	H10	FGP5	L10	SDGP0
B11	VID6	E11	FDE	H11	FD14	L11	FGP12
B12	VID4	E12	FD1	H12	FVDD	L12	FGP10
B13	VID2	E13	FD0	H13	FD16	L13	FGP13
B14	VCLK	E14	FSCLK	H14	FD17	L14	FGP14
C1	A12	F1	OSCFO	J1	D7	M1	D16
C2	A10	F2	OSCR	J2	D1	M2	D17
C3	A13	F3	RDYn	J3	D6	M3	D18
C4	A5	F4	BEn1	J4	D15	M4	D19
C5	MD2	F5	CVDD	J5	CSn	M5	D20
C6	TRST	F6	GND	J6	SDVDD	M6	D23
C7	TMS	F7	GND	J7	SDD3	M7	D25
C8	TD0	F8	GND	J8	SDCLK	M8	D28
C9	FLCLK1	F9	CVDD	J9	SDD2	M9	D30
C10	FLCLK0	F10	FD7	J10	FGP7	M10	BVDD
C11	ENVEE	F11	FD5	J11	FGP9	M11	NC
C12	ENCTL	F12	FD4	J12	FMOD1	M12	NC
C13	ENVDD	F13	FD2	J13	FGP3	M13	NC
C14	VVDD	F14	FD3	J14	FGP1	M14	NC

3.6 Solder Reflow

The solder reflow profile in Figure 3.66 and the reflow profile parameters in Table 3.44 are based on JEDEC Standard J-STD-020B for Small Body components. Refer to the JEDEC specs for further details.

Figure 3.66: Solder Reflow Profile

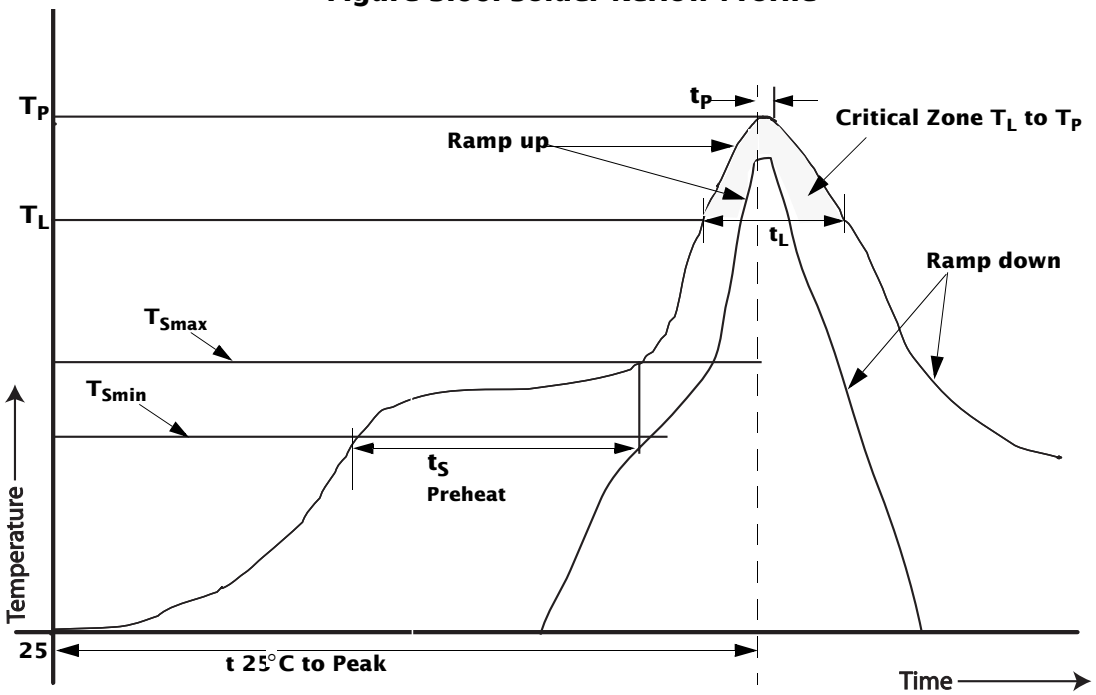


Table 3.44: Reflow Profile Parameters

Profile Feature	Sn-Pb Eutectic Assembly	Pb-free Assembly
Average ramp-up rate	3 °C/second maximum	3 °C/second maximum
Preheat - Temperature Min (T_{Smin}) - Temperature Max (T_{Smax}) - Time (min to max) (ts)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
T_{Smax} to TL - Ramp-up rate	 N/A	 3 °C/second max
Time maintained above: - Temperature (T_L) - Time (t_L)	 183 °C 60 - 150 seconds	 217 °C 60 - 150 seconds
Peak Temperature (T_P)	240 + 0/-5 °C	250 + 0/-5 °C
Time within 5C of actual Peak Temperature (t_P)	10 - 30 seconds	20 - 40 seconds
Ramp-down Rate	6 °C/second max.	6 °C/second max.
Time from 25C to Peak Temperature	6 minutes max.	8 minutes max.

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