GoForce 4000 Silicon

ERRATA

This document covers silicon errata for NVIDIA® GoForce™ 4000 Rev A01, Rev B02, Rev B03, and Rev B04. Each revision is given as a heading above a table containing its errata (issues.) Issues in this errata document are either addressed by a workaround action, a change to the next silicon revision, or a change in a future product. If the status for a given revision of silicon does not state that it will be fixed in a specific silicon revision, continue using the workaround for future silicon revisions. For example, if you have rev A0x silicon and its issue will be fixed in rev A0(x+1), use the workaround for rev A0x silicon product.

Summary of Errata

Silicon Revision	Issue		Workaround	Status
A01	#1	SD Response Buffer	Yes	Fixed in B02
	#2	MPEG-4 Decoder Coefficient FIFO	Yes	Use workaround
	#3	MPEG-4 Encoder Reset	Yes	Fixed in B02
	#4	Type C Host Interface Byte Enable	Yes	Fixed in B02
	#5	MPEG-4 Encoder VLC Overflow	Yes	Fixed in B02, with workaround
	#6	MPEG-4 Decoder Hang	Yes	Use Workaround
	#7	Operation of Force Reset Function	Yes	Use Workaround
B02	#1	PLL and Relaxation Oscillator[1]	Yes	Fixed in B03
	#2	Operation of Force Reset Function	Yes	Use Workaround
	#3	Power-on Sequence may affect internal memory repair logic when voltage SDVDD is below 3.0 V.[2]	No	N/A [1]
B03	#1	Corruption in JPEG-encoded frames originating in GC.[3]	No	Fixed in B04

	#2	Power-on Sequence may affect internal memory repair logic when voltage SDVDD is below 3.0 V.[2]	No	N/A [1]
B04	#1	Power-on Sequence may affect internal memory repair logic when voltage SDVDD is below 3.0 V.	Yes	Use Workaround

1. Version v04 of this document incorrectly showed one bug for silicon revision B02. This document's version v03 correctly showed bugs #1 and #2 for silicon version B02. In version v04 the listing of bug #1 was unintentionally dropped, and the omission was not caught. It has been added back into this document version.

2. The bug which shows as item #3 in B02 and item #2 in B03 was not recorded in earlier revisions of this errata document because it was not discovered until silicon revision B04. The Issue was discovered during the testing of a new GoForce driver release, concurrent to B04 silicon.

3. B03 was a silicon revision which was never used in production.

Device ID

Register DC13 contains the Device ID:

[23:20]: Major Revision ID: (full layer change)

[19:16]: Minor Revision ID: (metal)

[15:0]: 4500h = Rev B; 2300h = Rev A

GoForce 4000 Revision A01 Silicon Errata

The following issues existed in the A01 revision of GoForce 4000 silicon. System hardware and software designers should be aware of these and take appropriate action when using this version of the GoForce 4000.

Issue:

#1	**SD Response Buffer**	
	Description:	SD response buffer pointer is incremented at the end of every read access. This is correct with a 32 bit host interface. However, it is not correct with 8 and 16 bit host interfaces. The pointer should be incremented at the end of every other host read with 16 bit host interface; at the end of every four reads with 8 bit host interface.
	Workaround:	Read the lower 16 bits of every filled location of the response buffer, reset the response buffer, and then read the upper 16 bits of the same locations. The similar work around can be applied to 8-bit host interfaces.
	Status:	Fixed in revision B02.
#2	**MPEG-4 Decoder Coefficient FIFO**	
	Description:	The MPEG-4 decoder coefficient FIFO contains 32 entries, due to the full/empty logic counter, it can only handle up to 8 write synchronizations if read and write ratios are not the same. When the MPEG-4 decoder clock divider is at certain ratios, this can cause the full/empty signal to be incorrect causing corruption.
	Workaround:	Do not divide MPEG-4 decoder clock. The MPEG-4 decoder clock frequency can be derived from the PLL if it is required to operate at a high clock rate. Keep the MPEG decoder clock divider to '1' (i.e. DC19[7:4] must be set to '0000'b]. Another work around requires SW to poll the FIFO status and make sure not to write more than 8 back to back writes into the FIFO.
	Status:	Use the work around above.
#3	**MPEG-4 Encoder Reset**	
	Description:	The MPEG-4 encoder does not have a software reset.
	Workaround:	Need to power-down the entire chip to reset the MPEG-4 encoder
	Status:	Fixed in B02. Added two levels of reset as follows: ME00[0] resets the complete encoder module except the registers. ME00[1] resets the entire encoder, the VLC DMA and the clock generation module.

#4	**Type C Host Interface Byte Enable**	
	Description:	Internal memory byte enable generation is not correct with Type-C host interface if BEns are asserted earlier than CSn.
	Workaround:	Assert BEn later than CSn.
	Status:	Fixed in revision B02.
#5	**MPEG-4 Encoder VLC Overflow**	
	Description:	This is encountered when the VLC DMA buffer overflow condition is true from the start of a frame. In this case, the VLC DMA read state machine incorrectly interprets the linked list as two middle chunk entries instead of a first chunk of frame entry. If the bits in timestamp[31:17] are zero, this is recoverable, as the FIFO will contain 2 64 bit entries (ffffffff_fffffffe followed by fffffffe_00000000) followed by the correct header data in the FIFO. If the bits in timestamp[31:17] are non-zero, the overflow condition is non-recoverable as the VLC DMA write buffer status will become corrupted.
	Workaround:	Once the software detects a overflow (from the VLC READ DMA FIFO's Header), it should first read all the data (length indicated by the header). Then it should always compare the next 64-bit entry with the 0xffff_ffff_ffff_fffe. The next entry should be compared with the 0xfffffffe_00000000. If it matches then ignore these 2 64-bit entries and treat the next entry as the actual header. If it does not match then treat the first entry as the header.
	Status:	Fixed in B02. Use the following software workaround in conjunction with this fix: The header for the first chunk of a frame has a chunk length of 0 (implying overflow), the two 32-bit data following the time stamp should be thrown away. The next 32-bit data will be the next chunk header (this chunk header should be the header for the last chunk of the frame, with the overflow bit set).
#6	**MPEG-4 Decoder hang**	
	Description:	This is encountered when the coefficient FIFO becomes empty after the last coefficient is read out and the command FIFO becomes full with all the subsequent non-coded macroblocks. When this condition happens, the run length decode state machine freezes.
	Workaround:	Create a V block coded with dummy coefficients if all the blocks in the command FIFO are non-coded.
	Status:	Use the software work around.

#7 Operation of Force Reset Function: GC2A[3], GC2A[1], GCS2A[3], and GCS2A[1]

Description: This Force Reset function is enabled by writing a 1 to GC2A[1], GC2A[3], GCS2A[1], and GCS2A[3].

When enabled, the Force Reset function should allow the Send Frame logic to accept another Send Frame request, from the same requestor, before the frame has been sent to the Flat Panel Interface. (In other words, the request can be received while the requestor is still sending a frame from the previous Send Frame request.)

However, when Force Reset is enabled, the next Send Frame request can not be accepted until the previous Send Frame request process has completed sending a frame to the Flat Panel Interface.

Workaround: Program GC2A[1], GC2A[3], GCS2A[1], and GCS2A[3] to 0.

With GC2A[1] (for the Main Display) or GCS2A[1] (for the Alternate Display) set to 0, the next Cursor Send Frame request can be accepted as soon as the display gets into the cursor area.

With GC2A[3] (for the Main Display) or GCS2A[3] (for the Alternate Display) set to 0, a window-related Send Frame request, from the same source, can be accepted as soon as the display starts to send the data from the window area.

Setting any of the following bits to 1 enables Window A Send Frame: GC2A[7:4].

Window B send frame is enabled by setting any one of the following bits to 1, GC2A[11:8].

Status: Use the workaround.

GoForce 4000 Revisions B02, B03, and B04 Silicon Errata

The following issues exist in the above-mentioned revision of GoForce 4000 silicon. System hardware and software designers should be aware of these and take appropriate action.

Rev B02 Issues:

#1	**PLL and Relaxation Oscillator**	
	Description:	Excessive jitter occurs on clocks generated by the PLL and Relaxation Oscillator
	Workaround:	Will not affect chip functions.
	Status:	Will fix in next silicon revision.
#2	**Operation of Force Reset Function: GC2A[3], GC2A[1], GCS2A[3], and GCS2A[1]**	
	Description:	This Force Reset function is enabled by writing a 1 to GC2A[1], GC2A[3], GCS2A[1], and GCS2A[3]. When enabled, the Force Reset function should allow the Send Frame logic to accept another Send Frame request, from the same requestor, before the frame has been sent to the Flat Panel Interface. (In other words, the request can be received while the requestor is still sending a frame from the previous Send Frame request.) However, when Force Reset is enabled, the next Send Frame request can not be accepted until the previous Send Frame request process has completed sending a frame to the Flat Panel Interface.
	Workaround:	Program GC2A[1], GC2A[3], GCS2A[1], and GCS2A[3] to 0. With GC2A[1] (for the Main Display) or GCS2A[1] (for the Alternate Display) set to 0, the next Cursor Send Frame request can be accepted as soon as the display gets into the cursor area. With GC2A[3] (for the Main Display) or GCS2A[3] (for the Alternate Display) set to 0, a window-related Send Frame request, from the same source, can be accepted as soon as the display starts to send the data from the window area. Setting any of the following bits to 1 enables Window A Send Frame: GC2A[7:4]. Window B send frame is enabled by setting any one of the following bits to 1, GC2A[11:8].
	Status:	Use the workaround.
#3	**Power-on Sequence may affect internal memory repair logic when voltage SDVDD is below 3.0 V: Refer to Rev B04 Issues Bug #1.**	

Rev B03 Issue:

#1	**GC data going to be JPEG (continuous) encoded sometimes shows corruption.**	
	Description:	This happens more often when the clock source is the Relaxation Oscillator (ROSC,) but the behavior not related to the ROSC. Data going from the GC to the JPEG Encoder is difficult to sync, and so can be corrupted. This shows more often with the ROSC; the ROSC frequency has more variation than do the other clock frequencies.
	Workaround:	No workaround.
	Status:	Fixed in B04.
#2	**Power-on Sequence may affect internal memory repair logic when voltage SDVDD is below 3.0 V:** **Refer to Rev B04 Issues Bug #1.**	

Rev B04 Issue:

#1	**Power-on Sequence may affect internal memory repair logic when voltage SDVDD is below 3.3 V.**	
	Description:	The GoForce 4000 Rev B's memory system repair capability is based on poly-silicon fuses programmed after an ATE screening process. The repair logic block is powered by SDVDD; the SRAM repair port is powered by CVDD. The interface between these two is through a level shifter. Once the memory clock is enabled, the memory repair logic writes data through the level shifter to the SRAM repair port. When the appropriate data bit equals a value of one, the repair logic reassigns a column. However, the output of the level shifter may not be high enough to reach the required level.
	Workaround:	Change the reset sequence to a double reset sequence, as explained and illustrated in NVIDIA document DA-01992-001. Ensure SDVDD is equal to 2.7 V. After power is asserted, PORn is de-asserted, and the MIU source clock is running and stable, software must wait a minimum of 2 ms to re-assert PORn. After a minimum period of 100 µs, PORn can be de-asserted, the MIU clock can be restarted, and software must wait a minimum of 2 ms before accessing the internal memory.
	Status:	Use the workaround.