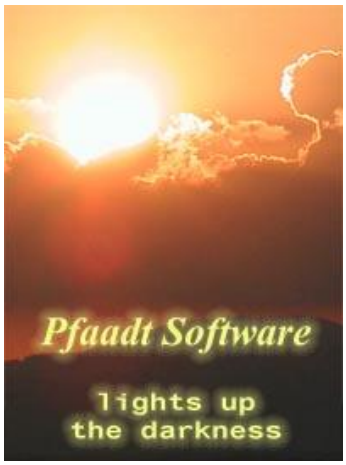


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Embedded Software, Windows CE.NET,
BIOS Adaptations, Driver Development,
Realtime Programming, Applications

User Documentation for the

PXA27x Configuration Utility

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Revision: 1.0

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1. Introduction

The PXA270 is a very powerful, but complex embedded processor. Compared to its predecessor PXA255, a lot of new internal devices have been added and the number of configurable pins have drastically increased. Each pin typically provides a larger number of configuration options.

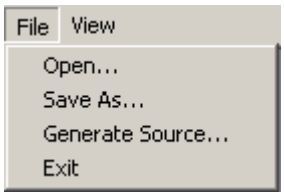
With its increased complexity, it has become much more difficult to fully understand and configure the chip. WindowsCE 5.0 contains a Board Support Package for the Mainstone II board. It consists of a boot loader that runs from ROM and initializes the hardware initially and device drivers to be included in WindowsCE.

To make adaptations easier we have designed a tool that allows you to make several configurations comfortably. The PXA270 configurator has been developed based on the following design goals:

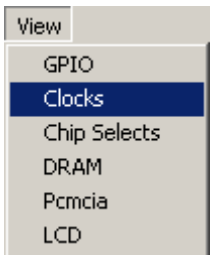
- Easy configuration of the GPIO pins
- Automatic Source Code generation for the GPIO pins for easy integration and maintenance
- Reverse Engineering of chipset registers for verification of board settings and comparison with other manufacturers
- Easy configuration of Timing Parameters with detailed output of selected clocks and times
- Support for user-specific LCD panels on the internal graphics controller

2. Working with the surface

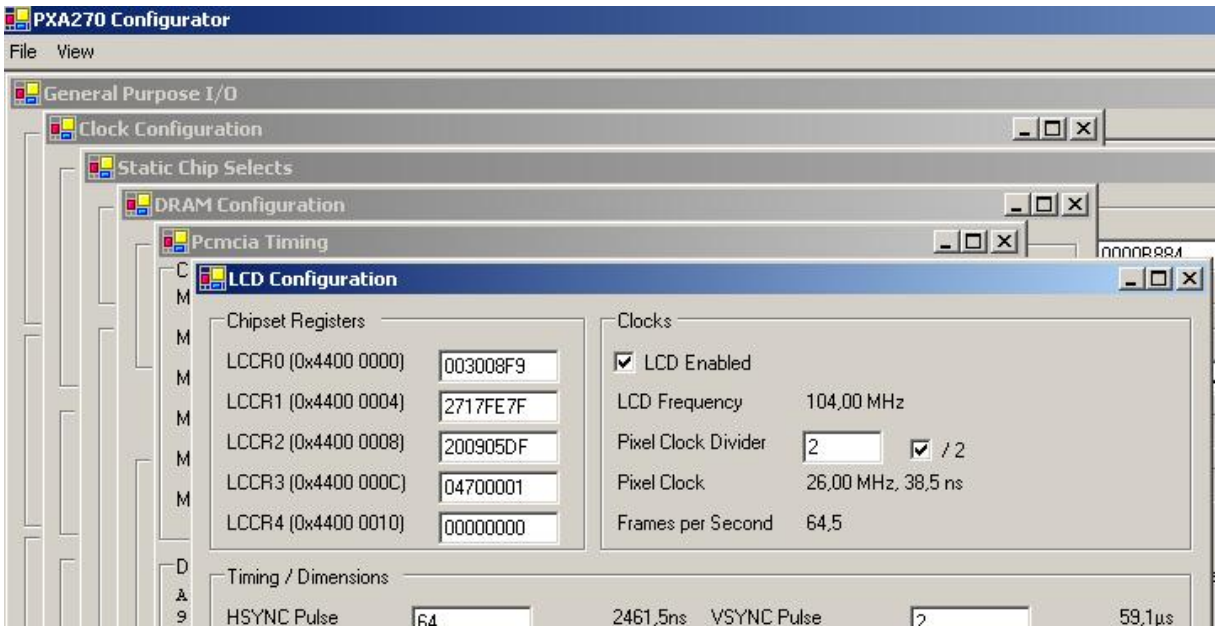
The PXA270 Configurator contains two menus, File and View. You can use the File menu to load or save a configuration, generate source codes that can later be included in your Platform Builder project or to Exit.



The View menu allows you to select between several configurators.



Each configurator can be opened one time only, but several different configurators can be opened at the same time.



3. General Purpose I/O

This tool makes the configuration of the PXA270's 121 gpio pins an easy task. On the left side you can see the chipset registers. Whenever you change one of these registers, the contents of the list will automatically reflect the new settings.

The chipset registers are divided into the following groups:

- Direction

  Defining a pin as an input or output.

- Level Set und Level Clear

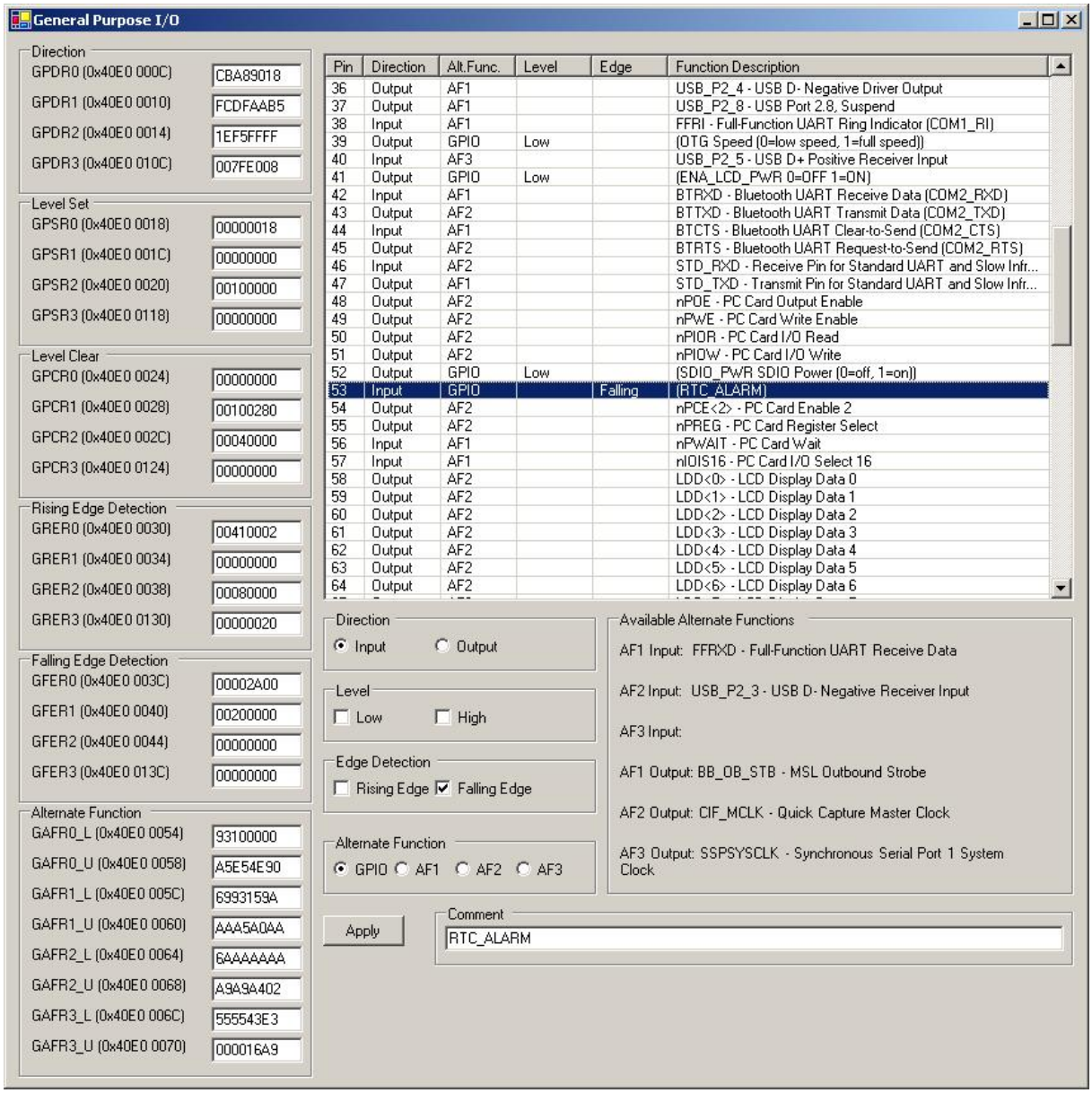
  Sets an output pin to a specific level. Setting and clearing a pin simultaneously is an invalid condition and results in unpredicted behaviour. The tool automatically warns by drawing the list entry in red color.

- Rising Edge Detection und Falling Edge Detection

  Whenever you want to use a gpio pin as an interrupt source, you must define whether the interrupt shall be sampled on the rising or falling edge of a signal. Since setting both rising and falling edge makes not much sense, the configurator warns you in such a case by marking the line red.

- Alternate Function

  Configure the pin for either gpio or an alternate function. This value is combined with the direction setting to achieve up to six different predefined alternate functions.



In the list you can see the configuration of the 121 different gpio pins. By clicking on an entry, the fields below the list are set according to the gpio's configuration. Besides the settings for Direction, Level, Edge Detection and Alternate Function, you can see a group "Available Alternate Functions". It displays all possible alternate functions for that pin. This may help you to configure the pins more easily.

In addition to that you can add a comment for each pin. The comment is displayed in brackets in the list as well as in the source codes that you may generate later.

By pressing the Apply button, your changes will be saved and the chipset registers and the list will be updated.

In the file menu, you can produce well documented source codes which you can include in your project. By doing modifications through the configurator only, your WindowsCE project remains open for future modifications to hardware variations.

Sample Output:

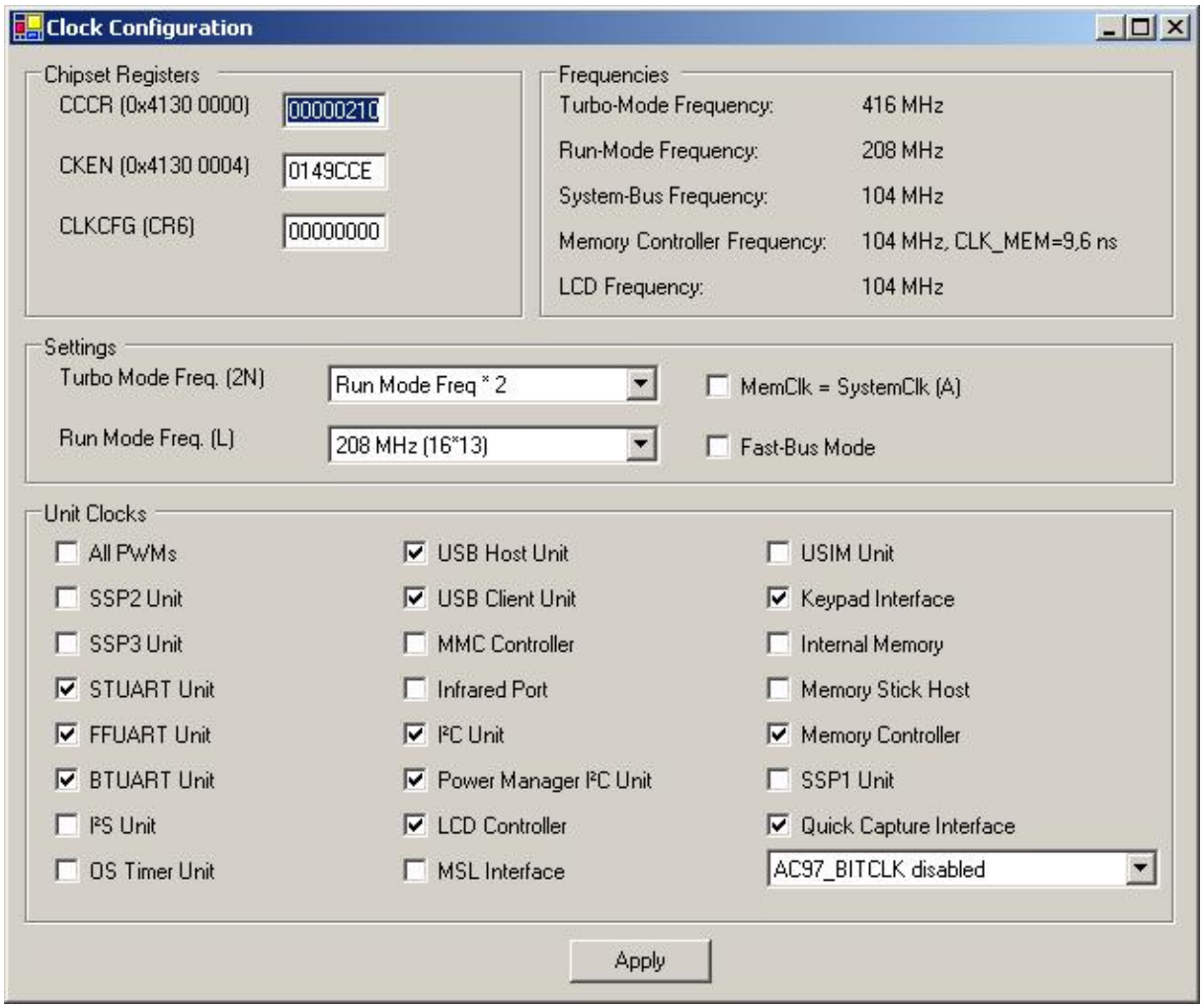
```
; GPIO 114: Output AF2   UVS0 - USIM Voltage Select 0
; GPIO 115: Output AF2   nUVS1 - USIM Voltage Select 1
; GPIO 116: Output AF2   nUVS2 - USIM Voltage Select 2
; GPIO 117: Output AF1   SCL - I²C Clock
; GPIO 118: Output AF1   SDA - I²C Data
; GPIO 119: Input  GPIO
; GPIO 120: Input  GPIO

; GPIO Direction
xlli_GPDR0_value    EQU  (0xCBA89018)
xlli_GPDR1_value    EQU  (0xFCDFAAB5)
xlli_GPDR2_value    EQU  (0x1EF5FFFF)
xlli_GPDR3_value    EQU  (0x007FE008)

; GPIO Set Register
xlli_GPSR0_value    EQU  (0x00000018)
```

4. Clock Settings

All clocks in PXA27x processors are based on its 13 MHz core clock. The Clock Configuration Register allows you to define other clocks by specifying a multiplier to the core clock. Derived clocks may be the run mode and turbo mode clock as well as the clocks for the memory controller and the LCD controller.

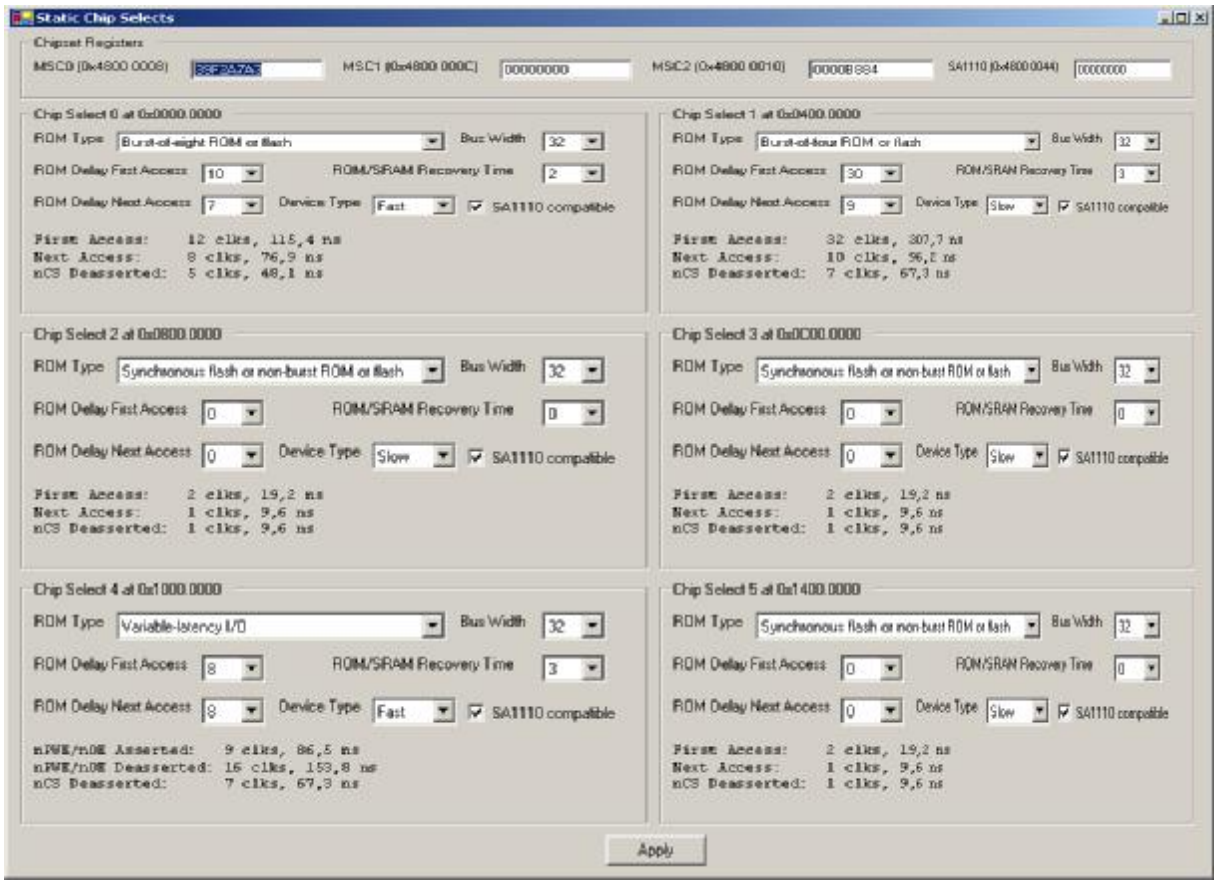


Clocks to several units can be turn on or off seperately. If you don't need a device, it is better to turn the clock off in order to save power.

This module is the basis for all timing calculations. Further clocks like e.g. the SDCLK for SDRAM's are derived by dividing the memory clock frequency by a specific value.

5. Static Chip Selects

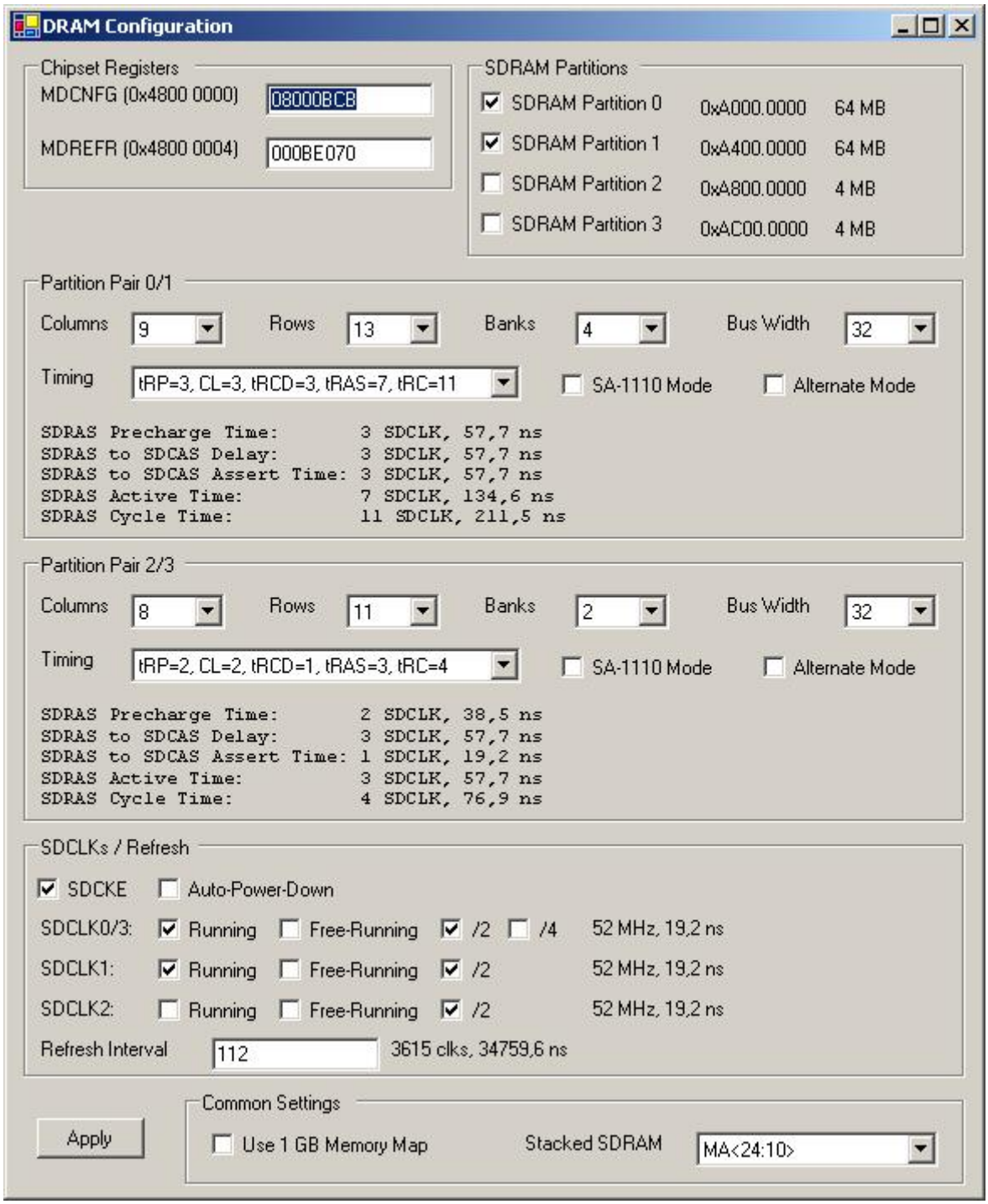
The PXA27x offers six static memory regions that can be configured individually for different types of memory. Memory Types can be Synchronous Flash, Burst-of-Four ROM, Burst-of-Eight ROM or VLIO.



Depending on the type of memory, the timing parameters have different meanings. The configuration tool displays the interpreted timings in clocks and nanoseconds.

6. DRAM

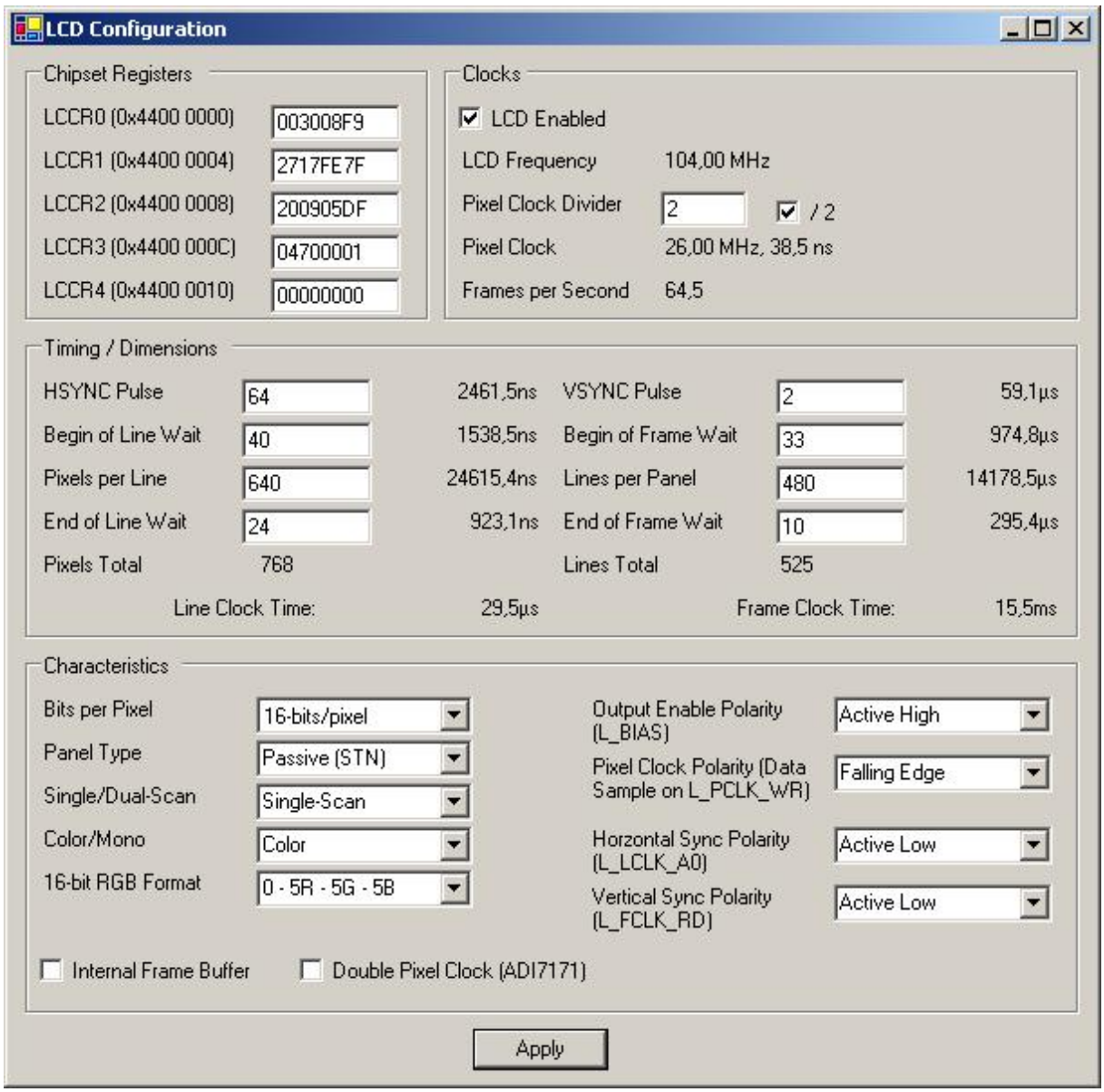
The DRAM configurator allows you to define the size and timing of the DRAM banks in the partition pairs 0 and 1. You can also define the SDCLK timing which is derived from the MEMCLK and the time between refresh cycles.



7. LCD

The LCD configurator simplifies the process of adding new panel types to the existing device driver for the internal graphics controller. A new panel type can be defined by

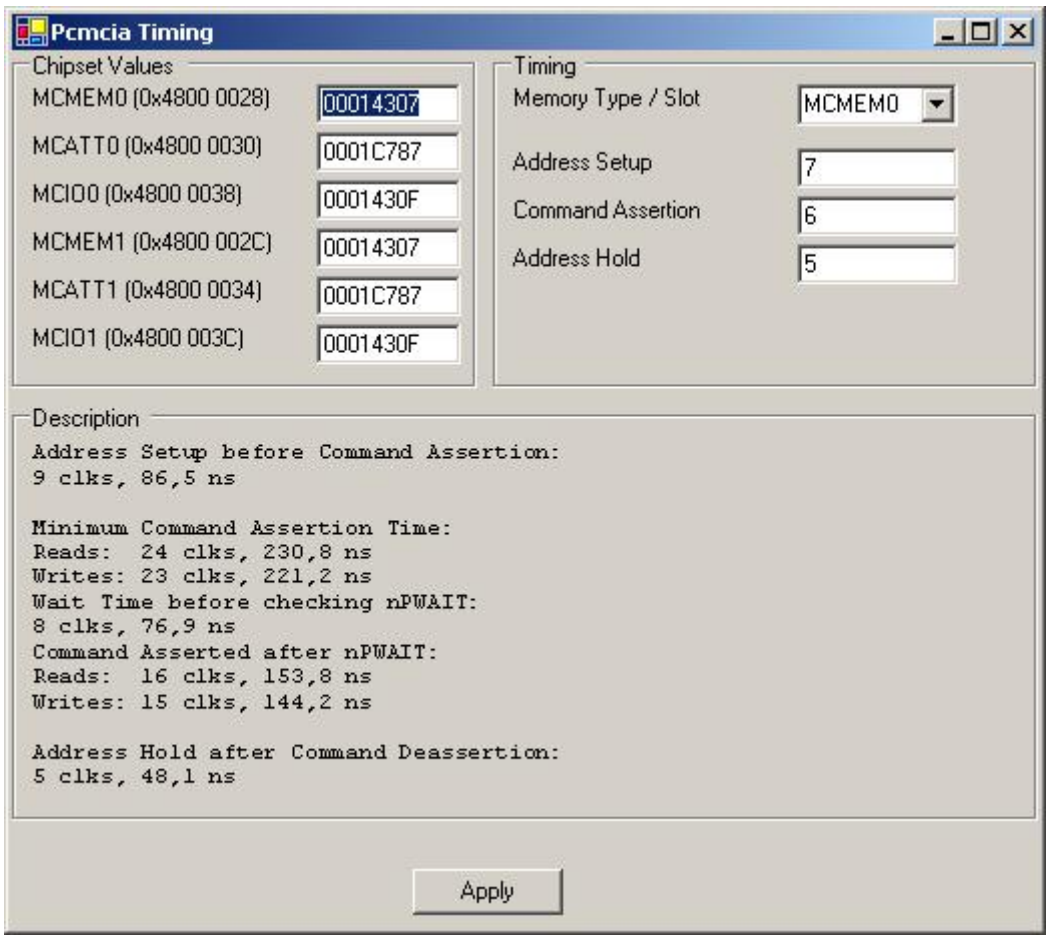
- Configuring an appropriate pixel clock frequency
- Setting the dimension of the display and the invisible regions
- Defining the panel's characteristics



The configurator automatically displays the number of pixel and line clocks and the time being used. The whole settings results in a screen refresh rate which should typically be around 60 frames/second.

8. PCMCIA

The PCMCIA dialog allows you to define the access timing for memory-, attribute- and I/O-regions for both slots. The bit fields and meanings are the same for all types of accesses. You can use the “Memory Type / Slot” combo box to switch between the different regions. The timing is shown in the Description groupbox.



The timing for the PCMCIA controller will initially be set up in the bootloader to allow for downloads from PCMCIA network cards during development. When WindowsCE gets started, the PCMCIA driver will initialize these registers again.

The timing values can be found in
public\common\oak\csp\arm\intel\px27x\xllp\inc\xlli_mainstone_defs.inc