M-Systems
Flash Disk Pioneers

DiskOnChip

DiskOnChip G3 Low Power (LP) 64MB (512Mb)

Flash Disk with 1.8V Core and I/O

Preliminary Data Sheet, September 2004

Highlights

M-Systems' DiskOnChip G3 LP is the industry's first, on-board Multi-Level Cell (MLC) NAND flash disk that is optimized with a 1.8V core and I/O to reduce power consumption both in operating and deep power-down modes. DiskOnChip G3 LP offers further benefits by implementing Toshiba's 0.13 micron MLC NAND flash technology and x2 technology from M-Systems, making it one of the industry's most efficient storage solutions. .

MLC NAND flash technology provides the smallest die size by storing 2 bits of information in a single memory cell. x2 technology enables MLC NAND to achieve highly reliable, high-performance data and code storage with a specially designed error detection and correction mechanism, optimized file management, and proprietary algorithms for enhanced performance.

DiskOnChip G3 LP includes a boot block that can replace expensive NOR flash, and incorporates both the flash array and an embedded thin controller in a single die.

DiskOnChip G3 LP provides:

- Flash disk for both code and data storage
- Low voltage: 1.65V~1.95V Core and I/O
- Hardware protection and security-enabling features
- High capacity single die 64MB (512Mb)
- Device cascade capacity: up to 256MB (2Gb)
- Enhanced Programmable Boot Block enabling eXecute In Place (XIP) functionality using 16-bit interface
- Small form factor:
  85-ball FBGA 7x10 mm package
- Enhanced performance by implementation of:
  - Multi-plane operation
  - DMA support
- Unrivaled data integrity with a robust Error Detection Code/Error Correction Code (EDC/ECC) tailored for MLC NAND flash technology
- Maximized flash endurance with TrueFFS® 6.2 (and higher)
- Support for major operating systems (OSs), including Symbian OS, Pocket PC 2002/3, Smartphone 2002/3, Palm OS, Nucleus, Linux, Windows CE, ThreadX, VxWorks, and more.
- Compatible with major Mobile smartphone and feature phone CPUs, including
  TI OMAP, XScale, Motorola MX,
  ADI 652x, Infineon EGold and SGold,
  TI DM270,TI Calypso, Freescale i.250, and
  Qualcomm MSMxxxx

Performance

- Erase: 30 MB/sec
- Sustained read: 5 MB/sec
- Sustained write: 1.1 MB/sec
- Access time: 52 nsec

Protection & Security-Enabling Features

- 16-byte Unique Identification (UID) number
- 6KByte user-controlled One Time Programmable (OTP) area
- Two configurable hardware-protected partitions for data and code:
  - Read-only mode
  - Write-only mode
  - One-Time Write mode (ROM-like) partition
  - Protection key and LOCK# signal
  - Sticky Lock (SLOCK) to lock boot partition
  - Protected Bad Block Table
- Support TI OMAP secure boot

Reliability and Data Integrity

- Hardware- and software-driven, on-the-fly EDC and ECC algorithms
- 4-bit Error Detection Code/Error Correction Code (EDC/ECC), based on a patented combination of BCH and Hamming code algorithms, tailored for MLC NAND flash technology
- Guaranteed data integrity after power failure
- Transparent bad-block management
- Dynamic and static wear-leveling

Boot Capability

- Programmable Boot Block with XIP capability to replace boot NOR
  - 2KB for 512Mb (64MB) devices
- Download Engine (DE) for automatic download of boot code from Programmable Boot Block
- Boot options:
  - CPU initialization
  - Platform initialization
  - OS boot
- Asynchronous Boot mode to boot from ARM-based CPUs, e.g. XScale, TI OMAP, Motorola MX without the need for external glue logic
- Exceptional boot performance with DMA support enhanced by external clock
- Virtual and Paged RAM boot modes.

Hardware Compatibility

- Configurable interface: simple NOR-like or multiplexed address/data interface
- CPU compatibility, including:
  - ARM-based CPUs
  - Texas Instruments OMAP
  - Intel StrongARM/XScale
  - Motorola MX family
  - Emblaze ER4525
  - Renesas SH mobile
  - Qualcomm MSMxxxx
  - AMD Alchemy
  - Motorola PowerPC™ MPC8xx
  - Philips PR31700
  - Hitachi SuperH™ SH-x
  - NEC VR Series
- Supports 8-, 16- and 32-bit architectures

Note: Refer to application note AP-DOC-0704, *Improving DiskOnChip Performance*, for more information about DiskOnChip performance parameters.

TrueFFS® Software

- Full hard-disk read/write emulation for transparent file system management
- Patented TrueFFS
  - Flash file system management
  - Automatic block management
  - Data management to maximize the limit of typical flash life expectancy
  - Dynamic virtual mapping
- Dynamic and static wear-leveling
- Programming, duplicating, testing and debugging tools available in source code

Operating Environment

- Wide OS support, including:
  - Symbian OS (EPOC)
  - Windows CE Pocket PC
  - Windows CE Smartphone
  - Palm OS
  - Nucleus
  - Linux
  - ThreadX
  - OSE
  - VxWorks
- TrueFFS Software Development Kit (SDK) for quick and easy support for proprietary OSs, or OS-less environment
- TrueFFS Boot Software Development Kit (BDK)

Power Requirements

- Operating voltage
  - Core and I/O: 1.65V to 1.95V
- Current Consumption
  - Active mode:
    Read: 4.2 mA
    Program/erase: 9.2 mA
  - Deep Power-Down mode: 4 μA

Capacity

- 64MB (512Mb) capacity
- Device cascading option for up to four devices (256MB/2Gb)

Packaging

- 85-ball FBGA package:
  7x10x1.2 mm (width x length x height)
- Ballout compatible with DiskOnChip G3 and DiskOnChip Plus FBGA 7x10 mm and 9x12 mm products:

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1. INTRODUCTION

This data sheet includes the following sections:

Section 1: Overview of data sheet contents

Section 2: Product overview, including a brief product description, ball diagrams and signal descriptions

Section 3: Theory of operation for the major building blocks

Section 4: Major features and benefits of x2 technology

Section 5: Detailed description of hardware protection and security-enabling features

Section 6: Detailed description of modes of operation and TrueFFS technology, including power failure management and 8KByte memory window

Section 7: DiskOnChip G3 register descriptions

Section 8: Overview of how to boot from DiskOnChip G3 LP

Section 9: Hardware and software design considerations

Section 10: Environmental, electrical, timing and product specifications

Section 11: Information on ordering DiskOnChip G3 LP

For additional information on M-Systems' flash disk products, please contact one of the offices listed on the back page.

2. PRODUCT OVERVIEW

2.1 Product Description

DiskOnChip G3 Low Power (LP) 1.8V is the latest addition to M-Systems' DiskOnChip G3 flash disk product family. DiskOnChip G3 LP, packed in the smallest available FBGA package with 64MB (512Mb) capacity, single-die device with an embedded thin flash controller and flash memory, DiskOnChip G3 LP also offers attractive cost benefits based on its use of Toshiba's 0.13 micron Multi-Level Cell (MLC) NAND flash technology, enhanced by M-Systems' proprietary x2 technology. MLC NAND technology enables two bits of data to be stored on a single cell, cutting in half the physical die size. M-Systems' proprietary x2 technology overcomes MLC-related error patterns and slow transfer rates by using a robust error detection and correction (EDC/ECC) mechanism. Furthermore, it provides performance enhancement with multi-plane operation, DMA support, and turbo operation. The combination of MLC and x2 technology results in a low-cost, minimal-sized flash disk that achieves unsurpassed reliability levels and enhanced performance.

This breakthrough in power consumption, performance, size and cost makes DiskOnChip G3 LP the ideal solution for product manufacturers who require high-capacity, small size, high-performance, and above all, high-reliability storage to enable applications such as Digital TVs (DTVs), rugged handheld terminals, Digital Still Cameras (DSCs), Mobile Point of Sale (POS), telecom equipment, multimedia phones, camera and Video on Demand (VOD) phones, enhanced Multimedia Messaging Service (MMS), gaming, video and Personal Information Management (PIM) on mobile handsets, and Personal Digital Assistants (PDAs).

As with the DiskOnChip G3 family, DiskOnChip G3 LP content protection and security-enabling features offer several benefits. Two write- and read-protected partitions, with both software- and hardware-based protection, can be configured independently for maximum design flexibility. The 16-byte Unique ID (UID) identifies each flash device, eliminating the need for a separate ID device on the motherboard. The 6KB One Time Programmable (OTP) area, written to once and then locked to prevent data and code from being altered, is ideal for storing customer and product-specific information.

DiskOnChip G3 LP 64MB (512Mb) has a 2KB Programmable Boot Block. This block provides eXecute In Place (XIP) functionality, enabling DiskOnChip G3 LP to replace the boot device and function as the only non-volatile memory device on-board. Eliminating the need for an additional boot device reduces hardware expenditures, board real estate, programming time, and logistics.

M-Systems' patented TrueFFS software technology fully emulates a hard disk to manage the files stored on DiskOnChip G3 LP. This transparent file system management enables read/write operations that are identical to a standard, sector-based hard disk. In addition, TrueFFS employs patented methods, such as virtual mapping, dynamic and static wear-leveling, and automatic block management to ensure high data reliability and to maximize flash life expectancy.

2.2 Standard Interface

2.2.1 Ball Diagram

See Figure 1 for the DiskOnChip G3 LP 64MB (512Mb) ballout for the standard interface. To ensure proper device functionality, balls marked RSRVD are reserved for future use and should not be connected.

Note: Third-generation DiskOnChip G3 LP is designed as a drop-in replacement for DiskOnChip G3 and second-generation (G2) DiskOnChip Plus products, assuming that the latter were integrated according to migration guide guidelines. Refer to the *DiskOnChip Plus (G2) to DiskOnChip G3/P3* migration guide for further information.

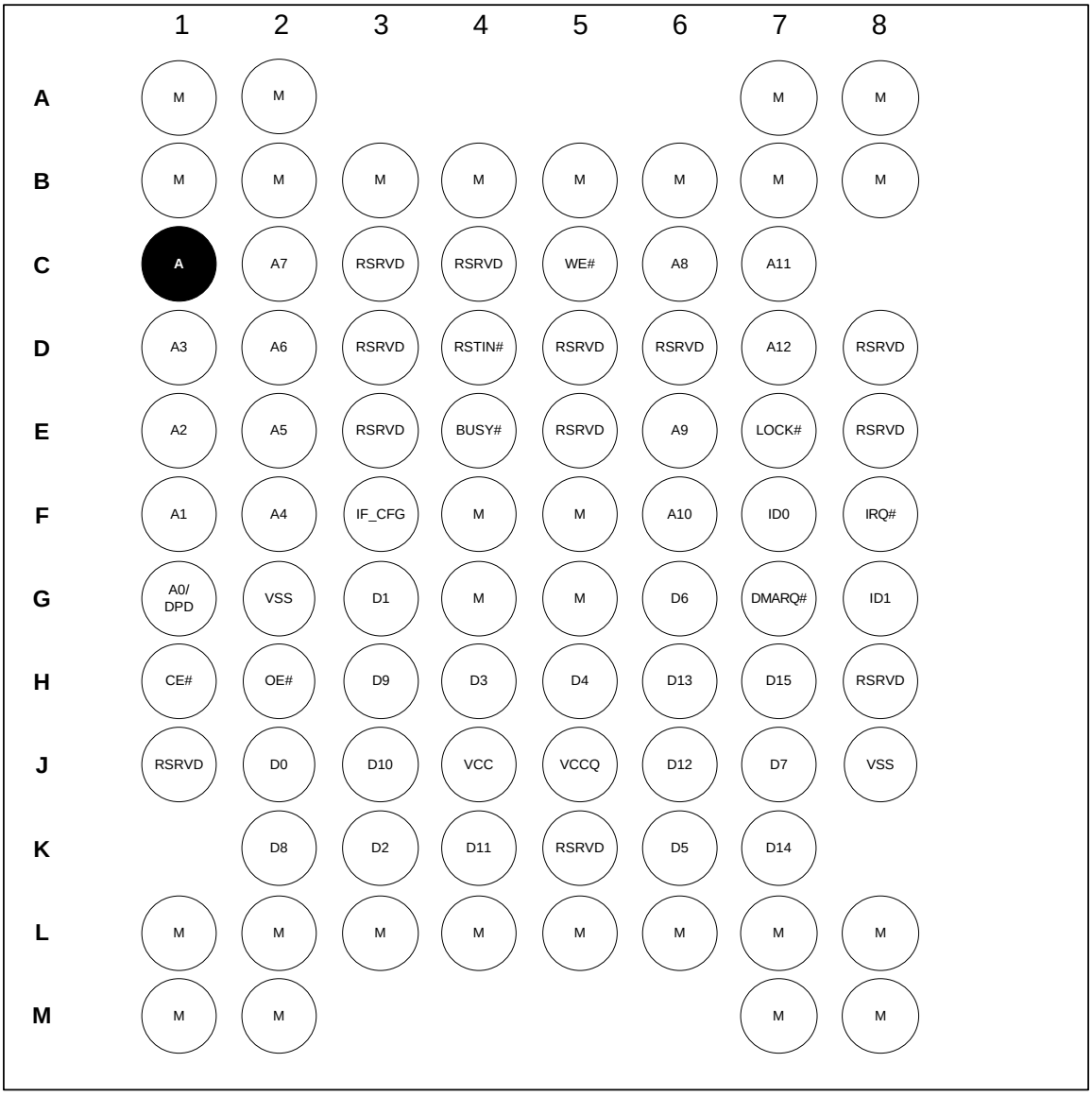


Figure 1: DiskOnChip G3 LP 7x10 FBGA Ballout for Standard Interface

2.2.2 System Interface

See Figure 2 for a simplified I/O diagram for a standard interface of DiskOnChip G3 LP 64MB (512Mb).

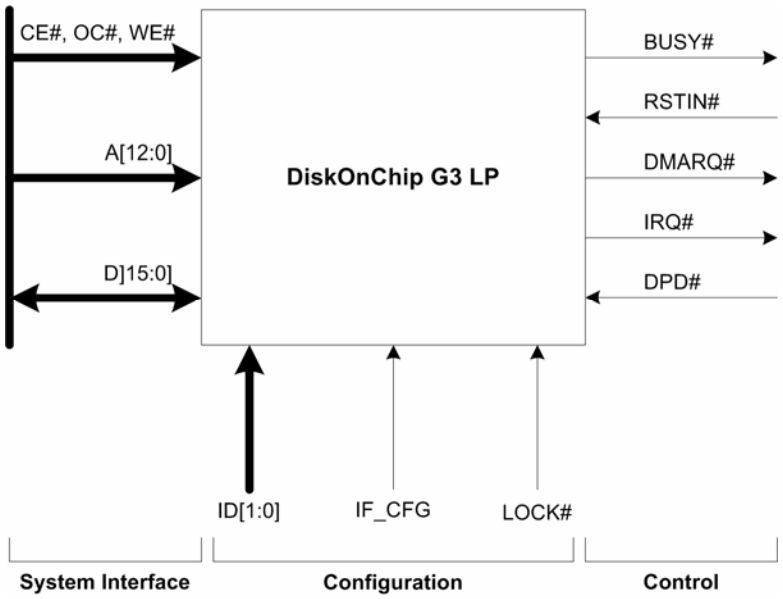


Figure 2: DiskOnChip G3 LP Standard Interface Simplified I/O Diagram

2.2.3 Signal Descriptions

DiskOnChip G3 LP FBGA packages support identical signals. The related ball designations are listed in the signal descriptions, presented in logic groups, in Table 1.

Table 1: Signal Descriptions for DiskOnChip G3 LP Standard Interface

Signal	Ball No.	Input Type[1]	Description	Signal Type
System Interface				
A[12:11] A[10:8] A[7:4] A[3:0]	D7, C7 F6, E6, C6 C2, D2, E2, F2 D1, E1, F1, G1		Address bus. When IF_CFG=1, A[0] is multiplexed with the DPD ball.	Input
D[15:14] D[13:12] D[11:8]	H7, K7 H6, J6 K4, J3, H3, K2	R8	Data bus, high byte. Not used and may be left floating when IF_CFG is set to 0 (8-bit mode).	Input/ Output
D[7:6] D[5:3] D[2:0]	J7, G6 K6, H5, H4 K3, G3, J2		Data bus, low byte.	Input/ Output
CE#	H1		Chip Enable, active low	Input
OE#	H2		Output Enable, active low	Input
WE#	C5		Write Enable, active low	Input
Configuration				
ID[1:0]	G8, F7		Identification. Configuration control to support up to four chips cascaded in the same memory window. Chip 1 = ID1, ID0 = VSS, VSS (0,0); must be used for single chip configuration Chip 2 = ID1, ID0 = VSS, VCCQ (0,1) Chip 3 = ID1, ID0 = VCCQ, VSS (1,0) Chip 4 = ID1, ID0 = VCCQ, VCCQ (1,1)	Input
LOCK#	E7		Lock, active low. When active, provides full hardware data protection of selected partitions.	Input
IF_CFG	F3		Interface Configuration, 1 (VCCQ) for 16-bit interface mode, 0 (VSS) for 8-bit interface mode.	Input
Control				
BUSY#	E4	OD	Busy, active low, open drain. Indicates that DiskOnChip is initializing and should not be accessed. A 10 KΩ pull-up resistor is required if this ball drives an input. A 10 KΩ pull-up resistor is recommended even if this ball is not used.	Output
RSTIN#	D4		Reset, active low.	Input

Signal	Ball No.	Input Type[1]	Description	Signal Type
DMARQ#	G7	OD	DMA Request, active low. A 10 KΩ pull-up resistor is required if this ball drives an input. A 10 KΩ pull-up resistor is recommended even if this ball is not used.	Output
IRQ#	F8	OD	Interrupt Request, active low. A 10 KΩ pull-up resistor is required if this ball drives an input. A 10 KΩ pull-up resistor is recommended even if this ball is not used.	Output
DPD	G1		Deep Power-Down. Used to enter and exit Deep Power-Down mode. This ball is assigned A0 instead of DPD when working in 8-bit mode.	Input
Power				
VCC	J4	-	Device supply. Requires a 10 nF and 0.1 µF capacitor.	Supply
VCCQ	J5	-	I/O power supply. Sets the logic **1** voltage level range of I/O balls. VCCQ should be connected to 1.65V to 1.95V. Requires a 10 nF and 0.1 µF capacitor.	Supply
VSS	G2, J8	-	Ground. All VSS balls must be connected.	Supply
Other				
RSRVD	E3	-	Reserved. If compatibility with previous DiskOnChip versions is necessary: In 16-bit mode (IF_CFG = 1) this ball must be connected to GND for compatibility with G2 devices. In 8-bit mode (IF_CFG = 0) may be left floating. Refer to the *DiskOnChip Plus (G2) to DiskOnChip G3/P3* migration guide for design guidelines when migrating from previous DiskOnChip versions (G2).	
	K5		System Clock. Not used in DiskOnChip G3 LP and may be left floating. To guarantee forward compatibility with future products, it is recommended to connect this signal to the system clock.	Input
	See Figure 1	-	Reserved. Other reserved signals are not connected internally and must be left floating to guarantee forward compatibility with future products.	
	M	-	Mechanical. These balls are for mechanical placement, and are not connected internally.	
	A	-	Alignment. This ball is for device alignment and is not connected internally.	

1. The following abbreviations are used: IN - Standard (non-Schmidt) input, OD - Open drain output, R8 - Nominal 22K pull-up resistor, enabled only for 8-bit interface mode (IF_CFG input is 0)

2.3 Multiplexed Interface

2.3.1 Ball Diagram

See Figure 3 for the DiskOnChip G3 LP 64MB (512Mb) ballout for the multiplexed interface. To ensure proper device functionality, balls marked RSRVD are reserved for future use and should not be connected.

Note: Third-generation DiskOnChip G3 LP is designed as a drop-in replacement for DiskOnChip G3 and second-generation (G2) DiskOnChip Plus products, assuming that the latter were integrated according to migration guide guidelines. Refer to the *DiskOnChip Plus (G2) to DiskOnChip G3/P3* migration guide for further information.

	1	2	3	4	5	6	7	8
A	M	M					M	M
B	M	M	M	M	M	M	M	M
C	A	VSS	RSRVD	RSRVD	WE#	VSS	VSS	
D	VSS	VSS	RSRVD	RSTIN#	RSRVD	RSRVD	VSS	RSRVD
E	VSS	VSS	RSRVD	BUSY#	RSRVD	VSS	LOCK#	RSRVD
F	VSS	VSS	VCCQ	M	M	VSS	ID0	IRQ#
G	DPD	VSS	AD1	M	M	AD6	DMARQ#	AVD#
H	CE#	OE#	AD9	AD3	AD4	AD13	AD15	RSRVD
J	RSRVD	AD0	AD10	VCC	VCCQ	AD12	AD7	VSS
K		AD8	AD2	AD11	RSRVD	AD5	AD14	
L	M	M	M	M	M	M	M	M
M	M	M					M	M

Figure 3: DiskOnChip G3 LP 7x10 FBGA Ballout for Multiplexed Interface

2.3.2 System Interface

See Figure 4 for a simplified I/O diagram of DiskOnChip G3 LP 64MB (512Mb).

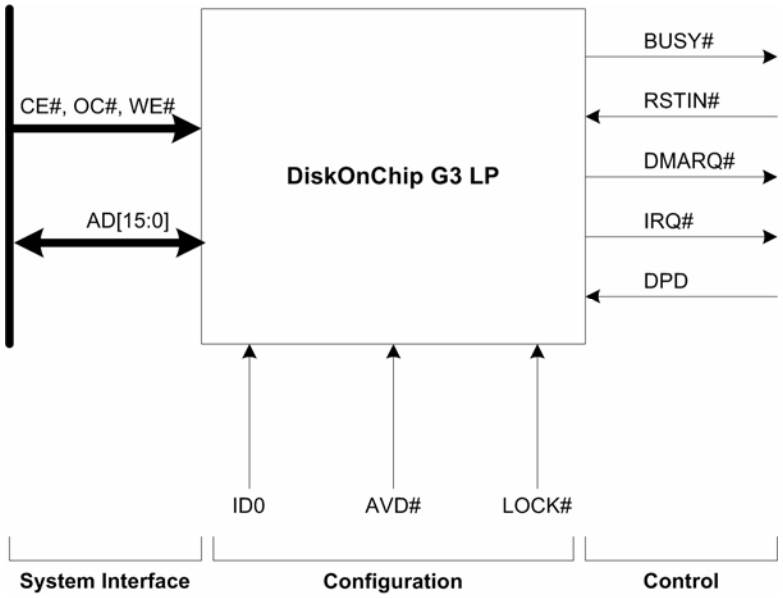


Figure 4: DiskOnChip G3 LP Multiplexed Interface Simplified I/O Diagram

2.3.3 Signal Description

DiskOnChip G3 LP 64MB (512Mb) 7x10 FBGA packages support identical signals in the multiplexed interface. The related ball designations are listed in the signal descriptions, presented in logic groups, in Table 2.

Table 2: DiskOnChip G3 LP Signal Descriptions for Multiplexed Interface

Signal	Ball No.	Input Type[1]	Description	Signal Type
System Interface				
AD[15:14] AD[13:12] AD[11:9] AD[8:6] AD[5:3] AD[2:0]	H7, K7 H6, J6 K4, J3, H3 K2, J7, G6 K6, H5, H4 K3, G3, J2		Multiplexed bus. Address and data signals	Input/ Output
CE#	H1		Chip Enable, active low	Input
OE#	H2		Write Enable, active low	Input
WE#	C5		Output Enable, active low	Input
Configuration				
AVD#	G8		Set multiplexed interface. Logic- 0 indicates that the host is driving a valid address on the AD[15:0] bus.	Input
ID0	F7		Identification. Configuration control to support up to two chips cascaded in the same memory window. Chip 1 = ID0 = VSS; must be used for single-chip configuration Chip 2 = ID0 = VCC	Input
LOCK#	E7		Lock, active low. When active, provides full hardware data protection of selected partitions.	Input
Control				
BUSY#	E4	OD	Busy, active low, open drain. Indicates that DiskOnChip is initializing and should not be accessed A 10 KΩ pull-up resistor is required if this ball drives an input. A 10 KΩ pull-up resistor is recommended even if this ball is not used.	Output
RSTIN#	D4		Reset, active low.	Input
DMARQ#	G7	OD	DMA Request, active low. A 10 KΩ pull-up resistor is required if this ball drives an input. A 10 KΩ pull-up resistor is recommended even if this ball is not used.	Output
IRQ#	F8	OD	Interrupt Request, active low. A 10 KΩ pull-up resistor is required if this ball drives an input. A 10 KΩ pull-up resistor is recommended even if this ball is not used.	Output

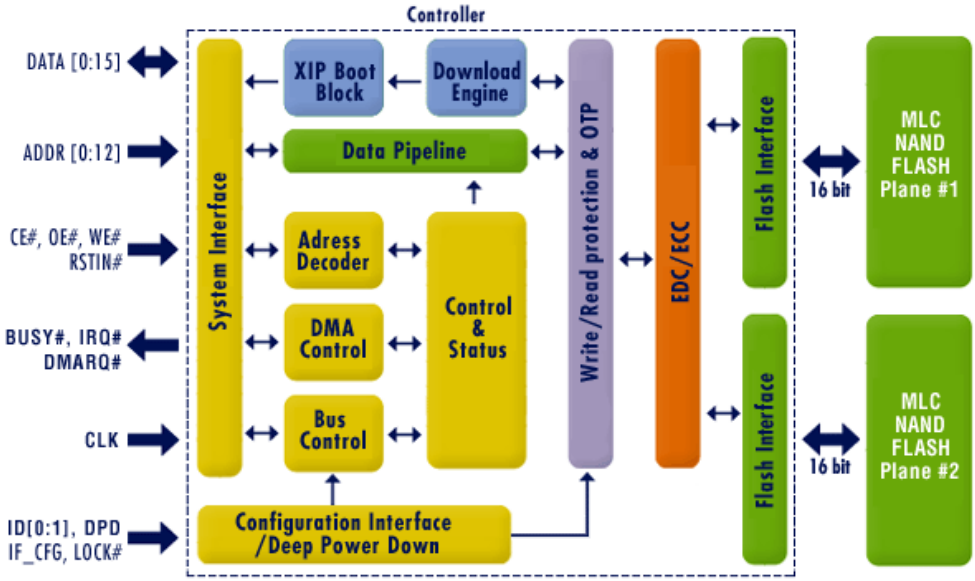
Signal	Ball No.	Input Type[1]	Description	Signal Type
DPD	G1		Deep Power-Down. Used to enter and exit Deep Power-Down mode. This ball is assigned A0 instead of DPD when working in 8-bit mode.	Input
Power				
VCC	J4	-	Device core supply. Requires a 10 nF and 0.1 µF capacitor.	Supply
VCCQ	J5, F3	-	I/O power supply. Sets the logic **1** voltage level range of I/O balls. VCCQ should be connected to 1.65V to 1.95V. Requires a 10 nF and 0.1 µF capacitor.	Supply
VSS	G2,J8, D7, C7, F6, E6, C6, C2, D2, E2, F2, D1, E1, F1	-	Ground. All VSS balls must be connected.	Supply
Other				
Reserved	See Figure 3	-	Reserved. Reserved signals are not connected internally and must be left floating to guarantee forward compatibility with future products.	
	K5		System Clock. Not used in DiskOnChip G3 LP and may be left floating. To guarantee forward compatibility with future products, it is recommended connecting it to the System clock.	Input
	M		Mechanical. These balls are for mechanical placement, and are not connected internally.	
	A	-	Alignment. This ball is for device alignment and is not connected internally.	

1. The following abbreviations are used: IN - Standard (non-Schmidt) input, OD - Open drain output

3. THEORY OF OPERATION

3.1 Overview

DiskOnChip G3 LP consists of the following major functional blocks, as shown in Figure 5.



*ADDR[0] and DPD are multiplexed on the same ball

Figure 5: DiskOnChip G3 LP Simplified Block Diagram, Standard Interface

These components are described briefly below and in more detail in the following sections.

- **System Interface** for the host interface.
- **Configuration Interface** for configuring DiskOnChip G3 LP to operate in 8-bit, 16-bit mode, cascaded configuration, hardware read/write protection and entering/exiting Deep Power-Down mode.
- **Read/Write Protection and OTP** for advanced data/code security and protection.
- **Programmable Boot Block with XIP** functionality enhanced with a **Download Engine (DE)** for system initialization capability.
- **Error Detection and Error Correction Code (EDC/ECC)** for on-the-fly error handling.
- **Data Pipeline** through which the data flows from the system to the NAND flash arrays.
- **Control & Status** block that contains registers responsible for transferring the address, data and control information between the TrueFFS driver and the flash media.
- **Flash Interface** that interfaces to two NAND flash planes.
- **Bus Control** for translating the host bus address, and data and control signals into valid NAND flash signals.
- **Address Decoder** to enable the relevant unit inside the DiskOnChip controller, according to the address range received from the system interface.

3.2 System Interface

3.2.1 Standard (NOR-Like) Interface

The system interface block provides an easy-to-integrate NOR-like (also SRAM and EEPROM-like) interface to DiskOnChip G3 LP, enabling it to interface with various CPU interfaces, such as a local bus, ISA bus, NOR interface, SRAM interface, EEPROM interface or any other compatible interface. In addition, the EEPROM-like interface enables direct access to the Programmable Boot Block to permit XIP (Execute-In-Place) functionality during system initialization.

A 13-bit wide address bus enables access to the DiskOnChip G3 LP 8KB memory window (as shown in Section 6.5). A 32-bit internal data bus is supported by parallel access to two 32MB (256Mb) flash planes (for 64MB/512Mb single-die devices), each of which enables 16-bit access. This 16-bit data bus permits 16-bit wide access to the host.

The Chip Enable (CE#), Write Enable (WE#) and Output Enable (OE#) signals trigger read and write cycles. A write cycle occurs while both the CE# and the WE# inputs are asserted. Similarly, a read cycle occurs while both the CE# and OE# inputs are asserted. Note that DiskOnChip G3 LP does not require a clock signal. It features a unique analog static design, optimized for minimal power consumption. The CE#, WE# and OE# signals trigger the controller (e.g., system interface block, bus control and data pipeline) and flash access.

The Reset In (RSTIN#) and Busy (BUSY#) control signals are used in the reset phase.

The Interrupt Request (IRQ#) signal can be used when long I/O operations, such as Block Erase, delay the CPU resources. The signal is also asserted when a Data Protection violation has occurred. This signal frees the CPU to run other tasks, continuing read/write operations with DiskOnChip G3 LP only after the IRQ# signal has been asserted and an interrupt handling routine (implemented in the OS) has been called to return control to the TrueFFS driver.

The DMARQ# output is used to control multi-page DMA operations, as described in Section 4.1.

3.2.2 Multiplexed Interface

In this configuration, the address and data signals are multiplexed. The ID[1] input is driven by the host AVD# signal, and the D[15:0] balls, used for both address inputs and data, are connected to the host AD[15:0] bus. While AVD# is asserted, the host drives AD[11:0] with bits [12:1] of the address. Host signals AD[15:12] are not significant during this part of the cycle.

This interface is automatically used when a falling edge is detected on ID[1]. This edge must occur after RSTIN# is negated and before the first read or write cycle to the controller. The first access must be a read cycle. When using a multiplexed interface, the value of ID[1] is internally forced to logic-0. The only possible device ID values are 0 and 1; therefore, only up to two DiskOnChip G3 LP 64MB (512Mb) devices may be cascaded in multiplexed configuration.

3.3 Configuration Interface

The Configuration Interface block enables configuring DiskOnChip G3 LP to operate in different modes. The ID[1:0] signals are used in a cascaded configuration (refer to Section 9.6), the DPD signal is used to enter and exit Deep Power-Down mode (see Section 6.3), the LOCK# signal is used for hardware write/read protection, and the IF_CFG signal is used to configure 8/16-bit access.

3.4 Protection and Security-Enabling Features

The Protection and Security-Enabling block, consisting of read/write protection, UID and an OTP area, enables advanced data and code security and content protection. Located on the main route of traffic between the host and the flash, this block monitors and controls all data and code transactions to and from DiskOnChip G3 LP.

3.4.1 Read/Write Protection

Data and code protection is implemented through a Protection State Machine (PSM). The user can configure one or two independently programmable areas of the flash memory as read protected, write protected, or read/write protected.

A protected partition may be protected by either/both of these hardware mechanisms:

- 64-bit protection key
- Hard-wired LOCK# signal

If the Lock option is enabled (by means of software) and the LOCK# signal is asserted, the protected partition has an additional hardware lock that prevents read/write access to the partition, even with the use of the correct protection key.

The size and protection attributes of the protected partition are defined during the media-formatting stage.

In the event of an attempt to bypass the protection mechanism, illegally modify the protection key or in any way sabotage the configuration parameters, the entire DiskOnChip G3 becomes both read and write protected, and is completely inaccessible.

For further information on hardware protection, please refer to the *TrueFFS Software Development Kit (SDK)* developer guide.

3.4.2 Unique Identification (UID) Number

Each DiskOnChip G3 LP is assigned a 16-byte UID number. Burned onto the flash during production, the UID cannot be altered and is unique worldwide. The UID is essential in security-related applications, and can be used to identify end-user products in order to fight fraudulent duplication by imitators.

3.4.3 One-Time Programmable (OTP) Area

The 6KB OTP area is user programmable for complete customization. The user can write to this area once, after which it is automatically and permanently locked. After it is locked, the OTP area becomes read only, just like a ROM device.

Typically, the OTP area is used to store customer and product information such as: product ID, software version, production data, customer ID and tracking information.

3.4.4 One-Time Write (ROM-Like) Partition

A partition in the DiskOnChip G3 LP can be set as One-Time Write. After it is locked, this partition becomes read only, just like a ROM device. Its capacity is defined during the media-formatting stage.

3.4.5 Sticky Lock (SLOCK)

The boot partition can be locked automatically by hardware after the boot phase is completed and the device is in Normal mode. This is done by setting the Sticky Lock (SLOCK) bit in the Output Control register to 1. This has the same effect as asserting the LOCK# signal. Once set, SLOCK can only be cleared by asserting the RSTIN# input. Like the LOCK# input, assertion of this bit prevents the protection key from disabling the protection for a given partition. There is no need to mount the partition before calling a hardware protection routine.

This feature can be useful when the boot code in the boot partition must be read/write protected. Upon power-up, the boot code must be unprotected so the CPU can boot directly from DiskOnChip. At the end of the boot process, protection can be set until the next power-up or reset.

3.5 Programmable Boot Block with eXecute In Place (XIP) Functionality

The Programmable Boot Block with XIP functionality enables DiskOnChip G3 to act as a boot device in addition to performing flash disk data storage functions. This eliminates the need for expensive, legacy NOR flash or any other boot device on the motherboard.

The Programmable Boot Block on DiskOnChip G3 LP 64MB (512Mb) is 2KB in size. The Download Engine (DE), described in the next section, expands the functionality of this block by copying the boot code from the flash into the boot block.

DiskOnChip G3 LP 64MB (512Mb) devices may be cascaded in order to form a larger flash disk. When DiskOnChip G3 LP 512Mb (64MB) is connected with a standard NOR-like interface, up to four devices may be cascaded to create a 256MB (2Gb) flash disk. When DiskOnChip G3 64MB (512Mb) is connected with a multiplexed interface, up to two devices may be cascaded to create a 128MB (1Gb) flash disk.

Notes: 1. When more than one DiskOnChip G3 LP 64MB (512Mb) device is cascaded, a maximum boot block of 4KB is available. The Programmable Boot Block of each device is mapped to a unique address space.

3.6 Download Engine (DE)

Upon power-up or when the RSTIN# signal is asserted, the DE automatically downloads the Initial Program Loader (IPL) to the Programmable Boot Block. The IPL is responsible for starting the booting process. The download process is quick, and is designed so that when the CPU accesses DiskOnChip G3 LP for code execution, the IPL code is already located in the Programmable Boot Block. During the download process, DiskOnChip G3 LP does not respond to read or write accesses. Host systems must therefore observe the requirements described in Section 10.3.6.

In addition, the DE downloads the data protection rules from the flash to the Protection State Machines (PSM), so that DiskOnChip G3 LP is secure and protected from the first moment it is active.

During the download process, DiskOnChip G3 LP asserts the BUSY# signal to indicate to the system that it is not yet ready to be accessed. Once BUSY# is negated, the system can access DiskOnChip G3 LP.

A failsafe mechanism prevents improper initialization due to a faulty VCC or invalid assertion of the RSTIN# input. Another failsafe mechanism is designed to overcome possible NAND flash data errors. It prevents internal registers from powering up in a state that bypasses the intended data protection. In addition, any attempt to sabotage the data structures causes the entire DiskOnChip to become both read and write protected, and completely inaccessible.

3.7 Error Detection Code/Error Correction Code (EDC/ECC)

Because NAND-based MLC flash is prone to errors, it requires unique error-handling capability. M-Systems' x2 technology implements 4-bit Error Detection Code/Error Correction Code (EDC/ECC), based on a patented combination of Bose, Chaudhuri and Hocquenghem (BCH) and Hamming code algorithms. Error Detection Code (EDC) is implemented in hardware to optimize performance, while Error Correction Code (ECC) is performed in software, when required, to save silicon costs.

Each time a 512-byte page is written, additional parity bits are calculated and written to the flash. Each time data is read from the flash, the parity bits are read and used to calculate error locations.

The Hamming code can detect 2 errors per page and correct 1 error per page. The BCH code can detect and correct 4 errors per page. It can even detect 5 errors per page with a probability of 99.9%. It ensures that the minimal amount of code required is used for detection and correction to deliver the required reliability without degrading performance.

3.8 Data Pipeline

DiskOnChip G3 LP uses a two-stage pipeline mechanism, designed for maximum performance while enabling on-the-fly data manipulation, such as read/write protection and Error Detection/Error Correction.

3.9 Control and Status

The Control and Status block contains registers responsible for transferring address, data and control information between the DiskOnChip TrueFFS driver and the flash media. Additional registers are used to monitor the status of the flash media (ready/busy) and the DiskOnChip controller. For further information on the DiskOnChip registers, refer to Section 7.

3.10 Flash Architecture

DiskOnChip G3 LP 64MB (512Mb) consists of two 32MB (256Mb) flash planes that consist of 1024 blocks each, organized in 64 pages, as follows:

- **Page** – Each page contains 512 bytes of user data and a 16-byte extra area that is used to store flash management and EDC/ECC signature data, as shown in Figure 6.
- **Block (Erase Unit)** – Each block contains 64 pages (total of 256Kb), as shown in Figure 7. A block is the minimal unit that can be erased, and is sometimes referred to as an erase block.

  Note: Since the device works with multiple planes, the operational block size is 512Kb, as described in the next section.

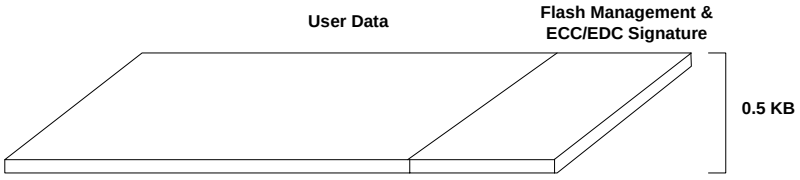


Figure 6: Page Structure

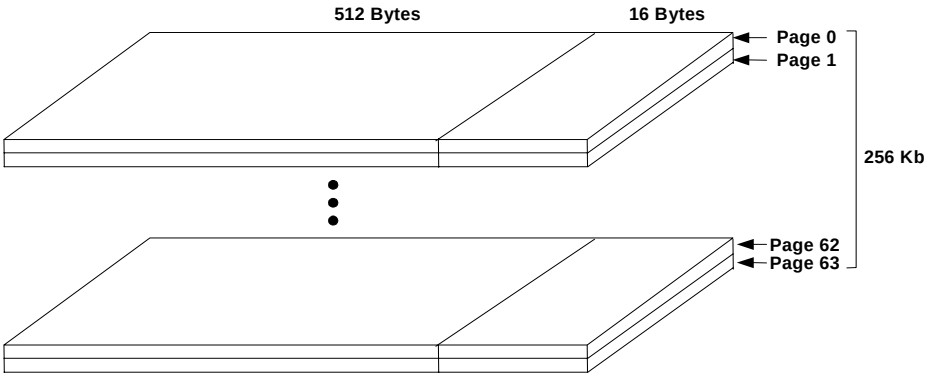


Figure 7: Block Structure

Parallel Multi-Plane Access

The two 32MB (256Mb) flash planes operate in parallel, thereby providing a true 32-bit internal data bus and four times the read, write and erase performance. Two pages on different planes can be concurrently read or written if they have the same offset within their respective units, even if the units are unaligned.

Bad units are mapped individually on each plane by enabling unaligned unit access, as shown in Figure 8. Good units can therefore be aligned or unaligned, minimizing the effects of bad units on the media. Without this capability, a bad unit in one plane would cause a good unit in the second

plane to be tagged as a bad unit, making it unusable. This customized method of bad unit handling for two planes enhances data utilization without adversely affecting performance.

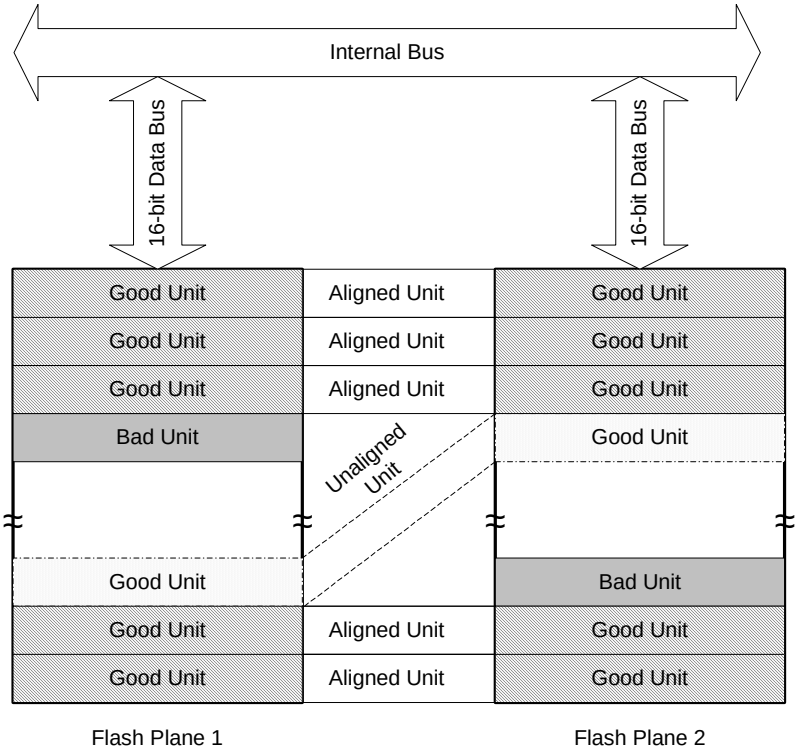


Figure 8: Unaligned Multi-Plane Access

4. X2 TECHNOLOGY

DiskOnChip G3 LP enhances performance using various proprietary techniques:

- Parallel access to the separate 32MB (256Mb) flash planes, thereby providing an internal 32-bit data bus. See Section 3.10 for further information.
- DMA operation to release the CPU for other tasks in coordination with the platform's DMA controller. This is especially useful during the boot stage. Up to 64KB of data can be transferred during a DMA operation.

4.1 DMA Operation

DiskOnChip G3 LP provides a DMARQ# output that enables up to 64KB to be read from the flash by the host DMA controller. During DMA operation, the DMARQ# output is used to notify the host DMA controller that the next flash page is ready to be read, and the IRQ# ball indicates whether an error occurred while reading the data from the flash or the end of the DMA transfer was reached.

The DMARQ# output sensitivity is chosen by setting the EDGE bit in the DMA Control register[0]:

- **Edge** – The DMARQ# output pulses to logic 0 for 250~500 nsec to indicate to the DMA controller that a flash page is ready to be read. The EDGE bit is set to 1 for this mode.
- **Level** – The DMARQ# output is asserted to initiate the block transfer and returns to the negated state at the end of each block transfer. The EDGE bit is set to 0 for this mode.

The following steps are required to initiate a DMA operation:

1. Initialize the platform's DMA controller to transfer 512 bytes upon each assertion of the DMARQ# output. If the DMA controller supports an edge-sensitive DMARQ# signal, then initialize the DMA controller to transfer 512 bytes upon each DMA request. If the DMA controller supports a level-sensitive DMARQ# signal, then initialize the DMA controller to transfer data while DMARQ# is asserted.
2. Set the bits in the Interrupt Control register (see Section 7) to enable interrupts on an ECC error and at the end of the DMA operation.
3. Write to the DMA Control register[0] to set the DMA_EN bit, the EDGE bit and the number of sectors (SECTOR_COUNT field) to be transferred to the host. At this point, DiskOnChip G3 LP generates a DMA request to indicate to the host that it is ready to transfer data.
4. The host DMA controller reads one sector (512 bytes) of data from DiskOnChip G3 LP.
5. If an ECC error is detected, an interrupt is generated (IRQ# signal asserted), the transfer of data is halted and control is returned to the host. If no ECC error is detected, a DMA request is initiated (DMARQ# signal asserted) and the next sector is read by the host.
6. The process continues until the last sector is read, after which DiskOnChip G3 LP generates an interrupt (IRQ# signal asserted) to indicate that it has transferred the last byte.

Notes: 1. DiskOnChip G3 LP generates a DMA request (DMARQ# signal asserted) after the last byte is read. It may therefore be necessary to clear the final DMA request from the DMA controller.

2. DMA operation may be aborted after transferring each 512-byte block (step 4) by clearing the DMA_EN bit in the DMA Control register[0].

3. RAM access is not permitted during DMA operation.

5. HARDWARE PROTECTION

5.1 Method of Operation

DiskOnChip G3 LP enables the user to define two partitions that are protected (in hardware) against any combination of read or write operations. The two protected areas can be configured as read protected or write protected, and are protected by a protection key (i.e. password) defined by the user. Each of the protected areas can be configured separately and can function separately, providing maximum flexibility for the user.

The size and protection attributes (protection key, read, write, changeable, lock) of the protected partition are defined in the media formatting stage (DFORMAT utility or the format function in the TrueFFS SDK).

In order to set or remove read/write protection, the protection key (i.e., password) must be used, as follows:

- Insert the protection key to remove read/write protection.
- Remove the protection key to set read/write protection.

DiskOnChip G3 LP has an additional hardware safety measure. If the Lock option is enabled (by means of software) and the LOCK# signal is asserted, the protected partition has an additional hardware lock that prevents read/write access to the partition, even with the use of the correct protection key. It is possible to set the Lock protection for one session only; that is, until the next power-up or reset. This Sticky Lock feature can be useful when the boot code in the boot partition must be read/write protected. Upon power-up, the boot code must be unprotected so the CPU can run it directly from DiskOnChip G3 LP. At the end of the boot process, protection can be set until the next power-up or reset.

Setting the Sticky Lock (SLOCK) bit in the Output Control register to 1 has the same effect as asserting the LOCK# signal. Once set, SLOCK can only be cleared by asserting the RSTIN# input. Like the LOCK# input, the assertion of this bit prevents the protection key from disabling the protection for a given partition. For more information, see Section 3.4.5. The target partition does not require mounting before calling a hardware protection routine.

The only way to read or write from a protected partition is to insert the key (even DFORMAT cannot remove the protection). This is also true for modifying its attributes (protection key, read, write and lock). Read/write protection is disabled (the key is automatically removed) in each of the following events:

- Power-down
- Change of any protection attribute (not necessarily in the same partition)
- Write operation to the IPL area
- Removal of the protection key.

For further information on hardware protection, please refer to the *TrueFFS Software Development Kit (SDK)* developer guide.

5.2 Low-Level Structure of the Protected Area

The first five blocks in DiskOnChip G3 LP contain foundry information, the Data Protect structures, IPL code, and bad block mapping information. See Figure 9.

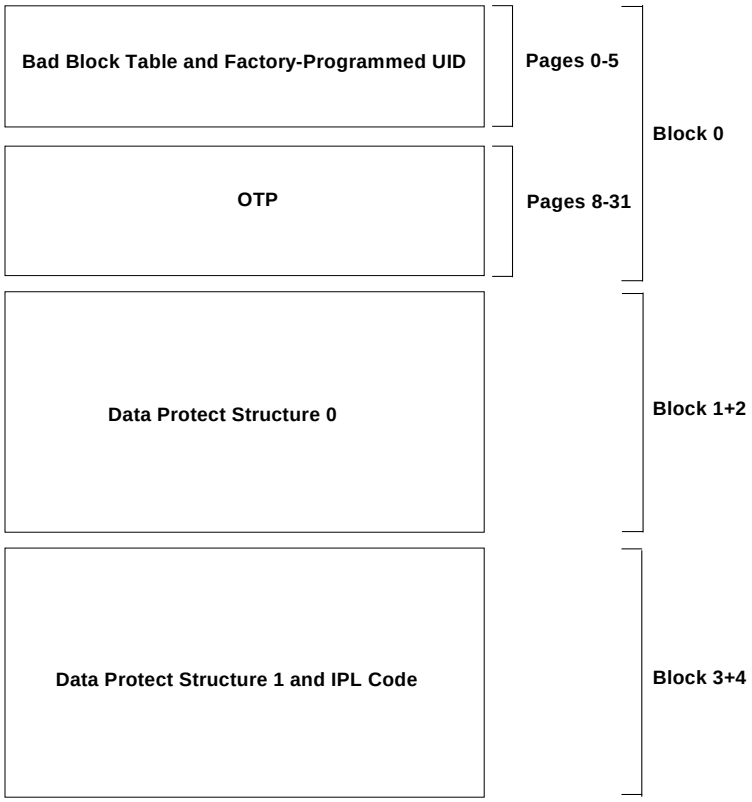


Figure 9: Low Level Structure of DiskOnChip G3

Blocks 0-4 in DiskOnChip G3 contain the following information:

Block 0

- Bad Block Table (page 4). Contains the information on unusable erase units on the flash media.
- UID (16 bytes). This number is written during the manufacturing stage, and cannot be altered at a later time.
- Customer OTP (occupies pages 8-31). The OTP area is written once and then locked.

Block 1 and 2

- Data Protect Structure 0. This structure contains configuration information on one of the two user-defined protected partitions. Block 2 is a copy of Block 1 for redundancy purposes.

Block 3 and 4

- Data Protect Structure 1. This structure contains configuration information on one of the two user-defined protected partitions.
- IPL Code (2KB). This is the boot code that is downloaded by the DE to the internal boot block.
- Block 4 is a copy of Block 3 for redundancy purposes.

6. MODES OF OPERATION

DiskOnChip G3 LP operates in one of three basic modes:

- Normal mode
- Reset mode
- Deep Power-Down mode

The current mode of the chip can always be determined by reading the DiskOnChip Control register. Mode changes can occur due to any of the following events:

- Assertion of the RSTIN# signal sets the device in Reset mode.
- During host power-up, boot detector circuitry sets the device in Reset mode.
- A valid write sequence to DiskOnChip G3 LP sets the device in Normal mode. This is done automatically by the TrueFFS driver on power-up (reset sequence end).
- Switching back from Normal mode to Reset mode can be done by a valid write sequence to DiskOnChip G3 LP, or by triggering the boot detector circuitry (via a soft reset).
- Deep Power-Down
  - A valid write sequence, initiated by software, sets the device from Normal mode to Deep Power-Down mode. Twelve read cycles from offset 0x1FFF set the device back to Normal mode. Alternately, the device can be set back to Normal mode with an extended access time during a read from the Programmable Boot Block.
  - Asserting the RSTIN# signal and holding it in this state puts the device in Deep Power-Down mode. When RSTIN# is released, the device is left in Reset mode.
  - Toggling the DPD signal as defined by the DPD Control register.

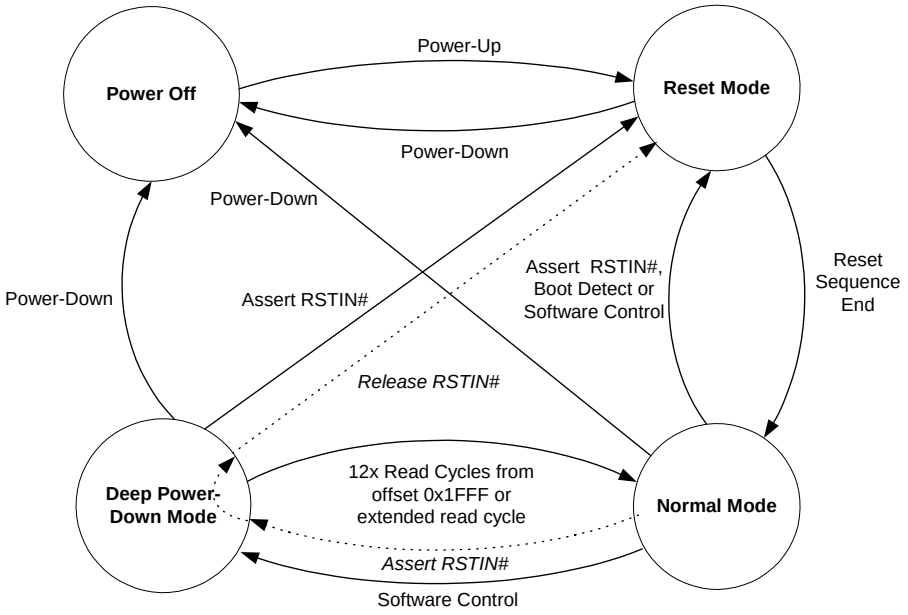


Figure 10: Operation Modes and Related Events

6.1 Normal Mode

This is the mode in which standard operations involving the flash memory are performed. Normal mode is entered when a valid write sequence is sent to the DiskOnChip Control register and Control Confirmation register. A write cycle occurs when both the CE# and WE# inputs are asserted. Similarly, a read cycle occurs when both the CE# and OE# inputs are asserted. Because the flash controller generates its internal clock from these CPU bus signals and some read operations return volatile data, it is essential that the timing requirements specified in Section 10.3 be met. It is also essential that read and write cycles not be interrupted by glitches or ringing on the CE#, WE#, and OE# inputs. All inputs to DiskOnChip G3 LP are Schmidt Trigger types to improve noise immunity.

6.2 Reset Mode

In Reset mode, DiskOnChip G3 LP ignores all write cycles, except for those to the DiskOnChip Control register and Control Confirmation register. All register read cycles return a value of 00H. Before attempting to perform any operation, the device is set to Normal mode by TrueFFS software.

6.3 Deep Power-Down Mode

While in Deep Power-Down mode, DiskOnChip G3 LP's quiescent power dissipation is reduced by disabling internal high current consumers (e.g. voltage regulators, input buffers, oscillator etc.). The following signals are also disabled in this mode:

- **Standard interface**: Input buffers A[12:0], WE#, D[15:0] and OE# (when CE# is negated)
- **Multiplexed interface**: Input buffers AD[15:0], AVD#, WE# and OE# (when CE# is negated).

To enter Deep Power-Down mode, a proper sequence must be written to the DiskOnChip G3 Control registers and the CE# input must be negated. All other inputs should be VSS or VCC.

Asserting the RSTIN# signal and holding it in low state puts the device in Deep Power-Down mode. When the RSTIN# signal is released, the device is left in Reset mode.

Toggling the DPD signal, as defined by the DPD Control register, puts the device in Deep Power-Down mode as well. In Deep Power-Down mode, write cycles have no effect and read cycles return indeterminate data (DiskOnChip G3 does not drive the data bus). Entering Deep Power-Down mode and then returning to the previous mode does not affect the value of any register.

To exit Deep Power-Down mode, use one of the following methods:

- Read twelve times from address 1FFFH (Programmable Boot Block). The data returned is undefined.
- Perform a single read cycle from the Programmable Boot Block with an extended access time and address hold time as specified in the timing diagrams. The data returned will be correct. Please note that this option can only be used with a standard interface, not with a multiplexed interface.
- Toggle the DPD input as defined by the DPD Control register, wait a minimum of 600 nS, and then perform a read/write cycle with normal timing, as specified in the timing diagrams.

Applications that use DiskOnChip G3 LP as a boot device must ensure that the device is not in Deep Power-Down mode before reading the Boot vector/instructions. This can be done by pulsing RSTIN# to the asserted state and waiting for the BUSY# output to be negated, toggling the DPD signal, or by entering Reset mode via software.

6.4 TrueFFS Technology

6.4.1 General Description

M-Systems' patented TrueFFS technology was designed to maximize the benefits of flash memory while overcoming inherent flash limitations that would otherwise reduce its performance, reliability and lifetime. TrueFFS emulates a hard disk, making it completely transparent to the OS. In addition, since it operates under the OS file system layer (see Figure 11), it is completely transparent to the application.

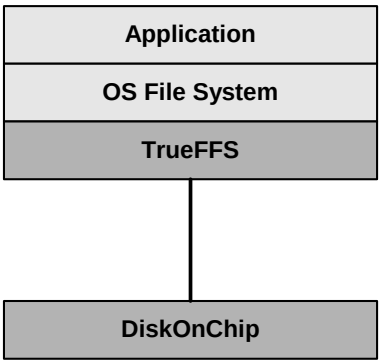


Figure 11: TrueFFS Location in System Hierarchy

TrueFFS technology support includes:

- Binary driver support for all major OSs
- TrueFFS Software Development Kit (TrueFFS SDK)
- Boot Software Development Kit (BDK)
- Support for all major CPUs, including 8, 16 and 32-bit bus architectures.

TrueFFS technology features:

- Block device API
- Flash file system management
- Bad-block management
- Dynamic virtual mapping
- Dynamic and static wear-leveling
- Power failure management
- Implementation of MLC-tailored EDC/ECC
- Performance optimization
- Compatibility with all DiskOnChip products

6.4.2 Built-In Operating System Support

The TrueFFS driver is integrated into all major OSs, including Symbian, Palm OS, Windows CE Pocket PC, Windows CE Smartphone, Windows CE, Linux (various kernels), Nucleus, OSE, and others. For a complete listing of all available drivers, please refer to M-Systems' website, www.m-systems.com. It is advised to use the latest driver versions that can be downloaded from the website.

6.4.3 TrueFFS Software Development Kit (SDK)

The basic *TrueFFS Software Development Kit (SDK)* developer guide provides the source code for the TrueFFS driver. It can be used in an OS-less environment or when special customization of the driver is required for proprietary OSs.

M-Systems also provide SureFS ruggedized file system support, designed to work optimally with TrueFFS. M-Systems' SureFS is a rugged, SCANDISK-free, FAT-16-compatible file system. SureFS offers protection from power failures and supports long file names only, which ensures data integrity after power failure.

When using DiskOnChip G3 LP as the boot replacement device, TrueFFS SDK also incorporates in its source code the boot software that is required for this configuration (this package is also available separately). Please refer to the *DiskOnChip Boot Software Development Kit (BDK)* developer guide for further information on using this software package.

Note: DiskOnChip G3 LP is supported by TrueFFS 6.1 and above.

6.4.4 File Management

TrueFFS accesses the flash memory within DiskOnChip G3 LP through an 8KB window in the CPU memory space. TrueFFS provides block device API by using standard file system calls, identical to those used by a mechanical hard disk, to enable reading from and writing to any sector on DiskOnChip G3 LP. This makes DiskOnChip G3 LP compatible with any file system and file system utilities, such as diagnostic tools and applications.

Note: DiskOnChip G3 LP is shipped unformatted and contains virgin media.

6.4.5 Bad-Block Management

Since NAND flash is an imperfect storage media, it can contain bad blocks that cannot be used for storage because of their high error rates. TrueFFS automatically detects and maps out bad blocks upon system initialization, ensuring that they are not used for storage. This management process is completely transparent to the user, who is unaware of the existence and location of bad blocks, while remaining confident of the integrity of data stored.

6.4.6 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the *erase cycle limit*, or *write endurance limit*, and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device. In DiskOnChip G3 LP, the erase cycle limit of the flash is 100,000 erase cycles. This means that after approximately 100,000 erase cycles, the erase block begins to generate storage errors at a rate significantly higher than the error rate that is typical to the flash.

In a typical application, and especially if a file system is used, specific pages are constantly updated (e.g., the page/s that contain the FAT, registry, etc.). Without any special handling, these pages would wear out more rapidly than other pages, reducing the lifetime of the entire flash.

To overcome this inherent deficiency, TrueFFS uses M-Systems' patented wear-leveling algorithm. This wear-leveling algorithm ensures that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime.

Dynamic Wear-Leveling

TrueFFS uses statistical allocation to perform dynamic wear-leveling on newly written data. This minimizes the number of erase cycles per block. Because a block erase is the most time-consuming operation, dynamic wear-leveling has a major impact on overall performance. This impact cannot be noticed during the first write to flash (since there is no need to erase blocks beforehand), but it is more and more noticeable as the flash media becomes full.

Static Wear-Leveling

Areas on the flash media may contain static files, characterized by blocks of data that remain unchanged for very long periods of time, or even for the whole device lifetime. If wear-leveling were only applied on newly written pages, static areas would never be cycled. This limited application of wear-leveling would lower life expectancy significantly in cases where flash memory contains large static areas. To overcome this problem, TrueFFS forces data transfer in static areas as well as in dynamic areas, thereby applying wear-leveling to the entire media.

6.4.7 Power Failure Management

TrueFFS uses algorithms based on "erase after write" instead of "erase before write" to ensure data integrity during normal operation and in the event of a power failure. Used areas are reclaimed for erasing and writing the flash management information into them only *after* an operation is complete. This procedure serves as a check on data integrity.

The "erase after write" algorithm is also used to update and store mapping information on the flash memory. This keeps the mapping information coherent even during power failures. The only mapping information held in RAM is a table pointing to the location of the actual mapping information. This table is reconstructed during power-up or after reset from the information stored in the flash memory.

To prevent data from being lost or corrupted, TrueFFS uses the following mechanisms:

- When writing, copying, or erasing the flash device, the data format remains valid at all intermediate stages. Previous data is never erased until the operation has been completed and the new data has been verified.
- A data sector cannot exist in a partially written state. The operation is either successfully completed, in which case the new sector contents are valid, or the operation has not yet been completed or has failed, in which case the old sector contents remain valid.

6.4.8 Error Detection/Correction

TrueFFS implements a unique MLC-tailored Error Correction Code (ECC) algorithm to ensure data reliability. Refer to Section 3.7 for further information on the EDC/ECC mechanism.

6.4.9 Special Features Through I/O Control (IOCTL) Mechanism

In addition to standard storage device functionality, the TrueFFS driver provides extended functionality. This functionality goes beyond simple data storage capabilities to include features such as: formatting the media, read/write protection, boot partition(s) access, flash defragmentation and other options. This unique functionality is available in all TrueFFS-based drivers through the standard I/O control command of the native file system.

6.4.10 Compatibility

DiskOnChip G3 LP requires TrueFFS driver 6.x or higher. Since this driver does not support DiskOnChip Plus products, migrating to DiskOnChip G3 LP requires changing the TrueFFS driver.

When using different drivers (e.g. TrueFFS SDK, BDK, SureFS, block device driver, etc.) to access DiskOnChip G3 LP, verify that all software is based on the same code base version. It is also important to use only tools (e.g. DFORMAT, DINFO, DIMAGE, etc.) from the same version as the TrueFFS drivers used in the application. Failure to do so may lead to unexpected results, such as lost or corrupted data. The driver version can be verified by the sign-on messages displayed, or by the version information presented by the driver or tool.

6.5 8KB Memory Window

TrueFFS utilizes an 8KB memory window in the CPU address space, consisting of four 2KB sections as depicted in Figure 12. When in Reset mode, read cycles from sections 1 and 2 always return the value 00H to create a fixed and known checksum. When in Normal mode, these two sections are used for the internal registers. The 2KB Programmable Boot Block is in section 0 and section 3, to support systems that search for a checksum at the boot stage both from the top and bottom of memory. The addresses described here are relative to the absolute starting address of the 8KB memory window.

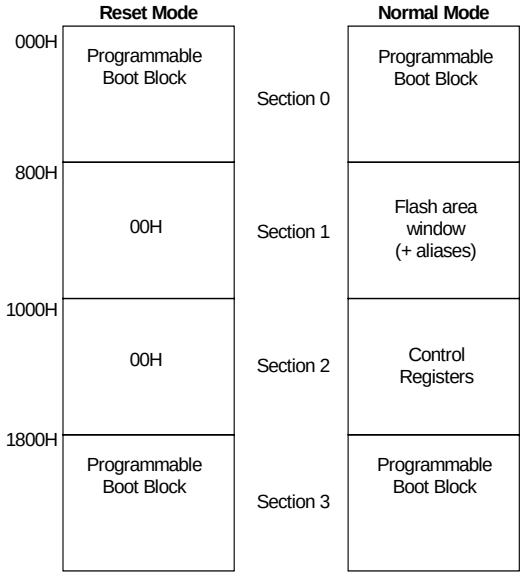


Figure 12: DiskOnChip G3 LP Memory Map

7. REGISTER DESCRIPTIONS

This section describes various DiskOnChip G3 LP registers and their functions, as listed in Table 3. Most DiskOnChip G3 registers are 8-bit, unless otherwise denoted as 16-bit.

Table 3: DiskOnChip G3 Registers

Address (Hex)	Register Name
0030	RAM page command
0070	RAM page Select
103E	No Operation (NOP)
1000/1074	Chip Identification [1:0]
1004	Test
1008	Endian Control
100C	DiskOnChip Control
1072	DiskOnChip Control Confirmation
100A	Device ID Select
100E	Configuration
1010	Interrupt Control
1020	Interrupt Status
1014	Output Control
107C	DPD Control
1078/107A	DMA Control [1:0]
101A	Read Address Register
1024	Virtual RAM status

7.1 Definition of Terms

The following abbreviations and terms are used within this section:

RFU — Reserved for future use. This bit is undefined during a read cycle and “don’t care” during a write cycle.

RFU_0 — Reserved for future use; when read, this bit always returns the value 0; when written, software should ensure that this bit is always set to 0.

RFU_1 — Reserved for future use; when read, this bit always returns the value 1; when written, software should ensure that this bit is always set to 1.

Reset Value — Refers to the value immediately present after exiting from Reset mode to Normal mode.

7.2 Reset Values

All registers return 00H while in Reset mode. The Reset value written in the register description is the register value after exiting Reset mode and entering Normal mode. Some register contents are undefined at that time (N/A).

7.3 RAM Page Command Register

Description: This 8-bit register is used to write the value 71H prior to writing to the RAM Page Select register.

Address (hex): 0030

Type: Write

	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write	W	W	W	W	W	W	W	W
Bit Name	COMMAND							
Reset Value	N/A							

Bit No.	Description
0-7	COMMAND The value 71H must be written to enable a subsequent write cycle to the RAM Page Select register. All other values: Reserved.

7.4 RAM Page Select Register

Description: This 8-bit register is used to initiate a download operation of the specified 1KB page. If the value 71H is not written to the RAM Page Command register immediately before to writing this register, the write cycle will be ignored. This register is writeable in Reset mode.

Address (hex): 0070

Type: Write

	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write	W	W	W	W	W	W	W	W
Description	SEQ	PAGE						
Reset Value	N/A	00H						

Bit No.	Description
7	SEQ (Sequential]). Setting this bit initiates a download from the NEXT_PAGE pointer of the previously downloaded page. The value written to the PAGE field is ignored.
0-6	PAGE. Specifies the page to load. Only significant when writing a 0 to the SEQ field. A PAGE value of 00H loads the same data as a hardware or software reset.

7.5 Read Address Register

Description: This 16-bit register is used to specify the next 13-bit address to be read from DiskOnChip G3 LP.

Address (hex): 101A

Type: Read/Write

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Description	INC	ONE_BYTE	RFU_0	REG_ADDR[12:8]				
Reset Value	0	0	0	See explanation below				

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Description	REG_ADDR[7:0]							
Reset Value	See explanation below							

Bit No.	Description
0-12	REG_ADDR[12:0]. Specifies the address of the register that will be read on the following read cycle. For 16-bit hosts, the LSB must be 0.
13	Reserved for future use.
14	ONE_BYTE. This bit is set when it is necessary to read/write only one byte of data from/to the Data Register. This bit is automatically cleared after the access to the Data register.
15	INC (Increment). **1**: After each read cycle, the address is incremented by 1 byte (when IF_CFG = 0) or by 1 word (when IF_CFG = 1). **0**: The address is not automatically incremented, and the same address may be read repeatedly.

7.6 No Operation (NOP) Register

Description: A call to this 16-bit register results in no operation. To aid in code readability and documentation, software should access this register when performing cycles intended to create a time delay.

Address (hex): 103E

Type: Write

Reset Value: None

7.7 Chip Identification (ID) Register [0:1]

Description: These two 16-bit registers are used to identify the DiskOnChip device residing on the host platform. They always return the same value.

Address (hex): 1000/1074

Type: Read only

Reset Value: Chip Identification Register[0]: 0200H

Chip Identification Register[1]: FDFFH

7.8 Test Register

Description: This register enables software to identify multiple DiskOnChip G3 LP devices or multiple aliases in the CPUs memory space. Data written is stored but does not affect the behavior of DiskOnChip G3 LP.

Address (hex): 1004

Type: Read/Write

Reset Value: 0

Bit No.	Description
7-0	D[7:0]: Data bits

7.9 Endian Control Register

Description: This 16-bit register is used to control the swapping of the low and high data bytes when reading or writing with a 16-bit host. This provides an Endian-independent method of enabling/disabling the byte swap feature.

Note: Hosts that support 8-bit access only do not need to write to this register.

Address (hex): 1008

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R							R/W
Description	RFU_0							SWAPL
Reset Value	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Read/Write	R							R/W
Description	RFU_0							SWAPH
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
0	SWAPL (Swap Low Byte): This bit must be set to enable byte swapping. If the bit is cleared, then byte swapping is disabled.
7-1	Reserved for future use.
8	SWAPH (Swap High Byte): This bit must be set to enable byte swapping. If the bit is cleared, then byte swapping is disabled.
15-9	Reserved for future use.

7.10 DiskOnChip Control Register/Control Confirmation Register

Description: These two registers are identical and contain information about the DiskOnChip G3 LP operational mode. After writing the required value to the DiskOnChip Control register, the complement of that data byte must also be written to the Control Confirmation register. The two writes cycles must not be separated by any other read or write cycles to the DiskOnChip G3 LP memory space, except for reads from the Programmable Boot Block space.

Address (hex): 100C/1072

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Description	RFU_0			RST_LAT	BDET	MDWREN	Mode[1:0]	
Reset Value	0	0	0	1	0	0	0	0

Note: The DiskOnChip Control Confirmation register is write only.

Bit No.	Description
1-0	Mode. These bits select the mode of operation, as follows: 00: Reset 01: Normal 10: Deep Power-Down
2	MDWREN (Mode Write Enable). The value 1 must be written to this bit when changing the mode of operation. It always returns 0 when read.
3	BDET (Boot Detect). This bit is set whenever the device has entered Reset mode as a result of the Boot Detector triggering. It is cleared by writing a 1 to this bit.
4	RST_LAT (Reset Latch). This bit is set whenever the device has entered the Reset mode as a result of the RSTIN# input signal being asserted or the internal voltage detector triggering. It is cleared by writing a 1 to this bit.
7-5	Reserved for future use.

7.11 Device ID Select Register

Description: In a cascaded configuration, this register controls which device provides the register space. The value of bits ID[0:1] is compared to the value of the ID configuration input balls. The device whose ID input matches the value of bits ID[0:1] responds to read and write cycles.

Address (hex): 100A

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R						R/W	
Description	RFU_0						ID[1:0]	
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
1-0	ID[1:0] (Identification). The device whose ID input balls match the value of bits ID[0:1] responds to read and write cycles to register space.
7-2	Reserved for future use.

7.12 Configuration Register

Description: This register indicates the current configuration of DiskOnChip G3 LP. Unless otherwise noted, the bits are reset only by a hardware reset, and not upon boot detection or any other entry to Reset mode.

Address (hex): 100E

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R		R/W		R			
Description	IF_CFG	RFU_0	MAX_ID		RFU	RFU_0		RFU_0
Reset Value	X	0	0	0	0	0	0	X

Bit No.	Description
5-4	MAX_ID (Maximum Device ID). This field controls the Programmable Boot Block address mapping when multiple devices are used in a cascaded configuration, using the ID[1:0] inputs. It should be programmed to the highest ID value that is found by software in order to map all available boot blocks into usable address spaces.
7	IF_CFG (Interface Configuration). Reflects the state of the IF_CFG input ball.

7.13 Interrupt Control Register

Description: This 16-bit register controls how interrupts are generated by DiskOnChip G3 LP, and indicates which of the following five sources has asserted an interrupt:

0: Flash array is ready

1: Data protection violation

2: Reading or writing more flash data than was expected

3: BCH ECC error detected (this feature is provided to support multi-page DMA transfers)

4: Completion of a DMA operation

Address (hex): 1010

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R		R/W					
Description	RFU_0		ENABLE					
Reset Value	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Read/Write	R/W							
Description	GMASK	EDGE	MASK					
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
5-0	ENABLE. For each bit in this field: **1**: Enables the respective bit in the STATUS field of the Interrupt Status register to latch activity and cause an interrupt if the corresponding MASK bit is set. **0**: Holds the respective bit in the STATUS field in the cleared state. To clear a pending interrupt and re-enable further interrupts on that channel, the respective ENABLE bit must be cleared and then set.
7-6	Reserved for future use.
13-8	MASK. For each bit in this field: **1**: Enables the respective bit in the STATUS field of the Interrupt Status register to generate an interrupt by asserting the IRQ# output. **0**: Prevents the respective STATUS bit from generating an interrupt.
14	EDGE. Selects edge or level triggered interrupts: **0**: Specifies level-sensitive interrupts in which the IRQ# output remains asserted until the interrupt is cleared. **1**: Specifies edge-sensitive interrupts in which the IRQ# output pulses low and return to logic 1.
15	GMASK (Global Mask). **1**: Enables the IRQ# output to be asserted. Setting this bit while one or more interrupts are pending will generate an interrupt. **0**: Forces the IRQ# output to the negated state.

7.14 Interrupt Status Register

Description: This register indicates which interrupt source created an interrupt.

Address (hex): 1020

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R		R/W					
Description	RFU_0		STATUS					
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
5-0	STATUS. Indicates which interrupt sources created an interrupt. For a list of the interrupt sources, please refer to the description of the Interrupt Control register.
7-6	Reserved for future use.

7.15 Output Control Register

Description: This register controls the behavior of certain output signals. This register is reset by a hardware reset, not by entering Reset mode.

Note: When multiple devices are cascaded, writing to this register will affect all devices regardless of the value of the ID[1:0] inputs.

Address (hex): 1014

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R					R/W		
Description	RFU_0					Turbo	PU_DIS	BUSY_EN
Reset Value	0	0	0	0	0	0	0	1

Bit No.	Description
0	BUSY_EN (Busy Enable). Controls the assertion of the BUSY# output during a download initiated by a soft reset. **1**: Enables the assertion of the BUSY# output **0**: Disables the assertion of the BUSY# output Upon the assertion of the RSTIN# input, this bit will be set automatically and the BUSY# output signal will be asserted until the completion of the download process.
1	PU_DIS (Pull-Up Disable). Controls the pull-up resistors D[15:8] as follows: **1**: Always disable the pull-ups **0**: Enable the pull-ups when IF_CFG = 0
2	TURBO. Activates turbo operation. **0**: DiskOnChip is used in normal operation, without improved access time. Output buffers are enabled only after a long enough delay to guarantee that there will be no more than a single transition on each bit. **1**. DiskOnChip is used in Turbo operation. Output buffers are enabled immediately after the assertion of OE# and CE#, resulting in improved access time. Read cycles from the Programmable Boot Block may result in additional noise and power dissipation due to multiple transitions on the data bus.
7-3	Reserved for future use.

7.16 DPD Control Register

Description: This register specifies the behavior of the DPD input signal.

Address (hex): 107C

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R				R/W			
Description	PD_OK	RFU_0			MODE[0:3]			
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
3-0	MODE[0:3]. Controls the behavior of the DPD input: 0000: DPD input is not used to control DPD mode 0001: DPD mode exited on rising edge of DPD input 0010: DPD mode exited on falling edge of DPD input 0100: DPD mode is entered when DPD=1 and exited when DPD=0 1000: DPD mode is entered when DPD=0 and exited when DPD=1
6-4	Reserved for future use.
7	PD_OK (Power- Down OK). This read-only bit indicates that it is currently possible to put DiskOnChip G3 LP in Deep Power-Down mode.

7.17 DMA Control Register [1:0]

Description: These two 16-bit registers specify the behavior of the DMA operation.

Address (hex): 1078/107A

DMA Control Register [o]								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Read/Write	R	R/W						
Description	RFU_0	SECTOR_COUNT						
Reset Value	0	0	0	0	0	0	0	0

	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Read/Write	R	R/W			R			
Description	DMA_EN	PAUSE	EDGE	POLRTY	RFU_0			
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
6-0	SECTOR_COUNT. Specifies the number of 512-byte sectors to be transferred plus one. Writing a value of 0 indicates a transfer of one sector. Reading a value of 0 indicates that there is still one sector to be transferred). This field is decremented by DiskOnChip G3 after reading the ECC checksum from each sector. In the event of an ECC error, this field indicates the number of sectors remaining to be transferred.
11-7	Reserved for future use.
12	POLRTY (Polarity). Specifies the polarity of the DMARQ# output: **0**: DMARQ# is normally logic -1 and falls to initiate DMA **1**: DMARQ# is normally logic -0 and rises to initiate DMA
13	EDGE. Controls the behavior of the DMARQ# output: **1**: DMARQ# pulses to the asserted state for 250 nS (typical) to initiate the block transfer. **0**: DMARQ# switches to the active state to initiate the block transfer and returns to the negated state at the beginning of the cycle in which the DCNT field of the ECC Control register[0] reaches the value specified by the NEGATE_COUNT field of the DMA Control register[1].
14	PAUSE. This bit is set in the event of an ECC error during a DMA operation. After reading the ECC parity registers and correcting the errors, the software must clear this bit to resume the DMA operation.
15	DMA_EN (DMA Enable). Setting this bit enables DMA operation.

DMA Control Register [1]								
	Bits 15-10				**Bits 9-0**			
Read/Write	R				R/W			
Description	RFU_0				NEGATE_COUNT			
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
9-0	NEGATE_COUNT. When the EDGE bit of the DMA Control register[0] is 0, this field must be programmed to specify the bus cycle in which DMARQ# will be negated, as follows: NEGATE_COUNT = BYTES_REMAINING + 16 + BYTES_PER_CYCLE. Example: To negate DMARQ# at the beginning of the cycle in which the last word is to be transferred by a 16-bit host: NEGATE_COUNT = 2 + 16 + 2 = 20.
15-10	Reserved for future use.

7.18 Virtual RAM Status Register

Description: This 8-bit register indicates the value of the VIRTUAL_RAM_MODE byte download from the flash. This register is writeable in Reset mode

Address (hex): 1024

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R	R	R	R	R	R	R	R
Description	VRS	RFU_0					RFU	RFU
Reset Value	1	0	0	0	0	0	Varies	Varies

Bit No.	Description
6-0	Reserved for future use.
7	VRS (Virtual RAM Supported). This read-only bit returns 1 to indicate a device that supports Virtual RAM mode. The bit can be used to distinguish between DiskOnChip G3 LP and DiskOnChip G3, which returns 0 in this bit.

DMA Control Register [1]								
	Bits 15-10				Bits 9-0			
Read/Write	R				R/W			
Description	RFU_0				NEGATE_COUNT			
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
9-0	NEGATE_COUNT. When the EDGE bit of the DMA Control register[0] is 0, this field must be programmed to specify the bus cycle in which DMARQ# will be negated, as follows: NEGATE_COUNT = BYTES_REMAINING + 16 + BYTES_PER_CYCLE. Example: To negate DMARQ# at the beginning of the cycle in which the last word is to be transferred by a 16-bit host: NEGATE_COUNT = 2 + 16 + 2 = 20.
15-10	Reserved for future use.

8. BOOTING FROM DISKONCHIP G3 LP

8.1 Introduction

DiskOnChip G3 LP can function both as a flash disk and as the system boot device. If DiskOnChip G3 is configured as a flash disk and as the system boot device, it contains the boot loader, an OS image and a file system. In such a configuration, DiskOnChip G3 LP can serve as the only non-volatile device on board. Refer to Section 8.2.1 for further information on boot replacement.

8.2 Boot Replacement

8.2.1 Non-PC Architectures

In non-PC architectures, the boot code is executed from a boot ROM, and the drivers are usually loaded from the storage device.

When using DiskOnChip G3 LP as the system boot device, the CPU fetches the first instructions from the DiskOnChip G3 LP Programmable Boot Block, which contains the IPL. Since in most cases this block cannot hold the entire boot loader, the IPL runs minimum initialization, after which the Secondary Program Loader (SPL) is copied to RAM from flash. The remainder of the boot loader code then runs from RAM.

The SPL is located in a separate (binary) partition on DiskOnChip G3 LP, and can be hardware protected if required. .

8.2.2 Asynchronous Boot Mode

Platforms that host CPUs that wake up in MultiBurst mode should use Asynchronous Boot mode when using DiskOnChip G3 LP as the system boot device.

During platform initialization, certain CPUs wake up in 32-bit mode and issue instruction fetch cycles continuously. An XScale CPU, for example, initiates a 16-bit read cycle, but after the first word is read, it continues to hold CE# and OE# asserted while it increments the address and reads additional data as a burst. A StrongARM CPU wakes up in 32-bit mode and issues double-word instruction fetch cycles.

Once in Asynchronous Boot mode, the CPU can fetch its instruction cycles from the DiskOnChip G3 LP Programmable Boot Block. After reading from this block and completing boot, DiskOnChip G3 LP returns to derive its internal clock signal from the CE#, OE#, and WE# inputs. Please refer to Section 10.3 for read timing specifications for Asynchronous Boot mode.

8.2.2.1 Virtual RAM Boot

The Virtual RAM Boot feature utilizes the 2KB physical IPL SRAM to provide XIP access to up to 8KB of flash data, without requiring any prior knowledge of the device architecture. This feature can be used to support the Secure Boot requirements of the TI OMAP processor family. The Virtual RAM Boot feature is intended for platforms that support the DiskOnChip G3 LP BUSY# output.

When DiskOnChip G3 LP is configured with the Virtual RAM Boot feature active, DiskOnChip remains in virtual RAM whenever it is in Reset mode. While in this mode, read cycles from the entire DiskOnChip 8KB memory window return virtual RAM data. Access to an address that is not the physical 2KB SRAM initiates a download operation in which the required data is copied from

the NAND flash to the physical SRAM. The DiskOnChip BUSY# output is asserted for the duration of the download, holding the platform in a wait state. The download is transparent to software, and XIP and random access from any location within the 8KB virtual address space are therefore supported. The platform must be capable of being held in a wait state for an arbitrary period during each download process, without interference from watchdog timers.

For more information on how to boot from DiskOnChip G3 LP in Virtual RAM Boot mode, please contact your local M-Systems sales office

8.2.2.2 Paged RAM Boot

The Paged RAM Boot feature separates the 2KB IPL SRAM into two 1KB sections. The first section provides constant data, while the other section can be downloaded with flash data. One application of this feature is to support the Secure Boot requirements of the TI OMAP processor family. The Paged RAM Boot feature does not support XIP (unlike the Virtual RAM Boot feature), but also does not require support of the BUSY# output.

After a hardware or software reset, DiskOnChip G3 LP initializes the first 2KB of RAM from data stored in a fixed location on DiskOnChip G3 LP. The Paged RAM Boot feature permits 1KB of the internal SRAM to be downloaded upon receiving a command sequence from one of many 1KB virtual pages (up to 14 sections of 1KB). Since the DiskOnChip G3 LP BUSY# output is not asserted by a page-load operation, a polling procedure is required to determine when the download is complete. XIP operations from the DiskOnChip G3 LP RAM are not supported during this polling operation, and so must be executed instead from system RAM or ROM.

Normally, the data in the first 1KB of RAM is fixed, while the second 1 KB is downloaded upon command.

To support platforms that boot from the top rather than the bottom of memory, DiskOnChip G3 LP can be configured with an alternate memory map where the top 1KB of the DiskOnChip G3 LP address space returns fixed RAM data, while the 1KB below that is downloadable.

When multiple DiskOnChip G3 LP devices are cascaded, Paged RAM downloads occur only on the first DiskOnChip in the cascaded configuration (device-0). The other cascaded devices move to Reset mode when a Paged RAM download is initiated.

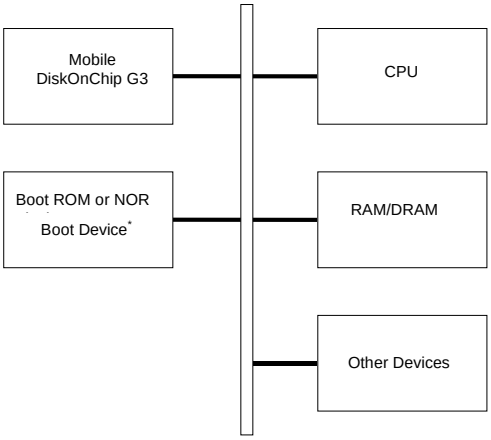
For more information on booting from DiskOnChip G3 LP in Paged RAM Boot mode, please contact your local M-Systems sales office

9. DESIGN CONSIDERATIONS

9.1 General Guidelines

A typical RISC processor memory architecture is shown in Figure 13. It may include the following devices:

- **DiskOnChip G3 LP**: Contains the OS image, applications, registry entries, back-up data, user files and data, etc. It can also be used to perform boot operation, thereby replacing the need for a separate boot device.
- **CPU**: DiskOnChip G3 LP is compatible with all major CPUs in the mobile phone, Digital TV (DTV) and Digital Still Camera (DSC) markets, including:
  - ARM-based CPUs
  - Texas Instruments DM270, OMAP family
  - Intel XScale, Bulverde
  - ADI 652x family
  - Infineon EGold and SGold
  - Freescale i.250, Dragon Ball MX family
  - Emblaze ER4525 application processor
  - Renesas SH mobile
  - SuperH SH-3/4
- **Boot Device**: ROM or NOR flash that contains the boot code required for system initialization, kernel relocation, loading the operating systems and/or other applications and files into the RAM and executing them.
- **RAM/DRAM Memory**: This memory is used for code execution.
- **Other Devices**: A DSP processor, for example, may be used in a RISC architecture for enhanced multimedia support.

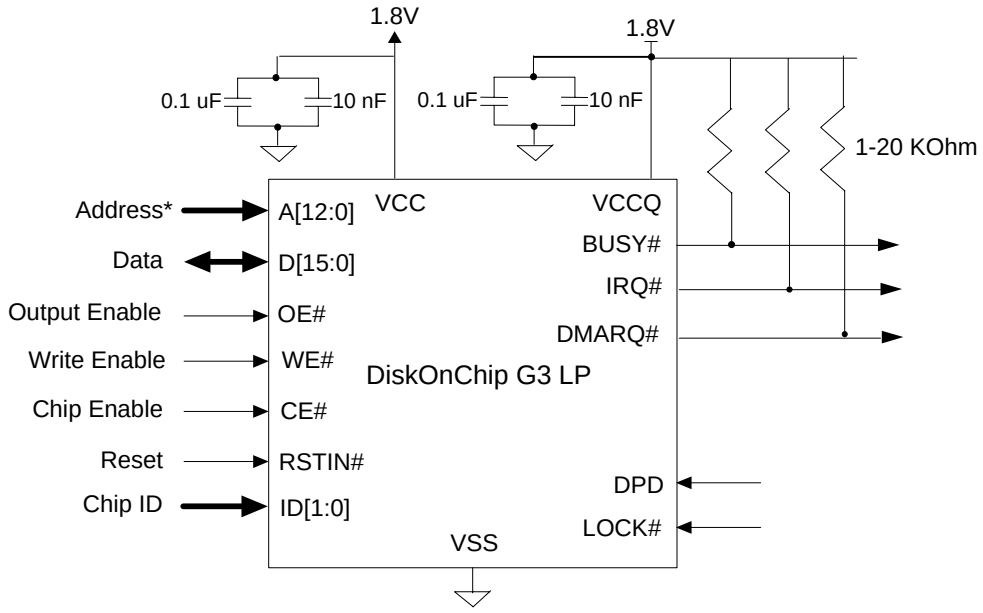


When used as a boot device, DiskOnChip G3 LP eliminates the need for a dedicated boot ROM/NOR device.

Figure 13: Typical System Architecture Using DiskOnChip G3 LP

9.2 Standard NOR-Like Interface

DiskOnChip G3 LP uses a NOR-like interface that can easily be connected to any microprocessor bus. With a standard interface, it requires 13 address lines, 8 data lines and basic memory control signals (CE#, OE#, WE#), as shown in Figure 14 below. Typically, DiskOnChip G3 can be mapped to any free 8KB memory space. In a PC-compatible platform, it is usually mapped into the BIOS expansion area. If the allocated memory window is larger than 8KB, an automatic anti-aliasing mechanism prevents the firmware from being loaded more than once during the ROM expansion search.



(*) Address A0 is multiplexed with the DPD signal.

Figure 14: Standard System Interface

Notes: 1. The 0.1 µF and the 10 nF low-inductance, high-frequency capacitors must be attached to each of the device's VCC and VSS balls. These capacitors must be placed as close as possible to the package leads.

2. DiskOnChip G3 LP is an edge-sensitive device. CE#, OE#, and WE# should be properly terminated (according to board layout, serial parallel or both terminations) to avoid signal ringing.

9.3 Multiplexed Interface

With a multiplexed interface, DiskOnChip G3 LP requires the signals shown in Figure 15 below.

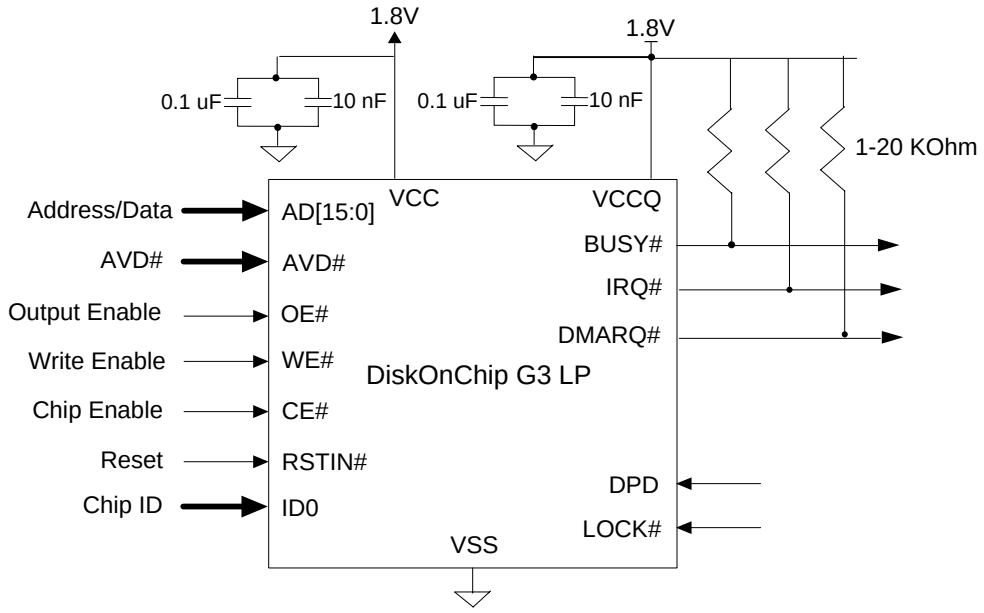


Figure 15: Multiplexed System Interface

9.4 Connecting Control Signals

9.4.1 Standard Interface

When using a standard NOR-like interface, connect the control signals as follows:

- A[12:0] – Connect these signals to the host's address signals (see Section 9.8 for platform-related considerations). Address signal A[0] is multiplexed with the DPD signal.
- D[15:0] – Connect these signals to the host's data signals (see Section 9.8 for platform-related considerations).
- Output Enable (OE#) and Write Enable (WE#) – Connect these signals to the host RD# and WR# signals, respectively.
- Chip Enable (CE#) – Connect this signal to the memory address decoder. Most RISC processors include a programmable decoder to generate various Chip Select (CS) outputs for different memory zones. These CS signals can be programmed to support different wait states to accommodate DiskOnChip G3 timing specifications.
- Power-On Reset In (RSTIN#) – Connect this signal to the host active-low Power-On Reset signal.
- Chip Identification (ID[1:0]) – Connect these signals as shown in Figure 14. Both signals must be connected to VSS if the host uses only one DiskOnChip. If more than one device is being used, refer to Section 9.6 for more information on device cascading.

- Busy (BUSY#) – This signal indicates when the device is ready for first access after reset. It may be connected to an input port of the host, or alternatively it may be used to hold the host in a wait-state condition. The later option is required for hosts that boot from DiskOnChip G3 LP.
- DMARQ# (DMA Request) – Output used to control multi-page DMA operations. Connect this output to the DMA controller of the host platform.
- IRQ# (Interrupt Request) – Connect this signal to the host interrupt.
- Lock (LOCK#) – Connect to a logical **0** to prevent the usage of the protection key to open a protected partition. Connect to logical **1** in order to enable usage of protection keys.
- Deep-Power Down (DPD) – multiplexed with A[0].
- 8/16 Bit Interface Configuration (IF_CFG) – This signal is required for configuring the device for 8- or 16-bit access mode. When negated, the device is configured for 8-bit access mode. When asserted, 16-bit access mode is operative.

9.4.2 Multiplexed Interface

DiskOnChip G3 LP can use a multiplexed interface to connect to the multiplexed bus (asynchronous read/write protocol). In this configuration, the ID[1] input is driven by the host's AVD# signal, and the D[15:0] balls, used for both address inputs and data, are connected to the host AD[15:0] bus. As with a standard interface, only address bits [12:0] are significant.

This mode is automatically entered when a falling edge is detected on ID[1]. This edge must occur after RSTIN# is negated and before OE# and CE# are both asserted; i.e., the first read cycle made to DiskOnChip must observe the multiplexed mode protocol. See Section 10.3 for more information about the related timing requirements.

Please refer to Section 2.3 for ballout and signal descriptions, and to Section 10.3 for timing specifications for a multiplexed interface.

9.5 Implementing the Interrupt Mechanism

9.5.1 Hardware Configuration

To configure the hardware for working with the interrupt mechanism, connect the IRQ# ball to the host interrupt input.

Note: A nominal 10 KΩ pull-up resistor must be connected to this ball.

9.5.2 Software Configuration

Configuring the software to support the IRQ# interrupt is performed in two stages.

Stage 1

Configure the software so that when the system is initialized, the following steps occur:

1. The correct value is written to the Interrupt Control register to configure DiskOnChip G3 for:
   - Interrupt source: Flash ready, data protection, last byte during DMA has been transferred, or BCH ECC error has been detected (used during multi-page DMA operations).
   - Output sensitivity: Either edge or level-triggered

   Note: Refer to Section 7 for further information on the value to write to this register.
2. The host interrupt is configured to the selected input sensitivity, either edge or level-triggered.
3. The handshake mechanism between the interrupt handler and the OS is initialized.
4. The interrupt service routine to the host interrupt is connected and enabled.

Stage 2

Configure the software so that for every long flash I/O operation, the following steps occur:

1. The correct value is written to the Interrupt Control register to enable the IRQ# interrupt.

   Note: Refer to Section 7 for further information on the value to write to this register.
2. The flash I/O operation starts.
3. Control is returned to the OS to continue other tasks. When the IRQ# interrupt is received, other interrupts are disabled and the OS is flagged.
4. The OS either returns control immediately to the TrueFFS driver, or waits for the appropriate condition to return control to the TrueFFS driver.

9.6 Device Cascading

When connecting DiskOnChip G3 LP 64MB (512Mb) using a standard interface, up to four devices can be cascaded with no external decoding circuitry. Figure 16 illustrates the configuration required to cascade four devices on the host bus (only the relevant cascading signals are included in this figure, although all other signals must also be connected). All balls of the cascaded devices must be wired in common, except for ID0 and ID1. The ID input balls are strapped to VCC or VSS, according to the location of each DiskOnChip. The ID ball values determine the identity of each device. For example, the first device is identified by connecting the ID balls as 00, and the last device by connecting the ID balls as 11. Systems that use only one DiskOnChip G3 64MB (512Mb) must connect the ID balls as 00. Additional devices must be configured consecutively as 01, 10, and 11.

When DiskOnChip G3 LP 64MB (512Mb) uses a multiplexed interface, the value of ID[1] is set to logic 0. Therefore, only two devices can be cascaded using ID[0].

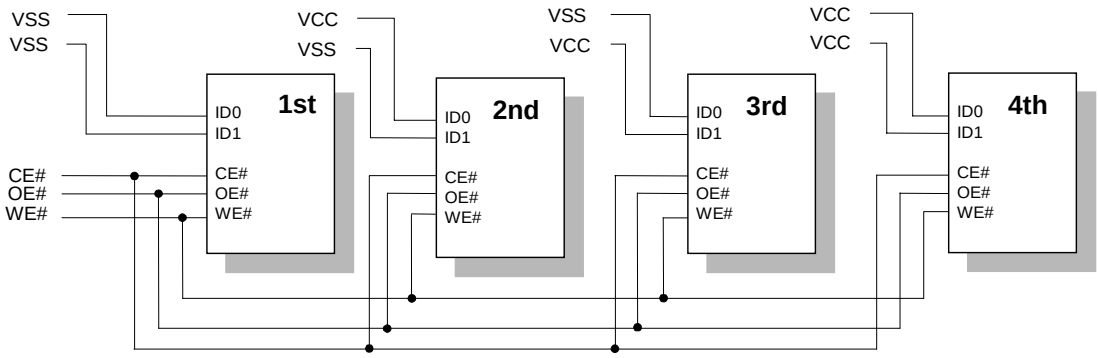


Figure 16: Standard Interface, Cascaded Configuration

Note: When more than one DiskOnChip G3 LP is cascaded, a boot block of 4KB is available. The Programmable Boot Block of each device is mapped to a unique address space.

9.7 Boot Replacement

A typical RISC architecture uses a boot ROM for system initialization. The boot ROM is also required to access DiskOnChip G3 LP during the boot sequence in order to load OS images and the device drivers.

M-Systems' Boot Software Development Kit (BDK) and DOS utilities enable full control of DiskOnChip G3 during the boot sequence. For a complete description of these products, refer to the *DiskOnChip Boot Software Development Kit (BDK)* developer guide and the *DiskOnChip Software Utilities* user manual. These tools enable the following operations:

- Formatting DiskOnChip G3 LP Creating multiple partitions for different storage needs (OS image files, registry entry files, backup partitions, and FAT partitions)
- Loading the OS image file

Figure 17 illustrates the system boot flow using DiskOnChip G3 LP in a RISC architecture.

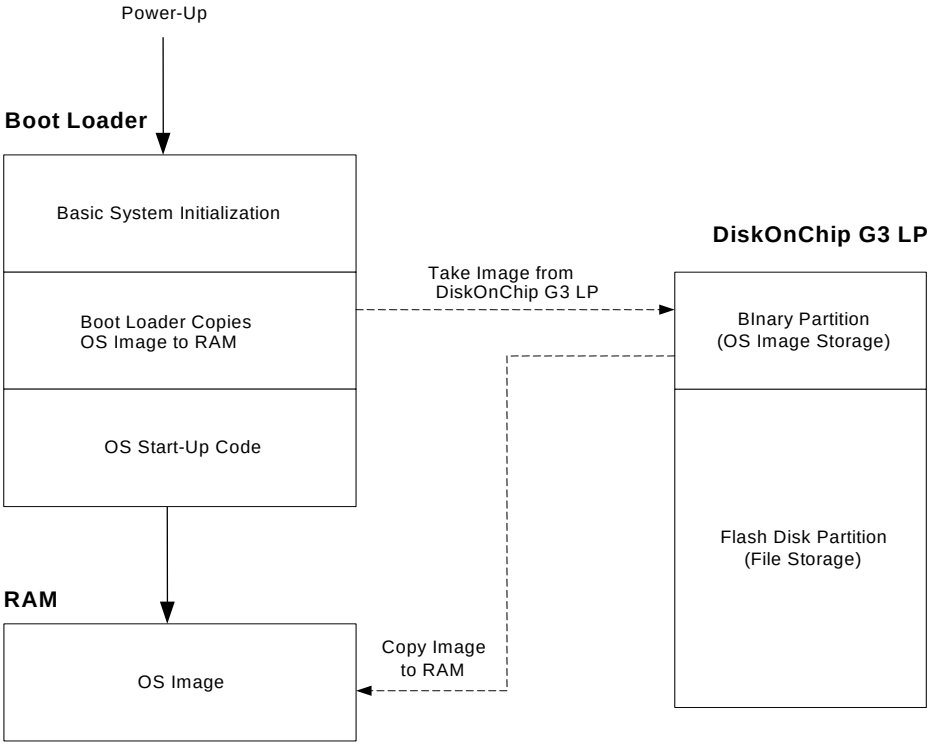


Figure 17: System Boot Flow with DiskOnChip G3 LP

9.8 Platform-Specific Issues

This section discusses hardware design issues for major embedded RISC processor families.

9.8.1 Wait State

Wait states can be implemented only when DiskOnChip G3 LP is designed in a bus that supports a Wait state insertion, and supplies a WAIT signal.

9.8.2 Big and Little Endian Systems

DiskOnChip G3 is a Little Endian device. Therefore, byte lane 0 (D[7:0]) is its Least Significant Byte (LSB) and byte lane 1 (D[15:8]) is its Most Significant Byte (MSB). Within the byte lanes, bit D0 and bit D8 are the least significant bits of their respective byte lanes. DiskOnChip G3 can be connected to a Big Endian device in one of two ways:

1. Make sure to identify byte lane 0 and byte lane 1 of your processor. Then, connect the data bus so that the byte lanes of the CPU match the byte lanes of DiskOnChip G3 LP. Pay special attention to processors that also change the bit ordering within the bytes (for example, PowerPC). Failing to follow these rules results in improper connection of DiskOnChip G3 LP, and prevents the TrueFFS driver from identifying it.
2. Set the bits SWAPH and SWAPL in the Endian Control register. This enables byte swapping when used with 16-bit hosts.

9.8.3 Busy Signal

The Busy signal (BUSY#) indicates that DiskOnChip G3 LP has not yet completed internal initialization. After reset, BUSY# is asserted while the IPL is downloaded into the internal boot block and the Data Protection Structures (DPS) are downloaded to the Protection State Machines. Once the download process is completed, BUSY# is negated. It can be used to delay the first access to DiskOnChip G3 LP until it is ready to accept valid cycles.

Note: DiskOnChip G3 LP does NOT use this signal to indicate that the flash is in busy state (e.g. program, read, or erase).

9.8.4 Working with 8/16/32-Bit Systems

DiskOnChip G3 LP uses a 16-bit data bus and supports 16-bit data access by default. However, it can be configured to support 8 or 32-bit data access mode. This section describes the connections required for each mode.

The default of the TrueFFS driver for DiskOnChip G3 LP is set to work in 16-bit mode. It must be specially configured to support 8 and 32-bit mode. Please see TrueFFS documentation for further details.

Note: The DiskOnChip data bus must be connected to the Least Significant Bits (LSB) of the system. The system engineer must verify whether the matching host signals are SD[7:0], SD[15:8] or D[31:24].

8-Bit (Byte) Data Access Mode

When configured for 8-bit operation, ball IF_CFG should be connected to VSS, and data lines D[15:8] are internally pulled up and may be left unconnected. The controller routes odd and even address accesses to the appropriate byte lane of the flash and RAM.

Host address SA0 must be connected to DiskOnChip G3 LP A0, SA1 must be connected to A1, etc.

16-Bit (Word) Data Access Mode

To set DiskOnChip G3 LP to work in 16-bit mode, the IF_CFG ball must be connected to VCC.

In 16-bit mode, the Programmable Boot Block is accessed as a true 16-bit device. It responds with the appropriate data when the CPU issues either an 8-bit or 16-bit read cycle. The flash area is accessed as a 16/32-bit device, regardless of the interface bus width. This has no affect on the design of the interface between DiskOnChip G3 LP and the host. The TrueFFS driver handles all issues regarding moving data in and out of DiskOnChip G3 LP.

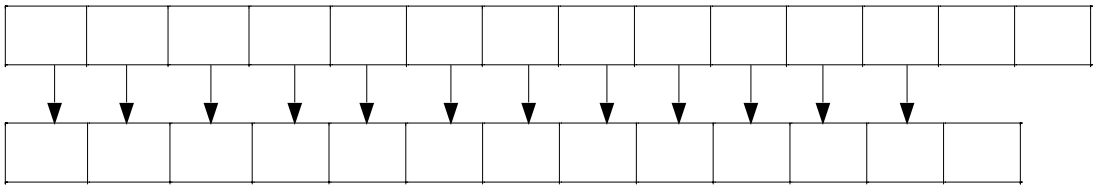
See Table 4 for A0 and IF_CFG settings for various functionalities with 8/16-bit data access.

Table 4: Active Data Bus Lines in 8/16-Bit Configuration

A0	IF_CFG	Functionality
0	1	16-bit access through both buses
0	0	8-bit access to even bytes through low 8-bit bus
1	0	8-bit access to odd bytes through low 8-bit bus
1	1	Illegal

32-Bit (Double Word) Data Access Mode

In a 32-bit bus system that cannot execute byte- or word-aligned accesses, the system address lines SA0 and SA1 are always 0. Consecutive double words (32-bit words) are differentiated by SA2 toggling. Therefore, in 32-bit systems that support only 32-bit data access cycles, DiskOnChip G3 LP signal A0 is connected to VSS and A1 is connected to the first system address bit that toggles; i.e., SA2.



Note: The prefix “S” indicates system host address lines

Figure 18: Address Shift Configuration for 32-Bit Data Access Mode

9.9 Design Environment

DiskOnChip G3 LP provides a complete design environment consisting of:

- Evaluation boards (EVBs) for enabling software integration and development with DiskOnChip G3, even before the target platform is available.
- Programming solutions:
  - GANG programmer
  - Programming house
  - On-board programming
- TrueFFS Software Development Kit (SDK) and Boot Software Development Kit (BDK)
- Support for various JTAG companies
- DOS and XP utilities:
  - DFORMAT
  - DIMAGE
  - DINFO
- Documentation:
  - Data sheet
  - Application notes
  - Technical notes
  - Articles
  - White papers

Please visit the M-Systems website (www.m-systems.com) for the most updated documentation, utilities and drivers.

10. PRODUCT SPECIFICATIONS

10.1 Environmental Specifications

10.1.1 Operating Temperature

Extended temperature range: -40°C to +85°C

10.1.2 Thermal Characteristics

Table 5: Thermal Characteristics

Thermal Resistance (°C/W)	
Junction to Case (θ_{JC}): 30	Junction to Ambient (θ_{JA}): 85

10.1.3 Humidity

10% to 90% relative, non-condensing

10.1.4 Endurance

DiskOnChip G3 LP is based on MLC NAND flash technology, which guarantees a minimum of 100,000 erase cycles. Due to the TrueFFS wear-leveling algorithm, the life span of all DiskOnChip products is significantly prolonged. M-Systems' website (www.m-systems.com) provides an online life-span calculator to facilitate application-specific endurance calculations.

10.2 Electrical Specifications

10.2.1 Absolute Maximum Ratings

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Rating1	Unit
VCC	DC core supply voltage	-0.6 to 4.6	V
VCCQ	DC I/O supply voltage	-0.6 to 4.6	V
$T_{1SUPPLY}$	Maximum duration of applying VCCQ without VCC, or VCC without VCCQ	1000	msec
I_{IN}	Input ball current (25 °C)	-10 to 10	mA
V_{IN}[2]	Input ball voltage	-0.6 to VCCQ+0.3V, 4.6V max	V
T_{STG}	Storage temperature	-55 to 150	°C
ESD: Charged Device Model	ESD_{CDM}	1000	V
ESD: Human Body Model	ESD_{HBM}	2000	V

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The voltage on any ball may undershoot to -2.0 V or overshoot to 6.6V for less than 20 ns.
3. When operating DiskOnChip G3 LP with separate power supplies for VCC and VCCQ, it is recommended to turn both supplies on and off simultaneously. Providing power separately (either at power-on or power-off) can cause excessive power dissipation. Damage to the device may result if this condition persists for more than 1 second.

10.2.2 Capacitance

Table 7: Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input capacitance (64MB/512Mb device)	V_{IN} = 0V		TBD	10	pF
C_{OUT}	Output capacitance (64MB/512Mb device)	V_O = 0V		TBD	10	pF

Capacitance is not 100% tested.

10.2.3 DC Electrical Characteristics over Operating Range

See Table 8 for DC characteristics for VCC=VCCQ ranges 1.65-1.95V

Table 8: DC Characteristics, VCCQ = 1.65-1.95V I/O

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC	Core supply voltage		1.65	1.8	1.95	V
VCCQ	Input/Output supply voltage		1.65	1.8	1.95	V
V_{IH}	High-level input voltage		VCCQ – 0.4			V
V_{IL}	Low-level input voltage				0.4	V
V_{OH}	High-level output voltage	I_{OH} = -100 µA	VCCQ – 0.1			V
V_{OL}	Low-level output voltage	D[15:0] I_{OL} = 100 µA			0.1	V
		Iol = 4 mA ,IRQ#, BUSY#, DMARQ# 4 mA			0.3	V
I_{ILK}	Input leakage current[2,3] (64MB/512Mb device)				±10	µA
I_{IOLK}	Output leakage current (64MB/512Mb device)				±10	µA
I_{CC}	Active supply current[1]	Read Program Erase Cycle Time = 100 ns		4.2 9.2 9.2	35	mA
I_{CCS}	Standby supply current, (64MB/512Mb device)	Deep Power-Down mode[3]		4	40	µA
		Non Deep Power-Down mode and CE# = VCCQ, All other inputs 0V or VCCQ		350	600	µA
I_{CCQS}	Standby supply current VCCQ	All inputs are VCCQ or 0v		1.7	6	µA

1. VCC = 3V, VCCQ = 1.8V, Outputs open
2. The CE# input includes a pull-up resistor which sources 0.3~1.4 (TBD) uA at Vin=0V
3. Deep Power-Down mode is achieved by asserting RSTIN# (when in Normal mode) or writing the proper write sequence to the DiskOnChip registers, and asserting the CE# input = VCCQ.

10.2.4 AC Operating Conditions

Timing specifications are based on the conditions defined below.

Table 9: AC Characteristics

Parameter	VCCQ = 1.65-1.95V
Ambient temperature (TA)	-40°C to +85°C
Core supply voltage (VCC)	1.65~1.95V
Input pulse levels	0.2/VCCQ-0.2V
Input rise and fall times	3 ns
Input timing levels	0.9V
Output timing levels	0.9V
Output load	30 pF

10.3 Timing Specifications

10.3.1 Read Cycle Timing Standard Interface

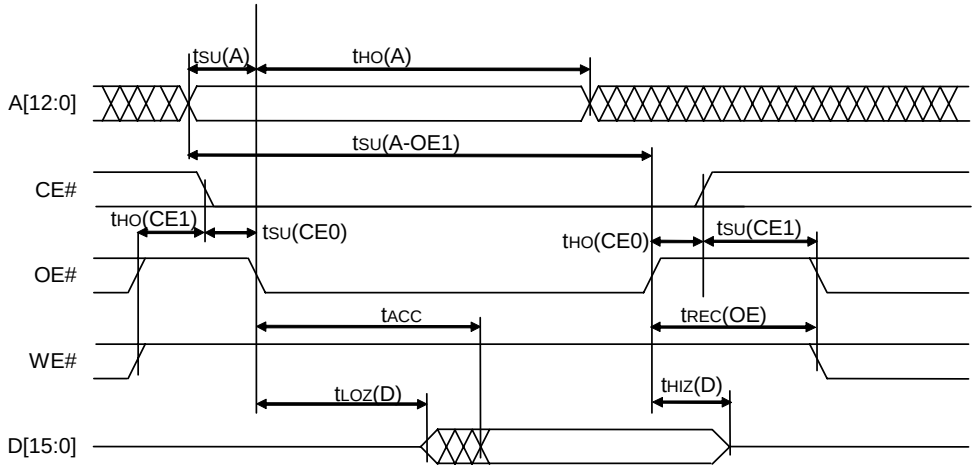


Figure 19: Standard Interface, Read Cycle Timing

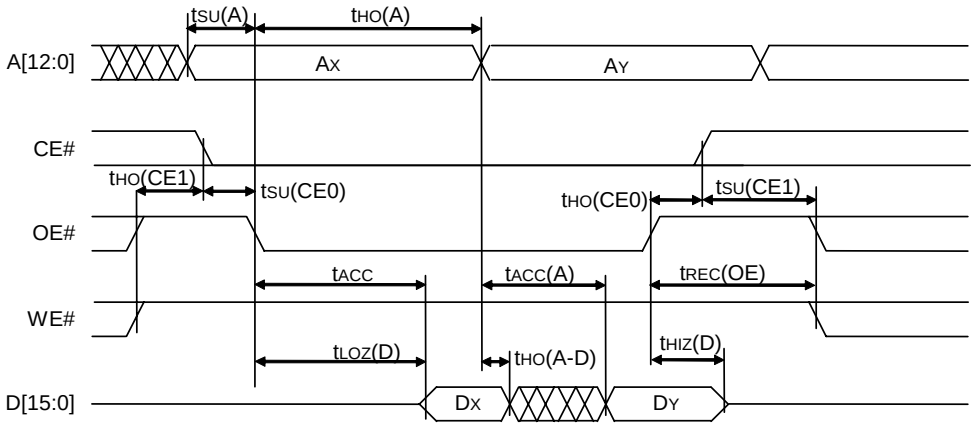


Figure 20: Standard Interface Read Cycle Timing – Asynchronous Boot Mode

Table 10: Standard Interface Read Cycle Timing Parameters

Symbol	Description		VCC= VCCQ=1.65-1.95V		Units
			Min	Max	
Tsu(A)	Address to OE# ↓ setup time[1]		-10		ns
Tho(A)	OE# ↓ to Address hold time[5]		48		ns
Tsu(CE0)	CE# ↓ to OE# ↓ setup time[1]		—		ns
Tho(CE0)	OE# ↑ to CE# ↑ hold time[2]		—		ns
Tho(CE1)	OE# or WE# ↑ to CE# ↓ hold time		5		ns
Tsu(CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time		5		ns
Trec(OE)	OE# negated to start of next cycle[2]		20		ns
Tacc	Read access time (RAM)[1, 4]			103	ns
	Read access time (all other addresses)[1]			52	
Tloz(D)	OE# ↓ to D driven[4]		17		ns
Thiz(D)	OE# ↑ to D Hi-Z delay[3,6]			22	ns
tacc(A)	RAM Read access time from A[9:0]	Asynchronous Boot mode		83	ns
tho(A-D)	Data hold time from A[9:0] (RAM)	Asynchronous Boot mode	TBD		ns

1. CE# may be asserted any time before or after OE# is asserted. If CE# is asserted after OE#, all timing relative to OE# asserted will be referenced instead to the time of CE# asserted.
2. CE# may be negated any time before or after OE# is negated. If CE# is negated before OE#, all timing relative to OE# negated will be referenced instead to the time of CE# negated.
3. No load (CL = 0 pF).
4. Access time 750 ns on the first read cycle when exiting Deep Power-Down mode if correct data is required from the RAM. See Section 6.3 for more information
5. For RAM read cycles, the address must be held valid until after the data is latched by the host.
6. Does not include output buffer Hi-Z delay (**TBD**).

10.3.2 Write Cycle Timing Standard Interface

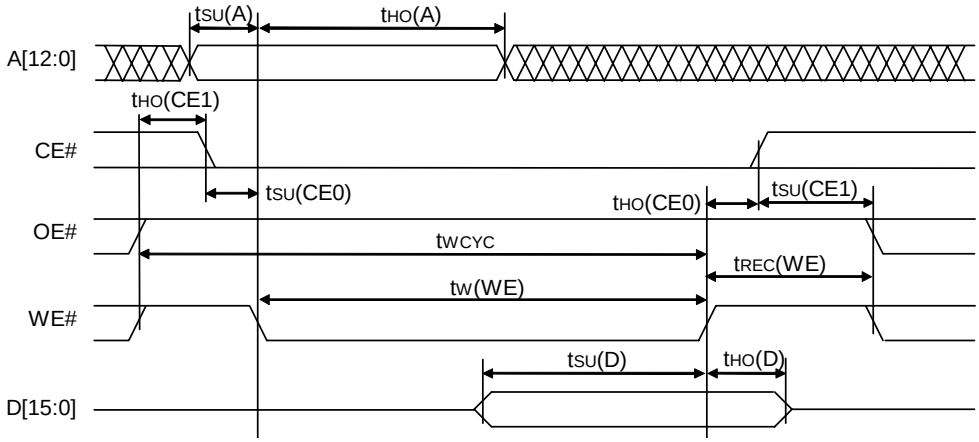


Figure 21: Standard Interface Write Cycle Timing

Table 11: Standard Interface Write Cycle Parameters

Symbol	Description	VCC= VCCQ=1.65-1.95V		Units
		Min	Max	
TSU(A)	Address to WE# ↓ setup time	0		ns
Tho(A)	WE# ↓ to Address hold time	48		ns
Tw(WE)	WE# asserted width (RAM)	63		ns
	WE# asserted width (all other addresses)	52		ns
Tsu(CE0)	CE# ↓ to WE# ↓ setup time[1]	--		ns
Tho(CE0)	WE# ↑ to CE# ↑ hold time[2]	--		ns
Tho(CE1)	OE# or WE# ↑ to CE# ↓ hold time	5		ns
Tsu(CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	5		ns
Trec(WE)	WE# ↑ to start of next cycle	20		ns
Tsu(D)	D to WE# ↑ setup time	50		ns
Tho(D)	WE# ↑ to D hold time	0		

1. CE# may be asserted any time before or after WE# is asserted. If CE# is asserted after WE#, all timing relative to WE# asserted should be referenced to the time CE# was asserted.
2. CE# may be negated any time before or after WE# is negated. If CE# is negated before WE#, all timing relative to WE# negated will be referenced to the time CE# was negated.
3. Twcyc - Write cycle time is limited by the sum of tw(WE) and trec(WE).

10.3.3 Read Cycle Timing Multiplexed Interface

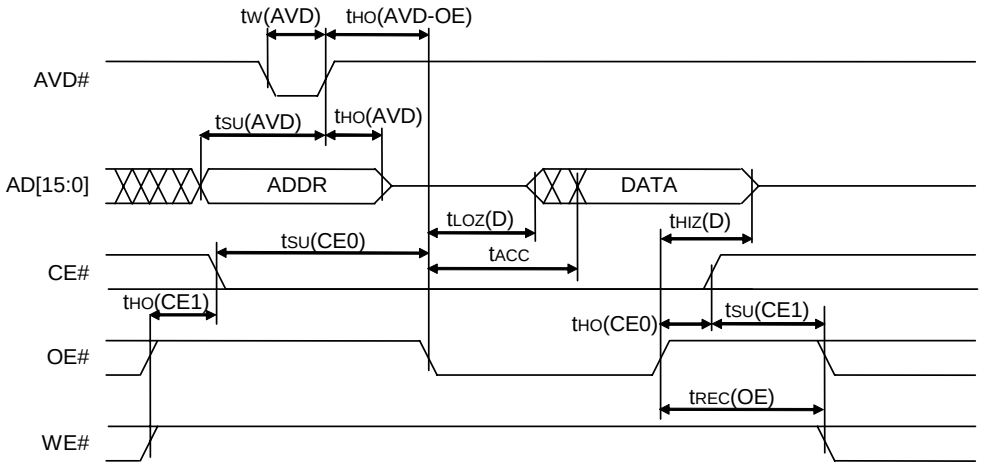


Figure 22: Multiplexed Interface Read Cycle Timing

Table 12: Multiplexed Interface Read Cycle Parameters

Symbol	Description	VCC= VCCQ=1.65-1.95V		Units
		Min	Max	
tsu(AVD)	Address to AVD# ↓ setup time[1]	14		ns
tho(AVD)	Address to AVD# ↑ hold time	2		ns
Tw(AVD)	AVD# low pulse width	8		ns
tHO(AVD-OE)	AVD# ↑ to OE# ↓ hold time[2]	0		ns
tsu(CE0)	CE# ↓ to OE# ↓ setup time[2]	—		ns
tho(CE0)	OE# ↑ to CE# ↑ hold time[3]	—		ns
tho(CE1)	OE# or WE# ↑ to CE# ↓ hold time	5		ns
tsu(CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	5		ns
trec(OE)	OE# negated to start of next cycle[4]	20		ns
Tacc	Read access time (RAM)		103	ns
	Read access time (all other addresses)		42	
tloz(D)	OE# ↓ to D driven[5]	17		ns
Thiz(D)	OE# ↑ to D Hi-Z delay[5,6]		22	ns

1. In DiskOnChip G3 64MB (512Mb), Tsu(AVD) was specified to the falling edge of AVD# rather than the rising edge
2. CE# may be asserted any time before or after OE# is asserted. If CE# is asserted after OE#, all timing relative to OE# asserted will be referenced instead to the time of CE# asserted.
3. CE# may be negated any time before or after OE# is negated. If CE# is negated before OE#, all timing relative to OE# negated will be referenced instead to the time of CE# negated.
4. Practical limit is determined by thiz(D)+ tsu(AVD)+ Tw(AVD)+MAX(0, tho(AVD-OE)- tloz(D)).
5. No load (C_L = 0 pF).
6. Does not include output buffer Hi-Z delay (**TBD**).

10.3.4 Write Cycle Timing Multiplexed Interface

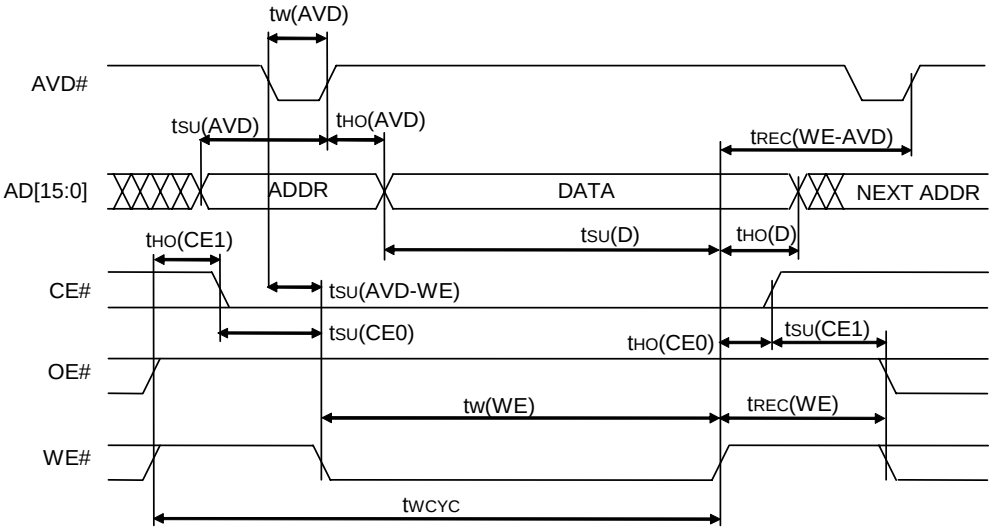


Figure 23: Multiplexed Interface Write Cycle Timing

Table 13: Multiplexed Interface Write Cycle Parameters

Symbol	Description	VCC= VCCQ=1.65-1.95V		Units
		Min	Max	
tsu(AVD)	Address to AVD# ↓ setup time[4]	14		ns
tho(AVD)	Address to AVD# ↑ hold time	2		ns
Tw(AVD)	AVD# low pulse width	8		ns
tsu(AVD-WE)	AVD# ↓ to WE# ↓ setup time[1]	4		ns
tw(WE)	WE# asserted width (RAM)[3]	63		ns
	WE# asserted width (all other addresses)[3]	52		
tsu(CE0)	CE# ↓ to WE# ↓ setup time[1]	—		ns
tho(CE0)	WE# ↑ to CE# ↑ hold time[2]	—		ns
tho(CE1)	OE# or WE# ↑ to CE# ↓ hold time	5		ns
tsu(CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	5		ns
trec(WE-AVD)	WE# ↑ to AVD# ↑ in next cycle	17		ns
trec(WE)	WE# ↑ to start of next cycle	20		ns
Tsu(D)	D to WE# ↑ setup time	50		ns
Tho(D)	WE# ↑ to D hold time	0		ns

1. CE# may be asserted any time before or after WE# is asserted. If CE# is asserted after WE#, all timing relative to WE# asserted will be referenced instead to the time of CE# asserted.
2. CE# may be negated any time before or after WE# is negated. If CE# is negated before WE#, all timing relative to WE# negated will be referenced instead to the time of CE# negated.
3. WE# may be asserted before or after the rising edge of AVD#. The beginning of the WE# asserted pulse width spec is measured from the later of the falling edge of WE# or the rising edge of AVD#.
4. On the DiskOnChip G3, Tsu(AVD) was specified to the falling edge of AVD# rather than the rising edge
5. Write cycle time is limited by the sum of tw(WE) and trec(WE).

10.3.5 Flash Characteristics

Table 14: Flash Program, Erase, and Read Timing

Symbol	Description	Rate		Unit
		Typ	Max	
tPROG	Page programming time	900	6000	uS
tERASE	Block erasing time	2	10	mS
tREAD	Even page reading time	32	40	uS
	Odd page reading time	16	20	uS

10.3.6 Power-Up Timing

DiskOnChip G3 LP is reset by assertion of the RSTIN# input. When this signal is negated, DiskOnChip G3 LP initiates a download procedure from the flash memory into the internal Programmable Boot Block. During this procedure, DiskOnChip G3 LP does not respond to read or write accesses.

Host systems must therefore observe the requirements described below for first access to DiskOnChip G3 LP. Any of the following methods may be employed to guarantee first-access timing requirements:

- Use a software loop to wait at least Tp (BUSY1) before accessing the device after the reset signal is negated.
- Poll the state of the BUSY# output.
- Poll the DL_RUN bit of the Download Status register until it returns 0. The DL_RUN bit will be 0 when BUSY# is negated.
- Use the BUSY# output to hold the host CPU in wait state before completing the first access which will be a RAM read cycle. The data will be valid when BUSY# is negated.

Hosts that use DiskOnChip G3 LP to boot the system must employ option 4 above or use another method to guarantee the required timing of the first-time access.

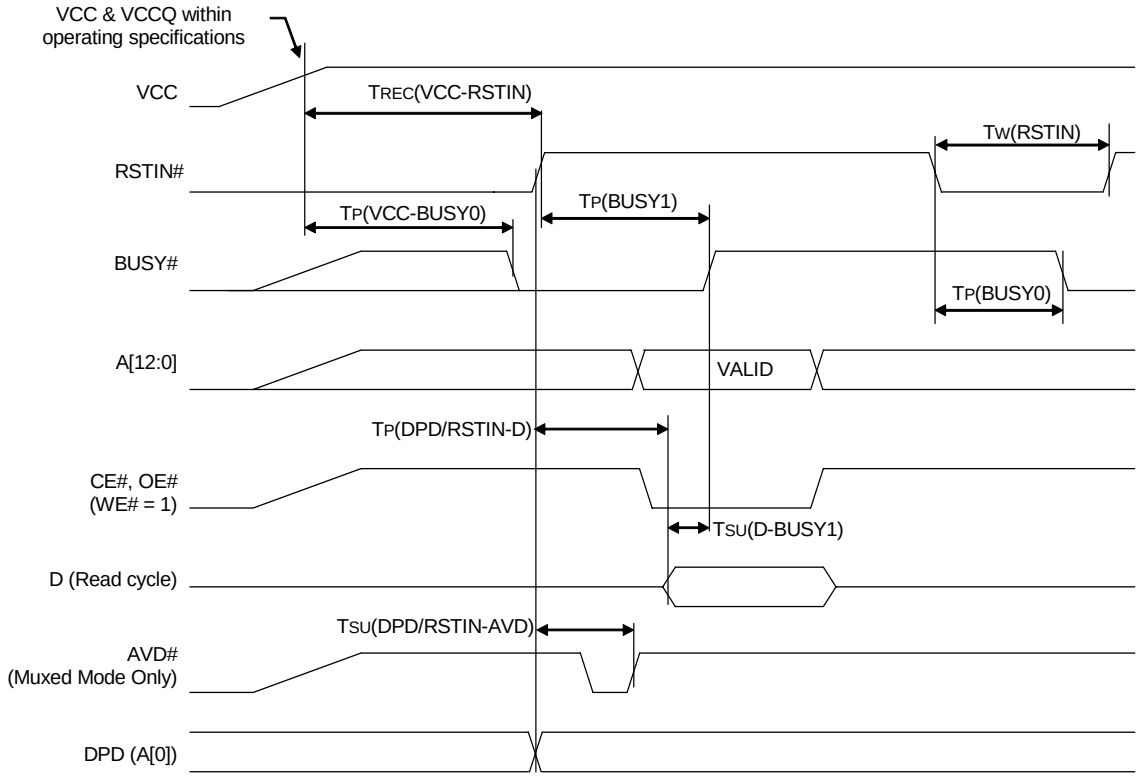


Figure 24: Reset Timing

Table 15: Power-Up Timing Parameters

Symbol	Description	Min	Max	Units
TREC (VCC-RSTIN)	VCC/VCCQ stable to RSTIN# ↑[1]	500		µs
TW (RSTIN)	RSTIN# asserted pulse width	50		ns
TP (BUSY0)	RSTIN# ↓ to BUSY# ↓		50	ns
TP (BUSY1)	RSTIN# ↑ to BUSY# ↑[2]		2066	µs
TSU (D-BUSY1)	Data valid to BUSY# ↑[3]	0		ns
tP(VCC-BUSY0)	VCC/VCCQ stable to BUSY# ↓		500	µs
tSU(DPD/RSTIN-AVD)[4,6]	DPD transition or RSTIN# ↑ to AVD# ↑	4200		nS
tP(DPD/RSTIN-D)[5,6]	DPD transition or RSTIN# ↑ to Data valid	710		nS
Trise(RSTIN)	RSTIN# rise time[7]	50		nS

1. Specified from the final positive crossing of VCC above 1.65V and VCCQ above 1.65V.
2. If the assertion of RSTIN# occurs during a flash erase cycle, this time could be extended by up to 500 µS.
3. Normal read/write cycle timing applies. This parameter applies only when the cycle is extended until the negation of the BUSY# signal.
4. Applies to multiplexed interface only.
5. Applies to SRAM mode only.
6. DPD transition refers to exiting Deep Power Down mode by toggling DPD (A[0]).
7. RSTIN# are not Schmidt-trigger types and therefore have no hysteresis. They should be driven only by standard logic with rise times not much greater 10 ns.

10.3.7 Interrupt Timing

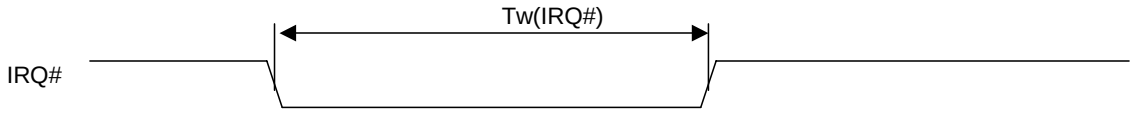
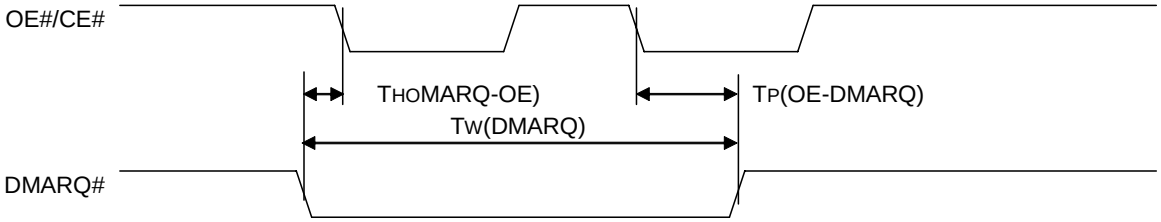


Figure 25: IRQ# Pulse Width in Edge Mode

Table 16: Interrupt Timing

Symbol	Description	Min	Max	Unit
Tw(IRQ#)	IRQ# asserted pulse width (Edge mode)	330	520	ns

10.3.8 DMA Request Timing



Note: Polarity of DMARQ# may be inverted based on the NORMAL bit of DMA Control Register[0].

Figure 26: DMARQ# Pulse Width

Table 17: DMA Request Timing

Symbol	Description	Min	Max	Unit
Tw(DMARQ#)	DMARQ# asserted pulse width	330	520	ns
Tho(DMARQ-OE)	DMARQ# asserted to start of cycle	0		ns
tP(OE-DMARQ)	Start of cycle to DMARQ# negated		55	ns

10.4 Mechanical Dimensions

10.4.1 DiskOnChip G3 64MB (512Mb)

FBGA dimensions: 7.0 ±0.20 mm x 10.0 ±0.20 mm x 1.1 ±0.1 mm
Ball pitch: 0.8 mm
FBGA weight: 135 mg

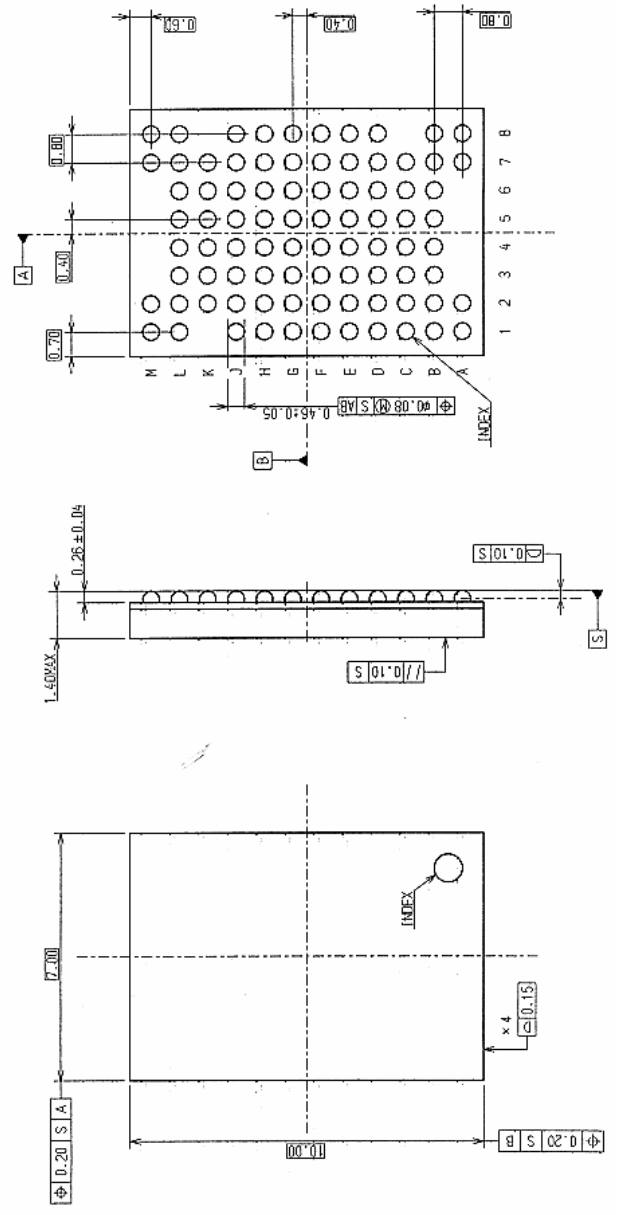


Figure 27: Mechanical Dimensions 7x10 FBGA Package

11. ORDERING INFORMATION

Refer to Table 18 for combinations currently available and the associated order numbers.

Table 18: Available Combinations

Ordering Code	Capacity		Package		Temperature Range
	MB	Mb			
MD6832-d512-V18-X			85-ball FBGA 7x10		Extended
MD6832-d512-V18-X-P			85-ball FBGA 7x10	Pb-free	Extended
MD6832-d00-DAISY	00	000	85-ball FBGA 7x10 Daisy-Chain	Daisy-chain format for package reliability testing	

A. SAMPLE CODE

This appendix provides sample code to verify basic DiskOnChip G3 LP 64MB (512Mb) operations in the system. This code is useful for the initial integration stages.

```
/*--------------------------------------------------------------------*/
/*               Identify DiskOnChip G3 LP 512Mb(64MB)                */
/*                                                                    */
/* The target of this sequence is to make sure that DiskOnChip G3     */
/* 64MB (512Mb) is alive and responds to basic commands.              */
/*                                                                    */
/* The sample code will set DiskOnChip in Normal mode, then check     */
/* ChipID, and then Write/Read to the internal SRAM of DiskOnChip     */
/* in order to confirm that the DiskOnChip is connected correctly     */
/*--------------------------------------------------------------------*/


/* Read DiskOnChip G3 LP 512Mb(64MB) ID before setting to Normal mode
*/
Read from offset 0x1000             /* Data undefined */


/* Set DiskOnChip G3 LP 512Mb(64MB)to Normal mode */
Write 0x0505 to offset 0x100C       /* Write to DiskOnChip Control
Register:Enter normal mode sequence */


Write 0xFAFA to offset 0x1072       /* Write to DiskOnChip
Confirmation Register: Enter normal mode sequence */


Write 0x1000 to offset 0x101A       /* Prepare to read Chip ID[0]
register from address 0x1000 by setting the address of ChipID[0]
register that will be read in the READ address register */


Read from offset 0x1000 into temp   /* DiskOnChip ID[0] should be
0x0200 */
If temp!=0x0200 return (FALSE)
```

```
Write 0x1074 to offset 0x101A       /* Prepare to read Chip ID[1]
register from address 0x1074 by setting the address of ChipID[1]
register that will be read in the READ address register */


Read from offset 0x1074 into temp   /* DiskOnChip ID[1] should be
0xFDFF */
If temp!=0xFDFF return (FALSE)


/* Write and Read Data from IPL area of DiskOnChip G3 LP 512Mb(64MB)
*/
for(i=0; i < 0x800; i+=2)           /* write/read cycle, 0x800 – IPL
size */
{
Write i to offset i                 /* write content of counter i at
offset i */
Read from offset i into temp        /* read data from same offset */
         If temp!= i return (FALSE) /* ERROR */
   }


/*-----------------------------------------------------------------*/
```

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