DiskOnChip®-Based MCP

Including Mobile DiskOnChip Plus and PSRAM

M-Systems
Flash Disk Pioneers

Highlights

DiskOnChip-based MCP (Multi-Chip Package) is a complete memory solution. Efficiently packed in a small Fine-Pitch Ball Grid Array (FBGA) package, it is ideal for data and code storage inside 2.5G and 3G mobile handsets and Personal Digital Assistants (PDAs). DiskOnChip-based MCP consists of:

- M-Systems' Mobile DiskOnChip Plus
- Toshiba's CMOS PSRAM (Pseudo Static RAM)

Using such an MCP configuration reduces overall memory costs, saves PCB real estate and maintains efficient power consumption levels. It may also have far-reaching implications on the mobile handset memory architecture, supporting a NOR-less memory system by providing boot functionality at a much less expensive cost than NOR.

General Features

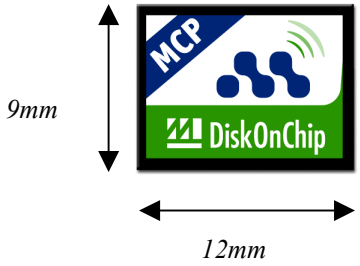
- Small 9x12x1.4 mm 107-ball, FBGA package
- 512Mbit (64MByte) Mobile DiskOnChip Plus
- 32Mbit (4MByte) Toshiba CMOS PSRAM
- High performance 16-bit interface to all devices
- Deep Power-Down mode for low power consumption
- Operating voltage: 2.7V to 3.3V
- Operating temperature: -30°C to +85°C

Mobile DiskOnChip Plus

Mobile DiskOnChip Plus 512Mbit (64MByte) is the industry's most efficient data and code storage solution, with the fastest write performance, the smallest die size and the highest level of reliability and flash endurance. Additionally, Mobile DiskOnChip Plus offers advanced data protection and security-enabling options.

Mobile DiskOnChip Plus features:

- Exceptional write, read, and erase performance
- Advanced protection and security-enabling features for data and code
- NAND-based flash technology that enables high density and small die size



- Proprietary TrueFFS® technology for full hard disk emulation, high data integrity and maximum flash lifetime
- Programmable Boot Block with eXecute In Place (XIP) functionality using 16-bit access to enable
  - CPU initialization
  - Platform initialization
  - OS boot
- Data integrity with Reed-Solomon-based Error Detection Code/Error Correction Code (EDC/ECC)
- Deep Power-Down mode for reduced power consumption
- Support for all major mobile operating systems (OSs), including
  - Symbian OS
  - Smartphone 2002/3
  - Pocket PC 2002/3
  - Windows CE/CE.NET
  - Linux
  - Nucleus
  - Palm
- Easy-to-integrate configurable interface
  - Simple NOR-like interface
- Compatible with all major CPUs, including
  - Texas Instruments OMAP
  - Intel StrongARM/XScale
  - Motorola MX1
  - Texas Instruments TMS320VC5509 DSP
  - NeoMagic MiMagic
  - AMD Alchemy
  - ARM-based CPUs

PSRAM

- Organization: 2M x 16 bits
- Power Dissipation
  - Operating: 50 mA max
  - Standby: 70 µA max
  - Deep Power-Down: 5 µA max
- Access Time
  - Random: 70 ns, CL=30 pF
  - Page: 30 ns, CL=30 pF
- Modes
  - Page read operation (8 words/page)
  - Deep Power-Down

Table of Contents

1. Product Overview 4
1.1 Ballout 4
1.2 Signal Descriptions 5
1.3 Internal Connections 6
1.4 Block Diagram 8
2. Specifications 9
2.1 Environmental 9
2.2 Mechanical 9
3. Ordering Information 10
4. Markings 10
Appendix A: 512Mbit Mobile DiskOnChip Plus Data Sheet
Appendix B: 32Mbit CMOS Pseudo Static RAM (PSRAM) Data Sheet

1. Product Overview

1.1 Ballout

M-Systems' DiskOnChip-based MCP is packaged in a 107-ball FBGA 9x12 mm package. See Figure 1 for the preliminary ball assignments.

Important! The ball assignment information in this section replaces and supersedes the assignment information in the individual data sheets from M-Systems and Toshiba, provided as part of this data sheet.

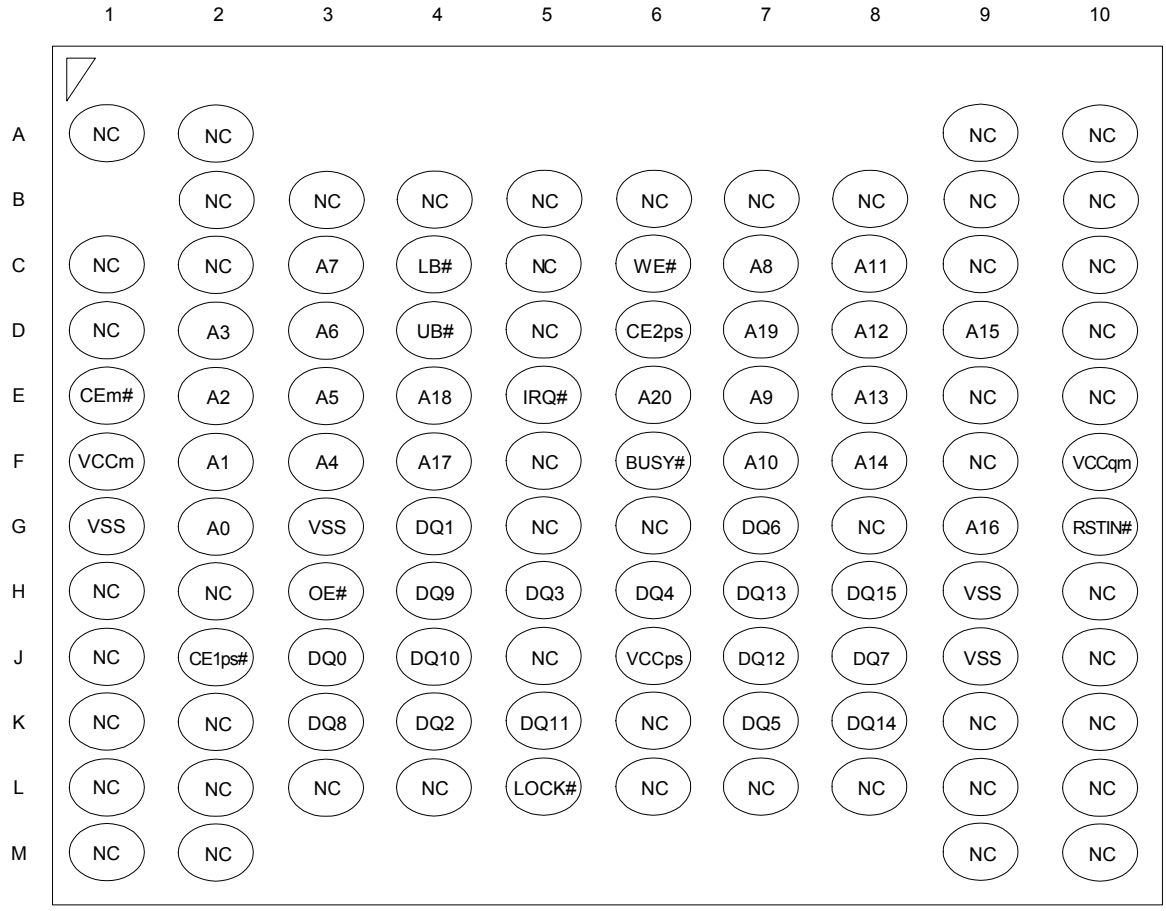


Figure 1: DiskOnChip-Based MCP Ball Diagram – Top View

1.2 Signal Descriptions

Table 1 contains signal descriptions based on the ball diagram in Figure 1.

Table 1: DiskOnChip-Based MCP Signal Descriptions

Signal	Description	Signal Type
A0-A22	Address bus: A1-A12 (Mobile DiskOnChip Plus) A0-A20 (PSRAM)	Input
CEm# CE1ps#, CE2ps	Chip Enable, active low (Mobile DiskOnChip Plus) Chip Enable 1 active low, Chip Enable 2 active high (PSRAM)	Input
DQ0-DQ15	Data bus	Input/Output
OE#	Output Enable, active low	Input
WE#	Write Enable, active low	Input
LB#, UB#	Data Byte control, active low (PSRAM)	Input
IRQ#	Interrupt Request (Mobile DiskOnChip Plus)	Output
BUSY#	Busy, active low (Mobile DiskOnChip Plus)	Output
RSTIN#	Reset, active low (Mobile DiskOnChip Plus)	Input
LOCK#	Lock, active low (Mobile DiskOnChip Plus). When active, provides full hardware data protection of selected partitions.	Input
VCCps	Power supply (PSRAM)	Supply
VCCm, VCCQm	Power supply (Mobile DiskOnChip Plus) (VCCm=VCCQm)	Supply
VSS	Ground. These balls must be connected.	Supply
NC	Not Connected.	

1.3 Internal Connections

Every component in the DiskOnChip-based MCP behaves as if it were a separate device. Each component has a separate ball for its Chip Enable (CE#) signal, as well as a separate ball for power supply. Table 2 shows the internal connections.

Note: Some signals described in the individual data sheets have been internally connected to VSS or VCC. Other signals are shared and therefore have been renamed.

Table 2: Internal Connections

Internal Connection		32Mb PSRAM	512Mb Mobile DiskOnChip Plus	Comments
BGA Location	Signal			
F10	VCCQm		VCCQ	
H2	NC			
F6	BUSY#		BUSY#	
J2	CE1ps#	CE1#		
F5	NC			
C4	LB#	LB#		
F1	VCCm		VCC	
H3	OE#	OE#	OE#	
D5	NC			
D4	UB#	UB#		
C6	WE#	WE#	WE#	
C5	NC			
D6	CE2ps	CE2		
G6	NC			
G8	NC			
E5	IRQ#		IRQ#	
G2	A0	A0	A1	A1 of Mobile DiskOnChip Plus is connected to A0 for 16-bit word support
F2	A1	A1	A2	
E2	A2	A2	A3	
D2	A3	A3	A4	
F3	A4	A4	A5	
E3	A5	A5	A6	
D3	A6	A6	A7	
C3	A7	A7	A8	
C7	A8	A8	A9	
E7	A9	A9	A10	
F7	A10	A10	A11	
C8	A11	A11	A12	
D8	A12	A12		
E8	A13	A13		
F8	A14	A14		

Internal Connection		32Mb PSRAM	512Mb Mobile DiskOnChip Plus	Comments
BGA Location	Signal			
D9	A15	A15		
G9	A16	A16		
F4	A17	A17		
E4	A18	A18		
D7	A19	A19		
E6	A20	A20		
E9	A21	A21		
F9	A22			Currently not connected – reserved for future expansion
J3	D0	D0	D0	
G4	D1	D1	D1	
K4	D2	D2	D2	
H5	D3	D3	D3	
H6	D4	D4	D4	
K7	D5	D5	D5	
G7	D6	D6	D6	
J8	D7	D7	D7	
K3	D8	D8	D8	
H4	D9	D9	D9	
J4	D10	D10	D10	
K5	D11	D11	D11	
J7	D12	D12	D12	
H7	D13	D13	D13	
K8	D14	D14	D14	
H8	D15	D15	D15	
J5	VCCf			
J6	VCCps	VCC		
G5	NC			
L5	LOCK#		LOCK#	
K6	NC			
H9	VSS		A0	AO of Mobile DiskOnChip Plus must be connected externally to VSS
G10	RSTIN#		RSTIN#	
G3	VSS	VSS	VSS	
J9	VSS	VSS	VSS	
E1	CEm#		CE#	
G1	VSS	VSS	VSS	
			ID0, ID1, BHE#	Internally connected to VSS
			IF_CFG	Internally connected to VCC

1.4 Block Diagram

Figure 2 shows a block diagram of all components that comprise the DiskOnChip-based MCP, including their special and interconnected signals.

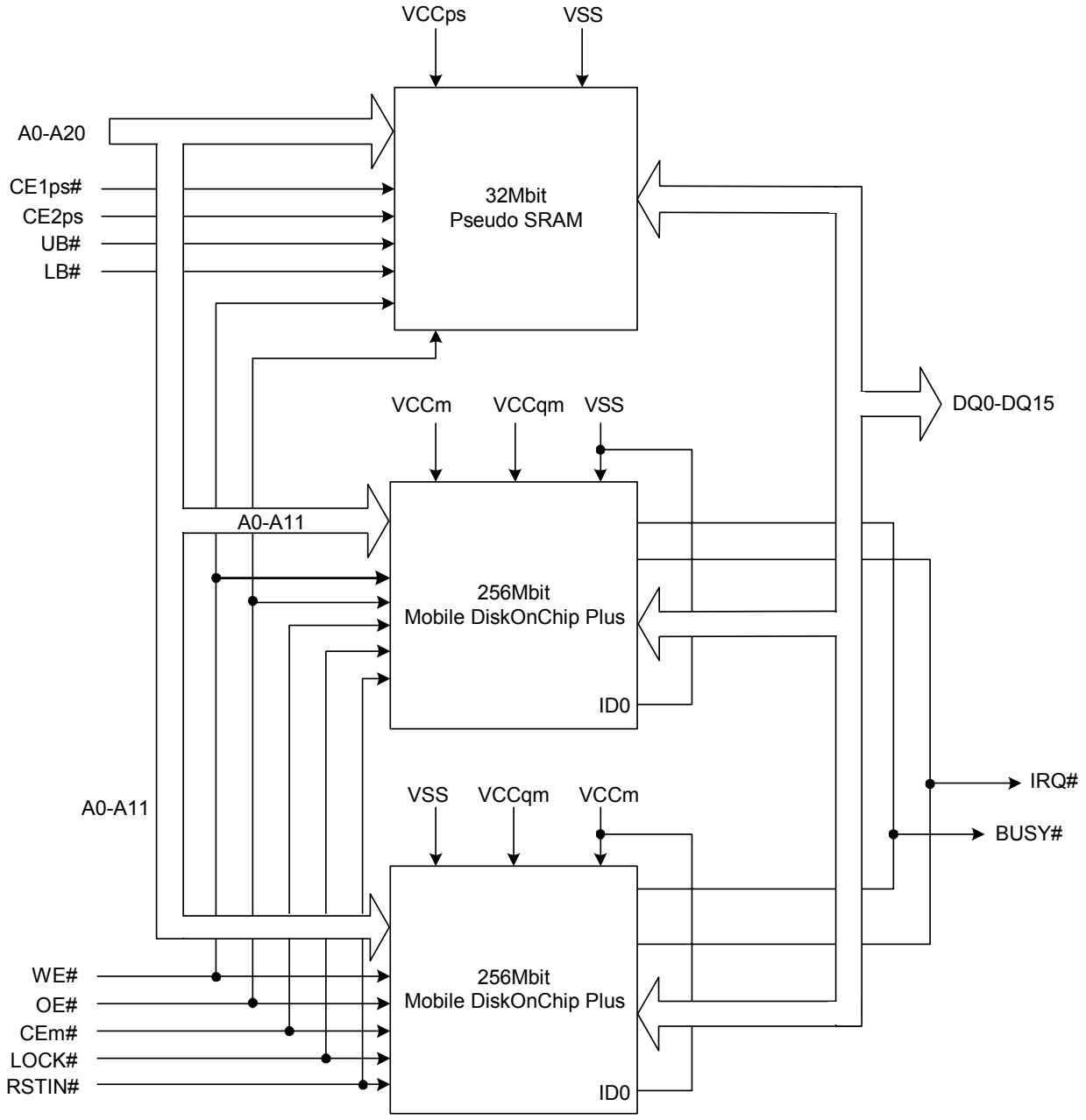


Figure 2: DiskOnChip-Based MCP Block Diagram

2. Specifications

2.1 Environmental

Temperature Range -30°C to +85°C

2.2 Mechanical

Dimensions 9.0±0.20 x 12.0±0.20 mm

Height 1.4±0.1 mm

Ball Count 107 balls

Ball Pitch 0.8 mm

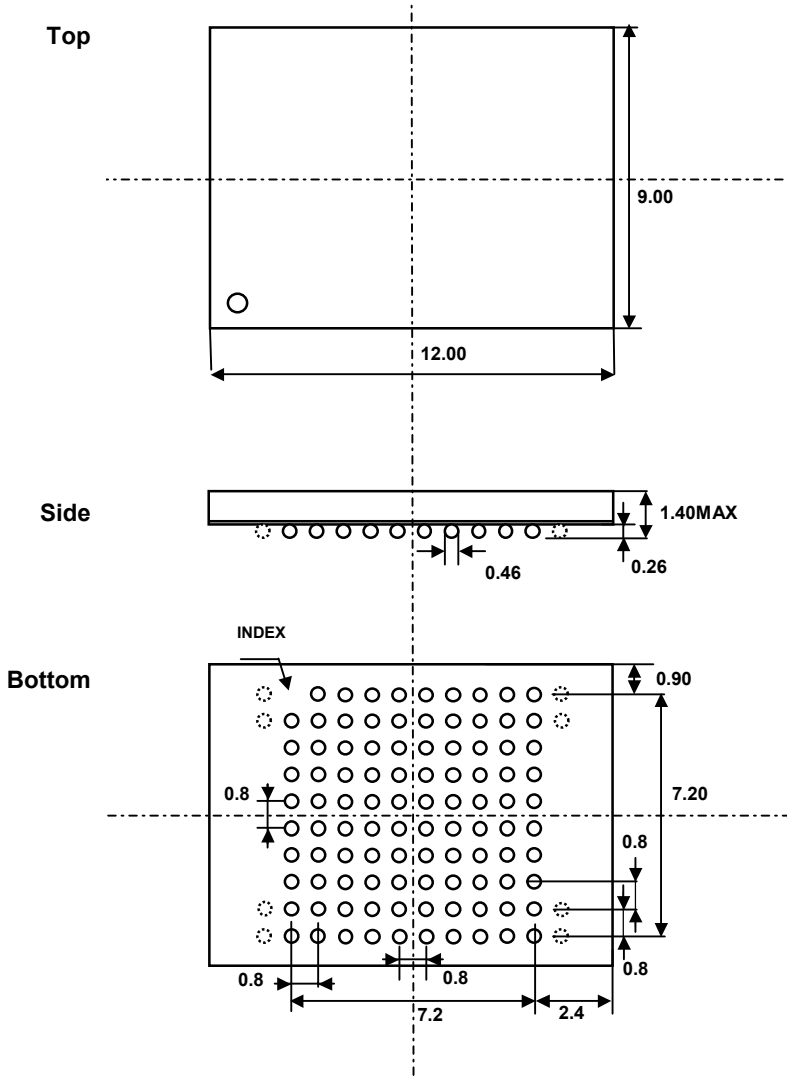


Figure 3: DiskOnChip-Based MCP Dimensions (all dimensions are in mm)

3. Ordering Information

MS04- D9P5-B1

MS04:	M-Systems' DiskOnChip-based MCP
D9:	Mobile DiskOnChip Plus 512Mbit (2^9 Mbit)
P5:	PSRAM 64Mbit (2^5 Mbit)
B1:	107-ball FBGA; 9x12x1.4 mm

4. Markings

First row: Product name – DiskOnChip MCP

Second row: Ordering information

Third row: Production information

yyww - Year and week

zzz - Product status: Engineering samples "-ES", Customer samples "-CS" or FAB marking

$$$$$$$$ - Internal marking



Appendix A: 512Mbit Mobile DiskOnChip Plus Data Sheet

Note: Information regarding packaging, ball assignment and package-level specifications does not apply to DiskOnChip-based MCP. For DiskOnChip-based MCP specifications, refer to Sections 1 and 2 of this data sheet.

Mobile DiskOnChip® Plus 32/64MByte

Flash Disk with Protection and Security-Enabling Features

M-Systems
Flash Disk Pioneers

Highlights

Mobile DiskOnChip Plus 32/64MByte (256/512Mbit) is one of the industry's most efficient storage solutions, with the fastest write rates, the smallest size and lowest power consumption. Additionally, it offers advanced data protection and security-enabling features. Based on a monolithic (dual-die) chip that utilizes Toshiba's 0.16µ NAND technology, Mobile DiskOnChip Plus attains levels of reliability that surpass competing products.

These characteristics make Mobile DiskOnChip Plus ideal for meeting the growing demand for secure and reliable data storage in mobile multimedia devices, such as mobile phones and Personal Digital Assistants (PDAs).

Mobile DiskOnChip Plus 32/64MByte features:

- Exceptional read, write and erase performance
- Advanced protection and security-enabling features for data and code
- Small form factor: 69-ball 9x12 mm Fine-Pitch Ball Grid Array (FBGA)
- NAND-based flash technology that enables high density and small die size
- Proprietary TrueFFS® technology for full hard disk emulation, high data reliability and maximum flash lifetime
- Single-die chip: 32MByte
  Dual-die chip: 64MByte with device cascade options for up to 128MByte capacity
- Programmable Boot Block with eXecute In Place (XIP) functionality using 16-bit access, with download support for more code
- Configurable for 8/16/32-bit bus interface
- Data integrity with Reed-Solomon-based Error Detection Code/Error Correction Code (EDC/ECC)
- Deep Power-Down mode for reduced power consumption
- Support for all major mobile OSs, including: Symbian OS, Windows CE, Smartphone 2002/3, Pocket PC, Nucleus, OSE, and Linux



Performance

- Burst read/write: 20 MB/sec
- Sustained read: 3.1 MB/sec
- Sustained write: 1.3 MB/sec

Protection and Security Enabling Features

- 16-byte Unique Identification (UID) number
- 6KByte user-configurable One Time Programmable (OTP) area
- Two configurable write-protected and read-protected partitions for data and boot code
- Hardware data and code protection:
  - Protection key and LOCK# signal
  - Protected Bad Block Table

Boot Capability

- Programmable Boot Block with XIP functionality to replace boot ROM:
  - 1KB for 32MByte devices
  - 2KB for 64MByte devices
- Download Engine (DE) for automatic download of boot code from Programmable Boot Block
- Boot capabilities:
  - CPU initialization
  - Platform initialization
  - OS boot

The following abbreviations are used in this document: MB for MByte, Mb for Mbit.

Reliability

- On-the-fly Reed-Solomon Error Detection Code/Error Correction Code (EDC/ECC)
- Guaranteed data integrity, even after power failure
- Transparent bad-block management
- Dynamic and static wear-leveling

Hardware Compatibility

- Simple SRAM-like interface
- Compatible with all major CPUs, including:
  - ARM-based CPUs
  - Texas Instruments OMAP
  - Intel StrongARM/XScale
  - AMD Alchemy
  - Motorola PowerPC™ MPC8xx
  - Motorola Dragon MX1
  - Philips PR31700
  - Hitachi SuperH™ SH-x
  - NEC VR Series
- 8-bit, 16-bit and 32-bit bus architecture support

TrueFFS Software

- Full hard-disk read/write emulation for transparent file system management
- Identical software for all DiskOnChip capacities
- Patented methods to extend flash lifetime, including:
  - Dynamic virtual mapping
  - Dynamic and static wear-leveling
- Support for all major OS environments, including:
  - Symbian OS
  - Windows CE
  - Pocket PC
  - Smartphone
  - OSE
  - ATI Nucleus
  - Linux
- Support for OS-less environments
- 8KByte memory window

Power Requirements

- Core and I/O voltage: 2.7V to 3.6V
- Current
  - Active: 25 mA (Typ.)
  - Deep Power-Down (Typ.): 10 µA (32MB) 20 µA (64MB)

Capacities

- 32MB (256Mb) with device cascading option for up to 128MB (1Gb)
- 64MB (512Mb) with device cascading option for up to 128MB (1Gb)

Packaging

- 69-ball FBGA: 9 x 12 x 1.4 mm (max)

Table of Contents

1. Introduction 6

2. Product Overview 8

2.1 Product Description 8

2.2 Standard Interface 9
2.2.1 Ball Diagram 9
2.2.2 System Interface 10
2.2.3 Signal Descriptions 11

3. Theory of Operation 13

3.1 Overview 13

3.2 System Interface 14

3.3 Configuration Interface 14

3.4 Protection and Security-Enabling Features 14
3.4.1 Read/Write Protection 14
3.4.2 Unique Identification (UID) Number 15
3.4.3 One-Time Programmable (OTP) Area 15

3.5 Programmable Boot Block with eXecute In Place (XIP) Functionality 15

3.6 Download Engine (DE) 15

3.7 Error Detection Code/Error Correction Code (EDC/ECC) 16

3.8 Data Pipeline 16

3.9 Control & Status 16

3.10 Flash Architecture 16

4. Hardware Protection 18

4.1 Method of Operation 18

4.2 Low-Level Structure of the Protected Area 19

5. Modes of Operation 20

5.1 Normal Mode 21

5.2 Reset Mode 21

5.3 Deep Power-Down Mode 21

6. TrueFFS Technology 22

6.1 General Description 22
6.1.1 Built-In Operating System Support 22
6.1.2 TrueFFS Software Development Kit (SDK) 23
6.1.3 File Management 23
6.1.4 Bad-Block Management 23
6.1.5 Wear-Leveling 23
6.1.6 Power Failure Management 24
6.1.7 Error Detection/Correction 24
6.1.8 Special Features through I/O Control (IOCTL) Mechanism 24
6.1.9 Compatibility 24

6.2 8KB Memory Window in Mobile DiskOnChip Plus 32MB 25

6.3 8KB Memory Window in Mobile DiskOnChip Plus 64MB 26

7. Register Descriptions 27
7.1 Definition of Terms 27
7.2 Reset Values 27
7.3 Chip Identification (ID) Register 27
7.4 No Operation (NOP) Register 28
7.5 Test Register 28
7.6 DiskOnChip Control Register/Control Confirmation Register 29
7.7 Device ID Select Register 30
7.8 Configuration Register 30
7.9 Interrupt Control Register 31
7.10 Toggle Bit Register 31
8. Booting from Mobile DiskOnChip Plus 32
8.1 Introduction 32
8.2 Boot Procedure in PC-Compatible Platforms 32
8.3 Boot Replacement 33
8.3.1 PC Architectures 33
8.3.2 Non-PC Architectures 33
9. Design Considerations 34
9.1 Design Environment 34
9.2 System Interface 35
9.3 Connecting Signals 36
9.4 Implementing the Interrupt Mechanism 36
9.4.1 Hardware Configuration 36
9.4.2 Software Configuration 36
9.5 Platform-Specific Issues 37
9.5.1 Wait State 37
9.5.2 Big and Little Endian Systems 37
9.5.3 Busy Signal 37
9.5.4 Working with 8/16/32-Bit Systems with a Standard Interface 38
9.6 Device Cascading 40
9.6.1 Memory Map in a Cascaded Configuration 40
10. Product Specifications 42
10.1 Environmental Specifications 42
10.1.1 Operating Temperature Ranges 42
10.1.2 Thermal Characteristics 42
10.1.3 Humidity 42
10.1.4 Endurance 42
10.2 Disk Capacity 42
10.3 Electrical Specifications 43
10.3.1 Absolute Maximum Ratings 43
10.3.2 Capacitance 43
10.3.3 DC Electrical Characteristics Over Operating Range 44
10.3.4 AC Operating Conditions 45

10.4 Timing Specifications 45
10.4.1 Read Cycle Timing Standard Interface 45
10.4.2 Write Cycle Timing Standard Interface 47
10.4.3 Power-Up Timing 48
10.4.4 Interrupt Timing 49
10.5 Mechanical Dimensions 50
11. Ordering Information 51

Revision History

Revision	Date	Description	
1.6	February 2003	Ordering info table replaced to reflect Pb-free ordering info.	See Section 11

1. Introduction

This data sheet includes the following sections:

Section 1: Overview of data sheet contents

Section 2: Product overview, including a brief product description, pin and ball diagrams and signal descriptions

Section 3: Theory of operation for the major building blocks

Section 4: Hardware Protection mechanism

Section 5: Modes of operation

Section 6: TrueFFS technology, including power failure management and 8KByte memory window

Section 7: Register description

Section 8: Using Mobile DiskOnChip Plus as a boot device

Section 9: Hardware and software design considerations

Section 10: Environmental, electrical, timing and product specifications

Section 11: Information on ordering Mobile DiskOnChip Plus

Appendix A: Sample code for verifying Mobile DiskOnChip Plus operation

To contact M-Systems' worldwide offices for general information and technical support, please see the listing on the back cover, or visit M-Systems' website (www.m-sys.com).

2. Product Overview

2.1 Product Description

Mobile DiskOnChip Plus 32/64MB is a member of M-Systems' DiskOnChip product series. It is a based on a single die (32MB) or dual die (64MB) with an embedded flash controller and flash memory, providing a complete, easily integrated flash disk for highly reliable data storage. Mobile DiskOnChip Plus also offers advanced features for hardware-protected data and code and security-enabling features for both data and code storage. With superior read and write performance, small size and low power consumption, it is optimized for the high-end handset, multimedia handset and PDA markets. These markets require fast read and write rates, minimum weight and space, and low power consumption to support the large and growing pool of data-rich applications.

Mobile DiskOnChip Plus protection and security features offer unique benefits. Two write- and read-protected partitions, with both software and hardware-based protection, can be configured independently for maximum design flexibility. The 16-byte Unique ID (UID) identifies each flash device, used with security and authentication applications, eliminating the need for a separate ID device (i.e. EEPROM) on the motherboard. The user-configurable One Time Programmable (OTP) area, written to once and then locked to prevent data and code from being altered, is ideal for storing customer and product-specific information. In addition, the Bad Block Table is hardware-protected, ensuring that it will not be damaged or accidentally changed to ensure maximum reliability.

Mobile DiskOnChip Plus devices have a simple SRAM-like interface, for easy integration.

Mobile DiskOnChip Plus is based on Toshiba's cutting-edge 0.16µ NAND flash technology. This technology enables Mobile DiskOnChip Plus to provide unmatched physical and performance-related benefits. It has the highest flash density in the smallest die size available on the market, for the best cost structure and the smallest real estate. Mobile DiskOnChip Plus devices use 16-bit internal flash access, featuring unrivaled write and read performance.

Mobile DiskOnChip Plus is a cost-effective solution for code storage as well as data storage. A Programmable Boot Block with eXecute In Place (XIP) functionality can store boot code, replacing the boot ROM to function as the only non-volatile memory on board. The Programmable Boot Block is 1KB for 32MB devices and 2KB for 64MB devices. This reduces hardware expenditures and board real estate. M-Systems' Download Engine (DE) is an automatic bootstrap mechanism that expands the functionality of the Programmable Boot Block to enable CPU and platform initialization directly from Mobile DiskOnChip Plus.

M-Systems' patented TrueFFS software technology fully emulates a hard disk to manage the files stored on Mobile DiskOnChip Plus. This transparent file system management enables read/write operations that are identical to a standard, sector-based hard disk. In addition, TrueFFS employs various patented methods, such as dynamic virtual mapping, dynamic and static wear-leveling, and automatic bad-block management to ensure high data reliability and to maximize flash lifetime. TrueFFS binary drivers are available for a wide range of popular OSs, including Symbian OS, Pocket PC, Smartphone, Windows CE/.NET, OSE, Nucleus, and Linux. Customers developing for target platforms not supported by TrueFFS binary drivers can use the *TrueFFS Software Development Kit (SDK)* developer guide. For customized boot solutions, M-Systems provides the *DiskOnChip Boot Software Development Kit (BDK)* developer guide.

Mobile DiskOnChip Plus is designed for compatibility and easy scalability. It can be used as a drop-in replacement for all capacities Mobile DiskOnChip Plus devices. Greater capacities may easily be obtained by cascading up to four 32MB devices or up to two 64MB devices with no additional glue logic. This upgrade path provides a flash disk of up to 128MB (1Gb), while remaining totally transparent to the file system and user.

2.2 Standard Interface

2.2.1 Ball Diagram

See Figure 1 for the Mobile DiskOnChip Plus standard interface FBGA ball diagram. To ensure proper device functionality, balls marked RSRVD are reserved for future use and should not be connected.

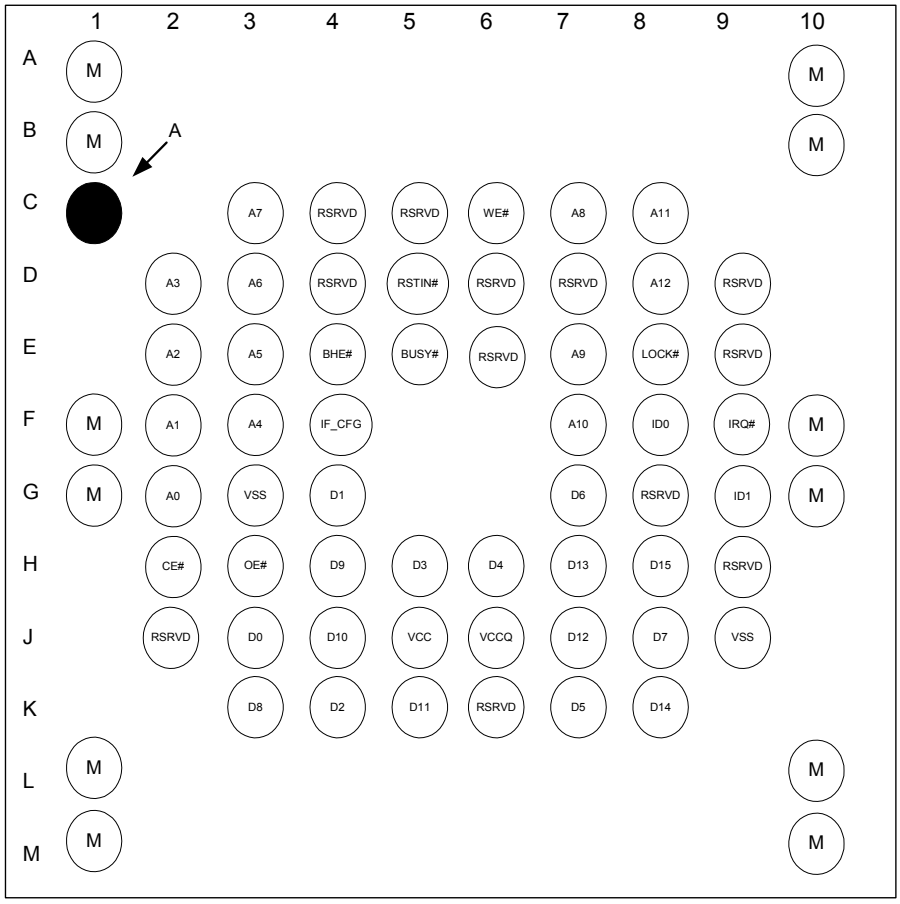


Figure 1: Standard Interface FBGA Ball Diagram (Top View)

2.2.2 System Interface

See Figure 2 for a simplified I/O diagram for a standard interface.

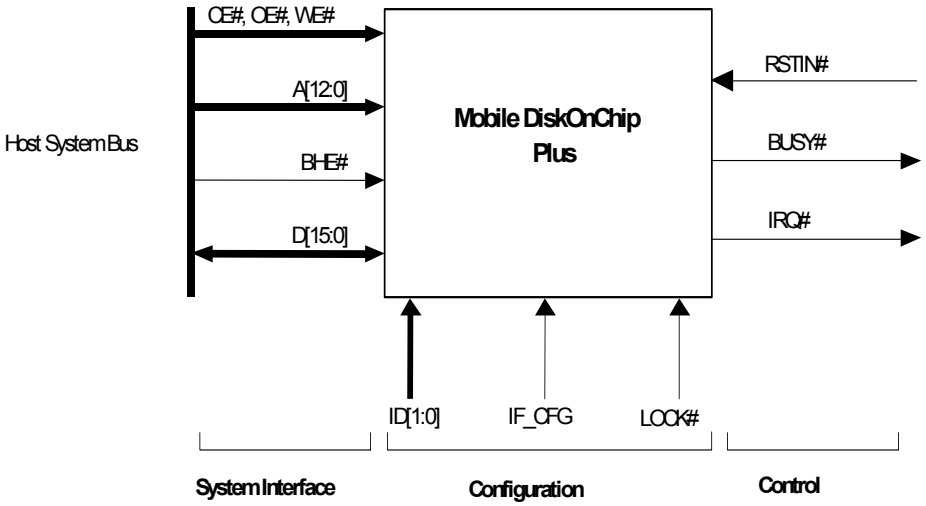


Figure 2: Standard Interface Simplified I/O Diagram

2.2.3 Signal Descriptions

The ball designations are listed in the signal descriptions, presented in logic groups, in Table 1.

Table 1: Standard Interface Signal Descriptions

Signal	Ball No.	Input Type	Description	Signal Type
System Interface				
A[12:11] A[10:8] A[7:4] A[3:0]	D8, C8 F7, E7, C7 C3, D3, E3, F3 D2, E2, F2, G2	ST	Address bus.	Input
BHE#	E4	ST, R8	Byte High Enable, active low. When low, data transaction on D[15:8] is enabled. Not used and may be left floating when IF_CFG is set to 0 (8-bit mode).	Input
CE#	H2	ST, R	Chip Enable, active low.	Input
D[7:0]	J8, G7, K7, H6, H5, K4, G4, J3	IN	Data bus, low byte.	Input/ Output
D[15:8]	H8, K8, H7, J7, K5, J4, H4, K3	IN, R8	Data bus, high byte. Not used and may be left floating when IF_CFG is set to 0 (8-bit mode).	Input
OE#	H3	ST	Output Enable, active low	Input
WE#	C6	ST	Write Enable, active low	Input
Configuration				
ID[1:0]	G9, F8	ST	Identification. For Mobile DiskOnChip 32MB, up to four chips can be cascaded in the same memory window, according to the following assignment: Chip 1 = ID1, ID0 = VSS, VSS (0,0); required for single chip Chip 2 = ID1, ID0 = VSS, VCC (0,1) Chip 3 = ID1, ID0 = VCC, VSS (1,0) Chip 4 = ID1, ID0 = VCC, VCC (1,1) For Mobile DiskOnChip 64MB, up to two chips can be cascaded in the same memory window, according to the following assignment: Chip 1 :ID1=VSS; ID0 = VSS; required for single chip Chip 2 : ID1=VSS; ID0 = Vcc	Input
IF_CFG	F4	ST	Interface Configuration, 1 for 16-bit interface mode, 0 for 8-bit interface mode.	Input
LOCK#	E8	ST	Lock, active low. When active, provides full hardware data protection of selected partitions.	Input
Control				
BUSY#	E5	OD	Busy, active low, open drain. Indicates that DiskOnChip is initializing and should not be accessed. A 10 KΩ pull-up resistor is required even if the ball is not used.	Output
IRQ#	F9	-	Interrupt Request. Requires a 10 KΩ pull-up resistor.	Input
RSTIN#	D5	ST	Reset, active low.	Input

Signal	Ball No.	Input Type	Description	Signal Type
Power				
VCCQ	J6	-	I/O power supply. Requires a 10 nF and 0.1 µF capacitor. For these devices VCCQ=VCC.	Supply
VCC	J5, J6	-	Device supply. Requires a 10 nF and 0.1 µF capacitor.	Supply
VSS	G3, J9	-	Ground. All VSS balls must be connected.	Supply
Reserved				
RSRVD	K6	-	Reserved signal that is not connected internally. Note: Future DiskOnChip devices will use this pin as a clock input. To be forward compatible, this pin can already be connected to the system CLK or to VCC when the clock input feature is not required.	
	Other. See Figure 1	-	All reserved signals are not connected internally and must be left floating to guarantee forward compatibility with future products. They should not be connected to arbitrary signals.	
Mechanical				
-	M	-	Mechanical. These balls are for mechanical placement, and are not connected internally.	
-	A	-	Alignment. This ball is for device alignment, and is not connected internally	

The following abbreviations are used:

IN	Standard (non-Schmidt) input
ST	Schmidt Trigger input
OD	Open drain
R8	Nominal 22 KΩ pull-up resistor, enabled only for 8-bit interface mode (IF_CFG input is 0)
R	3.7 MΩ nominal pull-up resistor

Note: For forward compatibility with future DiskOnChip 7x10 FBGA products, additional pads are required. Please refer to application note AP-DOC-067, *Preparing Your PCB Footprint for the DiskOnChip BGA Migration Path,* for detailed information.

3. Theory of Operation

3.1 Overview

Mobile DiskOnChip Plus consists of the following major functional blocks, as shown in Figure 3.

- **System Interface** for host interface
- **Configuration Interface** for configuring Mobile DiskOnChip Plus to operate in 8/16-bit mode, cascaded configuration and hardware write protection.
- **Protection and Security-Enabling** containing write/read protection and One-Time Programming (OTP), for advanced data/code security and protection.
- **Programmable Boot Block** with XIP capability enhanced with a **Download Engine (DE)** for system initialization capability.
- **Reed-Solomon-based Error Detection and Error Correction Code (EDC/ECC)** for on-the-fly error handling.
- **Data Pipeline** through which the data flows from the system to the NAND flash arrays.
- **Control & Status** block that contains registers responsible for transferring the address, data and control information between the TrueFFS driver and the flash media.
- **Flash Interface** whose architecture depends on the capacity: 32MB (256Mb) and 64MB[1] (512Mb) implement a unique interleaved, dual bank architecture of two embedded 16MB NAND flash arrays.
- **Bus Control** for translating the host bus address, data and control signals into valid NAND flash signals.
- **Address Decoder** to enable the relevant unit inside the DiskOnChip controller, according to the address range received from the system interface.

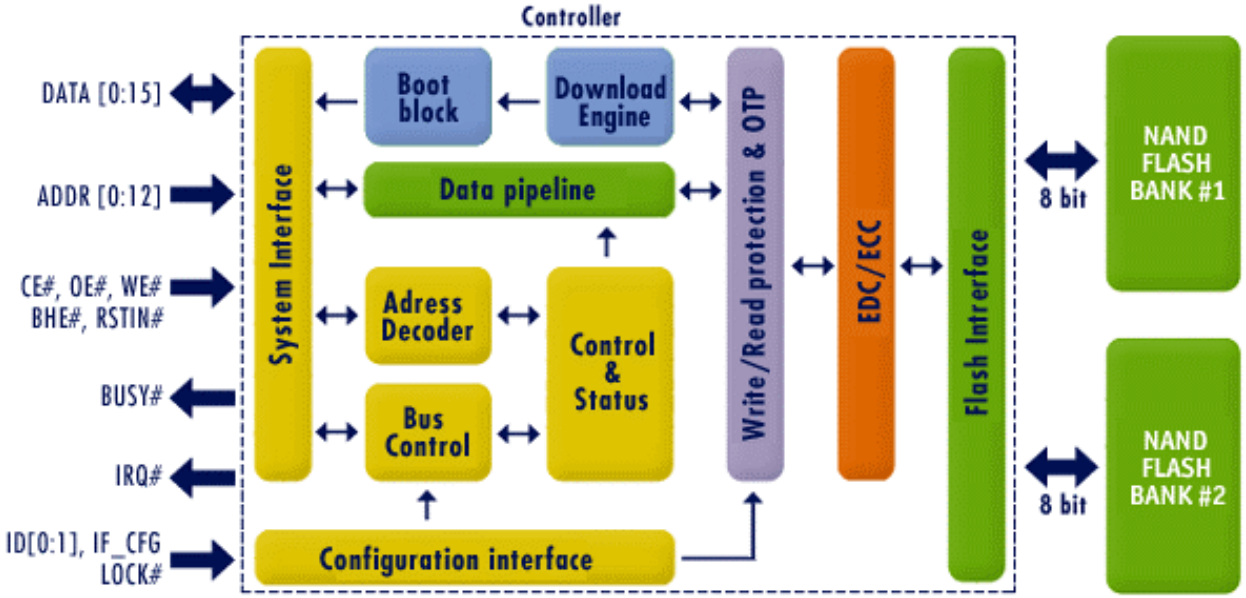


Figure 3: Standard Interface Simplified Block Diagram

[1] Mobile DiskOnChip Plus 64MB consists of two stacked Mobile DiskOnChip Plus 32MB devices in a dual-die package.

3.2 System Interface

The system interface block provides an easy-to-integrate SRAM-like (also EEPROM-like) interface to Mobile DiskOnChip Plus, enabling it to interface with various CPU interfaces, such as a local bus, ISA bus, SRAM interface, EEPROM interface or any other compatible interface. In addition, the EEPROM-like interface enables direct access to the Programmable Boot Block to permit XIP functionality during system initialization.

A 13-bit wide address bus enables access to the DiskOnChip 8KB memory window (as shown in Sections 6.2 and 6.3). The 16-bit data bus permits full 16-bit wide access to the flash, due to an internal, dual-bank, interleaved architecture. With both internal and external 16-bit access, Mobile DiskOnChip Plus 32/64MB provides unrivaled performance.

The Chip Enable (CE#), Write Enable (WE#) and Output Enable (OE#) signals trigger read and write cycles. A write cycle occurs while both the CE# and the WE# inputs are asserted. Similarly, a read cycle occurs while both the CE# and OE# inputs are asserted. Note that Mobile DiskOnChip Plus does not require a clock signal. Mobile DiskOnChip Plus features a unique analog static design, optimized for minimal power consumption. The CE#, WE# and OE# signals trigger the controller (e.g., system interface block, bus control and data pipeline) and flash access.

The Reset In (RSTIN#) and Busy (BUSY#) control signals are used in the reset phase. See Section 5.2 for further details.

The Interrupt Request (IRQ#) signal can be used when long I/O operations, such as Block Erase, delay the CPU resources. The signal is also asserted when a Data Protection violation has occurred. When this signal is implemented, the CPU can run other tasks and only returns to continue read/write operations with Mobile DiskOnChip Plus after the IRQ# signal has been asserted and an Interrupt Handling Routine (implemented in the OS) has been called to return control to the TrueFFS driver.

Mobile DiskOnChip Plus contains several configuration signals. The identification signals (ID[1:0]) are used for identifying the relevant DiskOnChip device in a cascaded configuration (see Section 9.6 on cascading for further details). The Lock (LOCK#) signal enables hard-wire hardware-controlled protection of code and data, as described below on protection and security-enabling features. For a standard interface, the Interface Configuration (IF_CFG) signal configures DiskOnChip for 16-bit or 8-bit data access (see Section 9.5.4).

3.3 Configuration Interface

The Configuration Interface block enables the designer to configure Mobile DiskOnChip Plus to operate in different modes. The identification signals (ID[1:0]) are used for identifying the relevant DiskOnChip device in a cascaded configuration (see Section 9.6 on cascading for further details). The Lock (LOCK#) signal enables hard-wire hardware-controlled protection of code and data, as described below. For a standard interface, the Interface Configuration (IF_CFG) signal configures Mobile DiskOnChip Plus for 16-bit or 8-bit data access (see Section 9.5.4).

3.4 Protection and Security-Enabling Features

The protection and security-enabling block, consisting of read/write protection, UID and OTP area, enables advanced data and code security and protection. Located on the main route of traffic between the host and the flash, this block monitors and controls all data and code transactions to and from Mobile DiskOnChip Plus.

3.4.1 Read/Write Protection

Data and code protection is implemented through a Protection State Machine (PSM). The user can configure one or two independently programmable areas of the flash memory as read protected, write protected, or read/write protected.

A protection area may be protected by either/both of these hardware mechanisms:

- 64-bit protection key
- Hard-wired LOCK# signal

The size and location of each area is user-defined to provide maximum flexibility for the target platform and application requirements.

The configuration parameters of the protected areas are stored on the flash media and are automatically downloaded from the flash to the PSM upon power-up, to enable robust protection throughout the flash lifetime.

In the event of an attempt to bypass the protection mechanism, illegally modify the protection key or in any way sabotage the configuration parameters, the entire DiskOnChip becomes both read and write protected, and is completely inaccessible.

For further information on the hardware protection mechanism, refer to Section 4.

3.4.2 Unique Identification (UID) Number

Each Mobile DiskOnChip Plus is assigned a 16-byte UID number. Burned onto the flash during production, the UID cannot be altered and is unique worldwide. The UID is essential in security-related applications, and can be used to identify end-user products in order to fight fraudulent duplication by imitators.

The UID on Mobile DiskOnChip Plus eliminates the need for an additional on-board ID device, such as a dedicated EEPROM.

3.4.3 One-Time Programmable (OTP) Area

The 6KB OTP area is user-programmable for complete customization. The user can write to this area once, after which it is automatically locked permanently. After it is locked, the OTP area becomes read only, just like a ROM device.

Typically, the OTP area is used to store customer and product information such as: product ID, software version, production data, customer ID and tracking information.

3.5 Programmable Boot Block with eXecute In Place (XIP) Functionality

During boot, code must be executed directly from the flash media, rather than first copied to the host RAM and then executed from there. This direct XIP code execution functionality is essential for booting.

The Programmable Boot Block with XIP functionality enables Mobile DiskOnChip Plus to act as a boot ROM device in addition to being a flash disk. This unique design enables the user to benefit from the advantages of NOR flash, typically used for boot and code storage, and NAND flash, typically used for data storage. No other boot device is required on the motherboard.

Mobile DiskOnChip Plus 32MB contains a 1KB Programmable Boot Block, and the 64MB contains a 2KB Programmable Boot Block. The Download Engine (DE) described in the next section expands the functionality of this block by copying the boot code from the flash to the boot block.

When two, three or four Mobile DiskOnChip Plus devices are cascaded, the Programmable Boot Block is accumulated respectively, providing 2, 3 or 4KB of boot block. The Programmable Boot Block of each device is mapped to a unique address space.

Note: Up to two Mobile DiskOnChip Plus 64MB devices can be cascaded, providing a Programmable Boot Block of 4KB.

3.6 Download Engine (DE)

Upon power up or when the RSTIN# signal is asserted high, the DE automatically downloads the Initial Program Loader (IPL) from the flash to the Programmable Boot Block. The IPL is responsible for starting the boot process. The download process is quick (1.3 ms max) and is designed so that when the CPU accesses Mobile DiskOnChip Plus for code execution, the IPL code is already located in the Programmable Boot Block.

In addition, the DE downloads the Data Protection Structures (DPS) from the flash to the Protection State Machines (PSMs), so that Mobile DiskOnChip Plus is secure and protected from the first moment it is active.

During the download process, Mobile DiskOnChip Plus asserts the BUSY# signal to indicate to the system that it is not yet ready to be accessed. After BUSY# is negated, the system can access Mobile DiskOnChip Plus.

A failsafe mechanism prevents improper initialization due to a faulty VCC or invalid assertion of the RSTIN# input. Another failsafe mechanism is designed to overcome possible NAND flash data errors. It prevents internal registers from powering up in a state that bypasses the intended data protection. In addition, in any attempt to sabotage the data structures causes the entire Mobile DiskOnChip Plus to become both read and write-protected and completely inaccessible.

3.7 Error Detection Code/Error Correction Code (EDC/ECC)

NAND flash, being an imperfect memory, requires error handling. Mobile DiskOnChip Plus implements Reed-Solomon Error Detection Code (EDC). A hardware-generated, 6-byte error detection signature is computed each time a page (512 bytes) is written to or read from Mobile DiskOnChip Plus.

The TrueFFS driver implements complementary Error Correction Code (ECC). Unlike error detection, which is required on every cycle, error correction is relatively seldom required, hence implemented in software. The combination of Mobile DiskOnChip Plus's built-in EDC mechanism and the TrueFFS driver ensures highly reliable error detection and correction, while providing maximum performance.

The following detection and correction capability is provided for each 512 bytes:

- Corrects up to two 10-bit symbols, including two random bit errors.
- Corrects single bursts up to 11 bits.
- Detects single bursts up to 31 bits and double bursts up to 11 bits.
- Detects up to 4 random bit errors.

3.8 Data Pipeline

Mobile DiskOnChip Plus uses a two-stage pipeline mechanism, designed for maximum performance while enabling on-the-fly data manipulation, such as read/write protection and Error Detection/Error Correction.

3.9 Control & Status

The Control & Status block contains registers responsible for transferring the address, data and control information between the DiskOnChip TrueFFS driver and the flash media. Additional registers are used to monitor the status of the flash media (ready/busy) and of the DiskOnChip controller. For further information on the Mobile DiskOnChip Plus registers, refer to Section 6.3).

3.10 Flash Architecture

A 16MB flash bank consists of 1024 blocks organized in 32 pages, as follows:

- **Page** – Each page contains 512 bytes of user data and a 16-byte extra area that is used to store flash management and EDC/ECC signature data, as shown in Figure 4. A page is the minimal unit for read/write operations.
- **Block** – Each block contains 32 pages (total of 16KB), as shown in Figure 5. A block is the minimal unit that can be erased, and is sometimes referred to as an erase block.

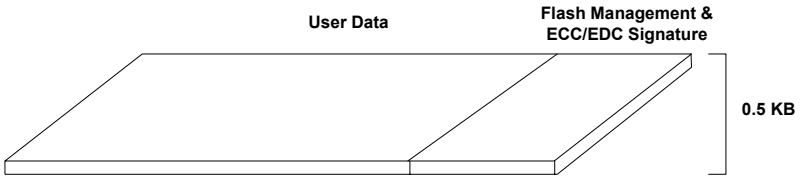


Figure 4: Page Structure

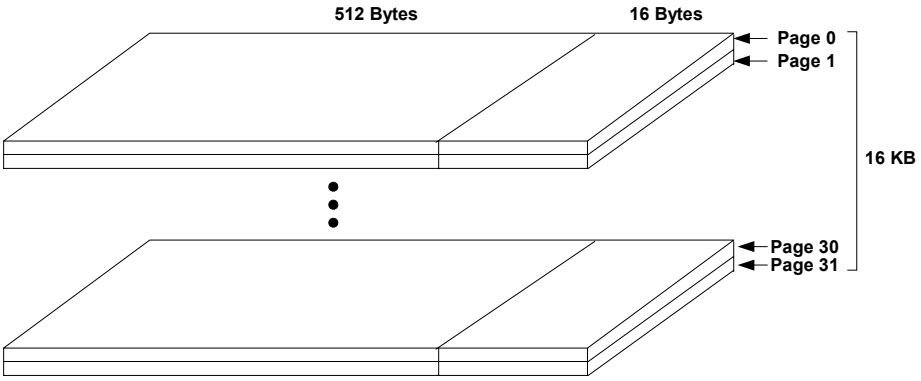


Figure 5: Block Structure

Mobile DiskOnChip Plus 32MB devices are designed with a dual-bank interleave architecture, consisting of two banks of 16MB NAND flash. The interleave architecture allows 16-bit internal flash access instead of the standard 8-bit flash access, thereby doubling performance for read, write and erase operations. The interleave architecture consists of 1024 dual blocks organized in 32 dual pages, for a total capacity of 32MB, as shown in Figure 4.

Mobile DiskOnChip Plus 64MB devices are dual-die devices, consisting of two stacked 32MB devices. Therefore, the interleave architecture, block and page size are similar to that of Mobile DiskOnChip Plus 32MB devices.

4. Hardware Protection

4.1 Method of Operation

Mobile DiskOnChip Plus enables the user to define two partitions that are protected (in hardware) against any combination of read or write operations. The two protected areas can be configured as read protected or write-protected, and are protected by a protection key (i.e. password) defined by the user. Each of the protected areas can be configured separately and can function separately, providing maximal flexibility for the user.

The size and protection attributes (protection key/read/write/changeable/lock) of the protected partition are defined in the media formatting stage (DFORMAT utility or the format function in the TrueFFS SDK).

In order to set or remove a read/write protection, the protection key (i.e., password) must be used, as follows:

- Insert the protection key to remove read/write protection.
- Remove the protection key to set read/write protection.

Mobile DiskOnChip Plus has an additional hardware safety measurement. If the Lock option is enabled (by means of software) and the LOCK# ball is asserted, the protected partition has an additional hardware lock that prevents read/write access to the partition, even with the use of the correct protection key. The LOCK# ball must be asserted during DFORMAT (and later when the partition is defined as changeable) to enable the additional hard-wired safety lock.

Only one partition can be defined as “changeable”; i.e., its password and attributes are fully configurable at any time (from read to write, both or none and visa versa). Note that “un-changeable” partition attributes cannot be changed unless the media is reformatted.

A change of any of the protection attributes causes a reset of the protection mechanism and consequently the removal of *all* device protection keys. That is, if the protection attributes of one partition are changed, the other partition will lose its key-protected read/write protection.

The only way to read or write from a read or write protected partition is to use the insert key call (even DFORMAT does not remove the protection). This is also true for modifying its attributes (key, read, write and lock enable state). Read/write protection is disabled in each one of the following events:

- Power-down
- Change of any protection attribute (not necessarily in the same partition)
- Write operation to the IPL area
- Removal of the protection key.

For further information on hardware protection, please refer to the *TrueFFS Software Development Kit (SDK)* developer guide or application note AP-DOC-057, *Protection and Security-Enabling Features in DiskOnChip Plus.*

4.2 Low-Level Structure of the Protected Area

The first three blocks on Mobile DiskOnChip Plus contain foundry information, the Data Protect structures, IPL code, and bad-block mapping information. See Figure 6.

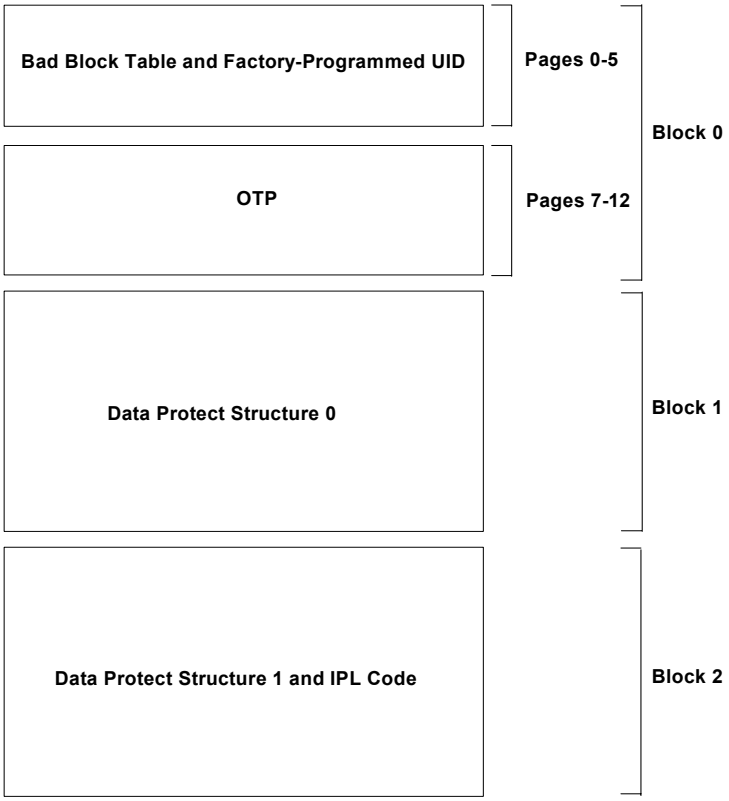


Figure 6: Low Level Format Mobile DiskOnChip Plus

Blocks 0, 1 and 2 in Mobile DiskOnChip Plus contain the following information:

Block 0

- Bad Block Table (page 2). Contains the mapping information to unusable Erase units on the flash media.
- UID (16 bytes). This number is written during the manufacturing stage, and cannot be altered at a later time.
- Customer OTP (occupies pages 26-31). The OTP area is written once and then locked.

Block 1

- Data Protect Structure 0. This structure contains configuration information on one of the two user-defined protected partitions.

Block 2

- Data Protect Structure 1. This structure contains configuration information on one of the two user-defined protected partitions.
- IPL Code (1-2KB). This is the boot code that is downloaded by the DE to the internal boot block.

5. Modes of Operation

Mobile DiskOnChip Plus has three modes of operation:

- Reset
- Normal
- Deep Power-Down

Mode changes can occur due to any of the following events, as shown in Figure 7:

- Assertion of the RSTIN# signal sets the device in Reset mode.
- During power-up, boot detector circuitry sets the device in Reset mode.
- A valid write sequence to Mobile DiskOnChip Plus sets the device in Normal mode. This is done automatically by the TrueFFS driver on power-up (reset sequence end).
- Switching back from Normal mode to Reset mode can be done by a valid write sequence to Mobile DiskOnChip Plus, or by triggering the boot detector circuitry (by soft reset).
- Power-down.
- A valid write sequence, initiated by software, sets the device from Normal mode to Deep Power-Down mode. Four read cycles from offset 0x1FFF set the device back to Normal mode. Alternately, the device can be set back to Normal mode with an extended access time during a read from the Programmable Boot Block (see Section 10.4.1 for read cycle timing).

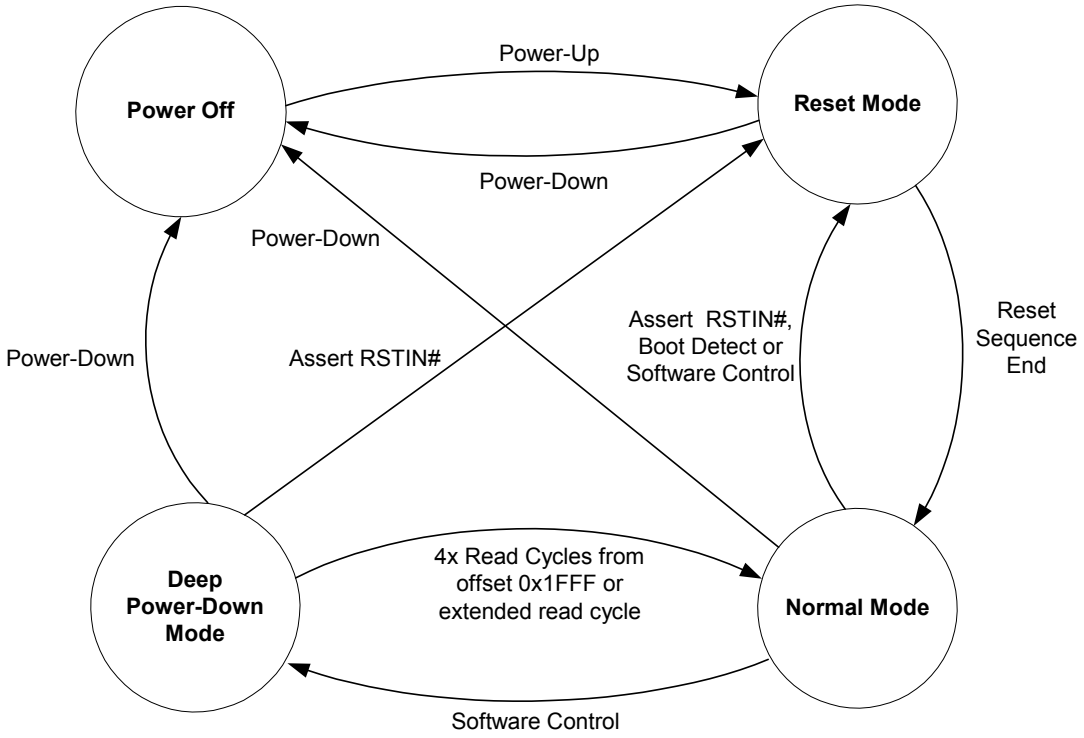


Figure 7: Operation Modes and Related Events

5.1 Normal Mode

This is the mode in which standard operations involving the flash memory are performed. Normal mode is automatically entered when a valid write sequence is sent to the DiskOnChip Control register and Control Confirmation register. The boot detector circuit triggers the software to set the device to Normal mode.

A write cycle occurs when both the CE# and WE# inputs are asserted. Similarly, a read cycle occurs when both the CE# and OE# inputs are asserted. Because the flash controller generates its internal clock from these CPU cycles and some read operations return volatile data, it is essential that the specified timing requirements contained in Section 10.4.1 be met. It is also essential that read and write cycles are not interrupted by glitches or ringing on the CE#, WE#, OE# address inputs. All inputs to Mobile DiskOnChip Plus are Schmidt Trigger types to improve noise immunity.

In Normal mode, Mobile DiskOnChip Plus responds to every valid hardware cycle. When there is no activity, it is possible to reduce the power consumption to a typical deep-power-down current of 10 µA (32MB) or 20 µA (64MB.) by setting the device in Deep Power-Down mode.

5.2 Reset Mode

In Reset mode, Mobile DiskOnChip Plus ignores all write cycles, except for those to the DiskOnChip Control register and Control Confirmation register. All register read cycles return a value of 00H. Before attempting to perform a register read operation, the device is set to Normal mode by the TrueFFS software.

5.3 Deep Power-Down Mode

In Deep Power-Down mode, Mobile DiskOnChip Plus internal high current voltage regulators are disabled to reduce quiescent power consumption to 10 µA (32MB) or 20 µA (64MB) (Typ.). The input buffer signals A[12:0], BHE#, WE#, D[15:0] and OE# (when CE# is negated) are also disabled in this mode:

To enter Deep Power-Down mode, a proper sequence must be written to the DiskOnChip Control registers and DiskOnChip Control Confirmation register, and the CE# input must be negated (CE# = VCC). All other inputs should be VSS or VCC.

In Deep Power-Down mode, write cycles have no effect and read cycles return indeterminate data (Mobile DiskOnChip Plus does not drive the data bus). Entering Deep Power-Down mode and then returning to the previous mode does not affect the value of any register.

To exit Deep Power-Down mode, perform the following sequence:

- Read four times from address 1FFFH. The data returned is undefined.
- Perform a single read cycle from the Programmable Boot Block with an extended access time and address hold time as specified in Section 10.4.1. The data returned will be correct.

Applications that require both Deep Power-Down mode and boot detection require BIOS support to ensure that Mobile DiskOnChip Plus exits from Power-Down mode prior to the expansion ROM scan. Similarly, applications that use Mobile DiskOnChip Plus as a boot ROM must ensure that the device is *not* in Deep Power-Down mode before reading the boot vector/instructions, either by pulsing RSTIN# to the asserted state and waiting for the BUSY# output to be negated, or by entering Reset mode via software.

6. TrueFFS Technology

6.1 General Description

M-Systems' patented TrueFFS technology was designed to maximize the benefits of flash memory while overcoming inherent flash limitations that would otherwise reduce its performance, reliability and lifetime. TrueFFS emulates a hard disk, making it completely transparent to the OS. In addition, since it operates under the OS file system layer (see Figure 8), it is completely transparent to the application.

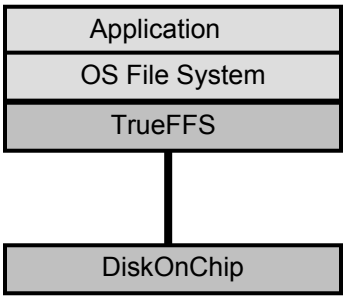


Figure 8: TrueFFS Location in System Hierarchy

TrueFFS technology support includes:

- Binary driver support for all major OSs
- *TrueFFS Software Development Kit (SDK)* developer guide
- *DiskOnChip Boot Software Development Kit (BDK*) developer guide
- Support for all major CPUs, including 8, 16 and 32-bit bus architectures

TrueFFS technology features:

- Block device API
- Flash file system management
- Bad-block management
- Dynamic virtual mapping
- Dynamic and static wear-leveling
- Power failure management
- Implementation of Reed-Solomon EDC/ECC
- Performance optimization
- Compatible with all DiskOnChip products

6.1.1 Built-In Operating System Support

The TrueFFS driver is integrated into all major OSs, including Symbian OS, Windows CE, Pocket PC, Smartphone, OSE, Nucleus, and others. For a complete listing of all available drivers, please refer to M-Systems' website http://www.m-sys.com. It is advised to use the latest driver versions that can be downloaded from the Mobile DiskOnChip Plus web page on the M-Systems site.

6.1.2 TrueFFS Software Development Kit (SDK)

The basic TrueFFS Software Development Kit (SDK) provides the source code of the TrueFFS driver. It can be used in an OS-less environment or when special customization of the driver is required for proprietary OSs.

When using Mobile DiskOnChip Plus as the boot replacement device, the TrueFFS SDK also incorporates in its source code the BDK, software that is required for this configuration (this package is also available separately). Please refer to the DiskOnChip Boot Software Development Kit (BDK) developer guide for further information on using this software package.

6.1.3 File Management

TrueFFS accesses the flash memory within Mobile DiskOnChip Plus through an 8KB window in the CPU memory space. It provides block device API, by using standard file system calls, identical to those used by a mechanical hard disk, to enable reading from and writing to any sector on Mobile DiskOnChip Plus. This makes it compatible with any file system and file system utilities such as diagnostic tools and applications. When using the File Allocation Table (FAT) file system, the data stored on Mobile DiskOnChip Plus uses FAT-16.

Note: Mobile DiskOnChip Plus is shipped unformatted and contains virgin media.

6.1.4 Bad-Block Management

As NAND flash is an imperfect storage media, it contains some bad blocks that cannot be used for storage because of their high error rates. TrueFFS automatically detects and maps bad blocks upon system initialization, ensuring that they are not used for storage. This management process is completely transparent to the user, who remains unaware of the existence and location of bad blocks, while remaining confident of the integrity of data stored. The Bad Block Table on Mobile DiskOnChip Plus is hardware-protected for ensured reliability.

6.1.5 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the *erase cycle limit* or *write endurance limit* and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device. In Mobile DiskOnChip Plus, the erase cycle limit of the flash is 300,000 erase cycles. This means that after approximately 300,000 erase cycles, the erase block begins to make storage errors at a rate significantly higher than the error rate that is typical to the flash.

In a typical application and especially if a file system is used, a specific page or pages are constantly updated (e.g., the page/s that contain the FAT, registry etc.). Without any special handling, these pages would wear out more rapidly than other pages, reducing the lifetime of the entire flash.

To overcome this inherent deficiency, TrueFFS uses M-Systems' patented wear-leveling algorithm. The wear-leveling algorithm ensures that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime. TrueFFS wear-leveling extends the flash lifetime 10 to 15 years beyond the lifetime of a typical application.

Dynamic Wear-Leveling

TrueFFS uses statistical allocation to perform dynamic wear-leveling on newly written data. This not only minimizes the number of erase cycles per block, it also minimizes the total number of erase cycles. Because a block erase is the most time-consuming operation, dynamic wear-leveling has a major impact on overall performance. This impact cannot be noticed during the first write to flash (since there is no need to erase blocks beforehand), but it is more and more noticeable as the flash media becomes full.

Static Wear-Leveling

Areas on the flash media may contain static files, characterized by blocks of data that remain unchanged for very long periods of time, or even for the whole device lifetime. If wear-leveling were only applied on newly written pages, static areas would never be cycled. This limited application of wear-leveling would lower life expectancy significantly in cases where flash memory contains large static areas. To overcome this problem, TrueFFS forces data transfer in static areas as well as in dynamic areas, thereby applying wear-leveling to the entire media.

6.1.6 Power Failure Management

TrueFFS uses algorithms based on “erase after write” instead of "erase before write" to ensure data integrity during normal operation and in the event of a power failure. Used areas are reclaimed for erasing and writing the flash management information into them only *after* an operation is complete. This procedure serves as a check on data integrity.

The “erase after write” algorithm is also used to update and store mapping information on the flash memory. This keeps the mapping information coherent even during power failures. The only mapping information held in RAM is a table pointing to the location of the actual mapping information. This table is reconstructed during power-up or after reset from the information stored in the flash memory.

To prevent data from being lost or corrupted, TrueFFS uses the following mechanisms:

- When writing, copying, or erasing the flash device, the data format remains valid at all intermediate stages. Previous data is never erased until the operation has been completed and the new data has been verified.
- A data sector cannot exist in a partially written state. Either the operation is successfully completed, in which case the new sector contents are valid, or the operation has not yet been completed or has failed, in which case the old sector contents remain valid.

6.1.7 Error Detection/Correction

TrueFFS implements a Reed-Solomon Error Correction Code (ECC) algorithm to ensure data reliability. Refer to Section 3.7 for further information on the EDC/ECC mechanism.

6.1.8 Special Features through I/O Control (IOCTL) Mechanism

In addition to standard storage device functionality, the TrueFFS driver provides extended functionality. This functionality goes beyond simple data storage capabilities to include features such as: format the media, read/write protect, binary partition(s) access, flash defragmentation and other options. This unique functionality is available in all TrueFFS-based drivers through the standard I/O control command of the native file system.

For further information, please refer to the *Extended Functions of the TrueFFS Driver for DiskOnChip* developer guide.

6.1.9 Compatibility

The TrueFFS driver supports all released DiskOnChip products. Upgrading from one product to another requires no additional software integration.

When using different drivers (e.g. TrueFFS SDK, BDK, BIOS extension firmware, etc.) to access Mobile DiskOnChip Plus, the user must verify that all software is based on the same code base version. It is also important to use only tools (e.g. DFORMAT, DINFO, GETIMAGE, etc.) derived from the same version as the firmware version and the TrueFFS drivers used in the application. Failure to do so may lead to unexpected results, such as lost or corrupted data. The driver and firmware version can be verified by the sign-on messages displayed, or by the version information stored in the driver or tool.

Note: When a new M-Systems DiskOnChip product with new features is released, a new TrueFFS version is required.

6.2 8KB Memory Window in Mobile DiskOnChip Plus 32MB

TrueFFS utilizes an 8KB memory window in the CPU address space consisting of four 2KB sections, as depicted in Figure 9. When in Reset mode, the Programmable Boot Block in sections 0 and 3 will show the IPL (1KB), aliased twice, to support systems that search for a checksum at the boot stage from the top and bottom of memory. Read cycles from sections 1 and 2 always return the value 00H to create a fixed and known checksum. When in Normal mode, sections 1 and 2 are used for the internal registers.

The addresses described here are relative to the absolute starting address of the 8KB memory window.

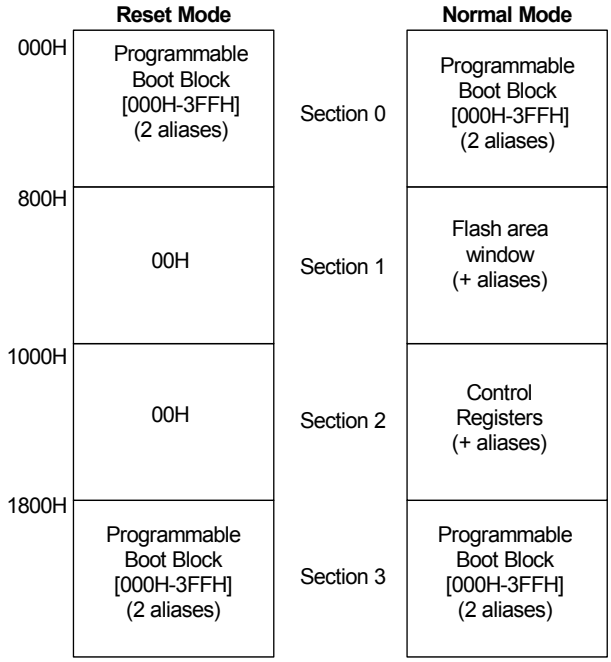


Figure 9: Mobile DiskOnChip Plus 32MB Memory Map

6.3 8KB Memory Window in Mobile DiskOnChip Plus 64MB

TrueFFS utilizes an 8KB memory window in the CPU address space consisting of four 2KB sections, as depicted in Figure 9. When in Reset mode, the Programmable Boot Block in sections 0 and 3 will show the IPL (1KB) of the first 32MB of the dual-die, aliased twice. Read cycles from sections 1 and 2 always return the value 00H to create a fixed and known checksum.

After setting the MAX_ID field in the Configuration register (done by IPL0), the second copy of IPL0 is replaced with the IPL of the second 32MB device of the dual-die, thereby creating a 2KB programmable boot block.

When in Normal mode, sections 1 and 2 are used for the internal registers. The Programmable Boot Block in section 0 contains IPL0 and IPL1. Section 3 contains IPL0 aliased twice.

The addresses described here are relative to the absolute starting address of the 8KB memory window.

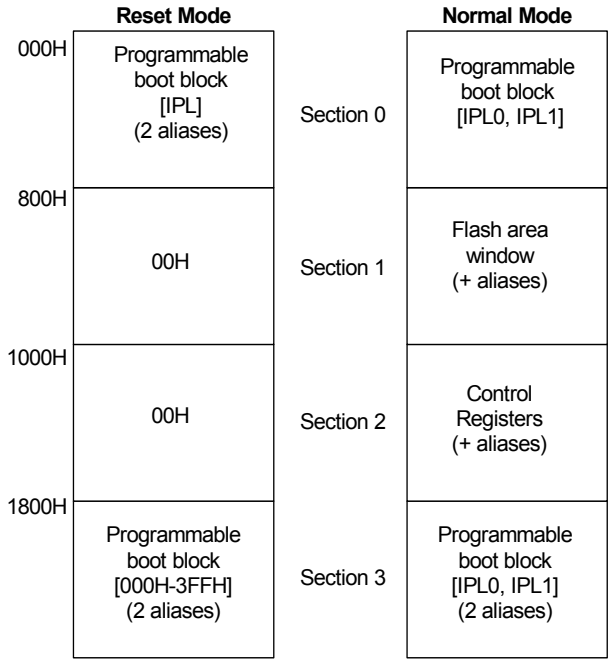


Figure 10: Mobile DiskOnChip Plus 64MB Memory Map

7. Register Descriptions

This section describes various Mobile DiskOnChip Plus registers and their functions, as listed in Table 2. This section can be used to enable the designer to better evaluate DiskOnChip technology.

Table 2: Mobile DiskOnChip Plus Registers

Address (Hex)	Register Name
1000	Chip Identification (ID)
1002	No Operation (NOP)
1004	Test
1006	DiskOnChip Control
1008	Device ID Select
100A	Configuration
100E	Interrupt Control
1046	Toggle Bit
1076	DiskOnChip Control Confirmation

7.1 Definition of Terms

The following abbreviations and terms are used within this section:

RFU — Reserved for future use. This bit is undefined during a read cycle and "don't care" during a write cycle.

RFU_0 — Reserved for future use; when read, this bit always returns the value 0; when written, software should ensure that this bit is always set to 0.

RFU_1 — Reserved for future use; when read, this bit always returns the value 1; when written, software should ensure that this bit is always set to 1.

Reset Value — Refers to the value immediately present after exiting from Reset mode to Normal mode.

7.2 Reset Values

All registers return 00H while in Reset mode. The Reset value written in the register description is the register value after exiting Reset mode and entering Normal mode. Some register contents are undefined at that time (N/A).

7.3 Chip Identification (ID) Register

Description: This register is used to identify the device residing on the host platform. It always returns 41H when read.

Address (hex): 1000

Type: Read only

Reset Value: 40H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
41H							

7.4 No Operation (NOP) Register

Description: A call to this register results in no operation. To aid in code readability and documentation, software should access this register when performing cycles intended to create a time delay.

Address (hex): 1002

Type: Write

Reset Value: None

7.5 Test Register

Description: This register enables software to identify multiple Mobile DiskOnChip Plus devices or multiple aliases in the CPUs memory space. Data written is stored but does not affect the behavior of Mobile DiskOnChip Plus.

Address (hex): 1004

Type: Read/Write

Reset Value: 00H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D[7:0]							

Bit No.	Description
0-7	D[7:0]: Data bits

7.6 DiskOnChip Control Register/Control Confirmation Register

Description: These two registers are identical and contain information on the operation mode of Mobile DiskOnChip Plus. After writing the required value to the DiskOnChip Control register, the complement of that data byte must also be written to the Control Confirmation register. The two writes cycles must not be separated by any other read or write cycles to the Mobile DiskOnChip Plus memory space, except for reads from the Programmable Boot Block space.

Address (hex): 1006/1076

Type: Read/Write

Reset Value: 10H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU_0			RST_LAT	BDET	MDWREN	Mode[1:0]	

Bit No.	Description
0-1	Mode. These bits select the mode of operation, as follows: 00: Reset 01: Normal 10: Deep Power-Down
2	MDWREN (Mode Write Enable). This bit must be set to 1 before changing the mode of operation.
3	BDET (Boot Detect). This bit is set whenever the device has entered Reset mode as a result of the Boot Detector triggering. It is cleared by writing a 1 to this bit.
4	RST_LAT (Reset Latch). This bit is set whenever the device has entered the Reset mode as a result of the RSTIN# input signal being asserted or the internal voltage detector triggering. It is cleared by writing a 1 to this bit.
5-7	Reserved for future use.

7.7 Device ID Select Register

Description: In a cascaded configuration, this register controls which device provides the register space. The value of bits ID[0:1] is compared to the value of the ID configuration input balls, as defined in Section 9.6. The device whose ID input balls matches the value of bits ID[0:1] responds to read and write cycles to register space.

Address (hex): 1008

Type: Read/Write

Reset Value: 00H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU_0						ID[1:0]	

Bit No.	Description
0-1	ID[1:0] (Identification). The device whose ID input balls matches the value of bits ID[0:1] responds to read and write cycles to register space.
2-7	Reserved for future use.

7.8 Configuration Register

Description: This register indicates the current configuration of the device. Unless otherwise noted, the bits are reset only by a hardware reset, and not upon boot detection or any other entry to Reset mode.

Address (hex): 100A

Type: Read/Write (except bit 7, which is Read Only)

Reset Value: X0000X10

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IF_CFG	RFU_0	MAX_ID		RFU		RFU_0	

Bit No.	Description
0-3, 6	Reserved for future use.
4-5	MAX_ID (Maximum Device ID). This field controls the RAM address mapping when multiple devices are used in a cascaded configuration, using the ID[1:0] inputs. It should be programmed to the highest ID value that is found by software in order to map all available boot blocks into usable address space.
7	IF_CFG (Interface Configuration). Reflects the state of the IF_CFG input pin.

7.9 Interrupt Control Register

Description: Interrupts may be generated when the flash transitions from the busy state to the ready state, or by a data protection violation.

Address (hex): 100E

Type: Read/Write

Reset Value: 00H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU_0	IRQ_P	IRQ_F	EDGE	PROT_T	FRDY_T[2:0		

Bit No.	Description
0-2	FRDY_T[2:0] (Flash Ready Trigger). This field determines if an interrupt will be generated when the flash array of Mobile DiskOnChip Plus is ready, as follows: 000: Interrupts are disabled – Holds the IRQ# output in the negated state. 001: Interrupt when flash array is ready.
3	PROT_T (Protection Trigger). When set, an interrupt is generated upon a data protection violation.
4	EDGE (Edge-sensitive interrupt) 0: Specifies level-sensitive interrupts in which the IRQ# output remains asserted until the interrupt is cleared. 1: Specifies edge-sensitive interrupts in which the IRQ# output pulses low.
5	IRQ_F: (Interrupt Request when flash array is ready) Indicates that the IRQ# output has been asserted due to an indication that the flash array is ready. Writing **1** to this bit clears its value, negates the IRQ# output and permits subsequent interrupts to occur.
6	IRQ_P (Interrupt Request on Protection Violation). Indicates that the IRQ# output has been asserted due to a data protection violation. Writing a 1 to this bit clears its value, negates the IRQ# output and permits subsequent interrupts to occur.
7	Reserved for future use.

7.10 Toggle Bit Register

Description: This register identifies the presence of the device.

Address (hex): 1046

Type: Read Only

Reset Value: 82H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU			RFU_0	RFU	TOGGLE	RFU_1	RFU

Bit No.	Description
0, 1, 3-7	Reserved for future use.
2	TOGGLE. This read-only bit toggles on consecutive reads and identifies the presence of the device.

8. Booting from Mobile DiskOnChip Plus

8.1 Introduction

Mobile DiskOnChip Plus can function both as a flash disk and the system boot device. If DiskOnChip is configured as a flash disk, it can operate as the OS boot device. DiskOnChip default firmware contains drivers to enable it to perform as the OS boot device under DOS (see Section 8.2). For other OSs, please refer to the *readme* file of the TrueFFS driver.

If Mobile DiskOnChip Plus is configured as a flash disk and as the system boot device, it contains the boot loader, an OS image and a file system. In such a configuration, Mobile DiskOnChip Plus can serve as the only non-volatile device on board. Refer to Section 8.3.2 for further information on boot replacement.

8.2 Boot Procedure in PC-Compatible Platforms

When used in PC-compatible platforms, Mobile DiskOnChip Plus is connected to an 8KB memory window in the BIOS expansion memory range, typically located between 0C8000H to 0EFFFFH. During the boot process, the BIOS loads the TrueFFS firmware into the PC memory and installs Mobile DiskOnChip Plus as a disk drive in the system. When the operating system is loaded, Mobile DiskOnChip Plus is recognized as a standard disk. No external software is required to boot from Mobile DiskOnChip Plus.

Figure 11 illustrates the location of the Mobile DiskOnChip Plus memory window in the PC memory map.

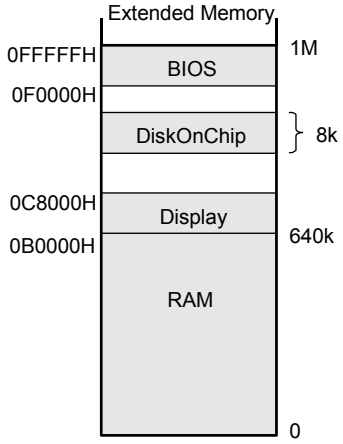


Figure 11: Mobile DiskOnChip Plus Memory Window in the PC Memory Map

After reset, the BIOS code first executes the Power On Self-Test (POST) and then searches for all expansion ROM devices. When Mobile DiskOnChip Plus is located, the BIOS code executes from it the IPL code, located in the XIP portion of the Programmable Boot Block. This code loads the TrueFFS driver into system memory, installs Mobile DiskOnChip Plus as a disk in the system, and then returns control to the BIOS code. The operating system subsequently identifies Mobile DiskOnChip Plus as an available disk. TrueFFS responds by emulating a hard disk.

From this point onward, Mobile DiskOnChip Plus appears as a standard disk drive. It is assigned a drive letter and can be used by any application, without any modifications to either the BIOS set-up or the autoexec.bat/ config.sys files. Mobile DiskOnChip Plus can be used as the only disk in the system, with or without a floppy drive, and with or without hard disks.

The drive letter assigned depends on how Mobile DiskOnChip Plus is used in the system, as follows:

- If Mobile DiskOnChip Plus is used as the only disk in the system, the system boots directly from it and assigns it drive C.
- If Mobile DiskOnChip Plus is used with other disks in the system:
  - Mobile DiskOnChip Plus can be configured as the last drive (the default configuration). The system assigns drive C to the hard disk and drive D to Mobile DiskOnChip Plus.
  - Alternatively, Mobile DiskOnChip Plus can be configured as the system's first drive. The system assigns drive D to the hard disk and drive C to Mobile DiskOnChip Plus.
- If Mobile DiskOnChip Plus is used as the OS boot device when configured as drive C, it must be formatted as a bootable device by copying the OS files onto it. This is done by using the SYS command when running DOS.

8.3 Boot Replacement

8.3.1 PC Architectures

In current PC architectures, the first CPU fetch (after reset is negated) is mapped to the boot device area, also known as the *reset vector*. The reset vector in PC architectures is located at address FFFF0, by using a Jump command to the beginning of the BIOS chip (usually F0000 or E0000). The CPU executes the BIOS code, initializes the hardware and loads Mobile DiskOnChip Plus software using the BIOS expansion search routine (e.g. D0000). Refer to Section 8.2 for a detailed explanation on the boot sequence in PC-compatible platforms.

Mobile DiskOnChip Plus implements both disk and boot functions when it replaces the BIOS chip. To enable this, Mobile DiskOnChip Plus requires a location at two different addresses:

- After power-up, Mobile DiskOnChip Plus must be mapped in F segment, so that the CPU fetches the reset vector from address FFFF0, where Mobile DiskOnChip Plus is located.
- After the BIOS code is loaded into RAM and starts execution, Mobile DiskOnChip Plus must be reconfigured to be located in the BIOS expansion search area (e.g. D0000) so it can load the TrueFFS software.

This means that the CS# signal must be remapped between two different addresses. For further information on how to achieve this, refer to application note AP-DOC-047, *Designing DiskOnChip as a Flash Disk and Boot Device Replacement*.

8.3.2 Non-PC Architectures

In non-PC architectures, the boot code is executed from a boot ROM, and the drivers are usually loaded from the storage device.

When using Mobile DiskOnChip Plus as the system boot device, the CPU fetches the first instructions from the Mobile DiskOnChip Plus Programmable Boot Block, which contains the IPL. Since in most cases this block cannot hold the entire boot loader, the IPL runs minimum initialization, after which the Secondary Program Loader (SPL) is copied to RAM from flash. The remainder of the boot loader code then runs from RAM.

The IPL and SPL are located in a separate (binary) partition on Mobile DiskOnChip Plus, and can be hardware protected if required.

For further information on software boot code implementation, refer to application note AP-DOC-070, *Writing an IPL for DiskOnChip Plus 32/64MByte.*

9. Design Considerations

9.1 Design Environment

Mobile DiskOnChip Plus provides a complete design environment consisting of:

- Evaluation Boards (EVB) for enabling software integration and development with Mobile DiskOnChip Plus, even before the target platform is available. An EVB with Mobile DiskOnChip Plus soldered on it is available with an ISA standard connector and a PCI standard connector for immediate plug-and-play usage.
- Programming solutions:
  - GANG programmer
  - Programming house
  - On-board programming
- TrueFFS Software Development Kit (SDK) and BDK
- DOS utilities:
  - DFORMAT
  - GETIMG/PUTIMG
  - DINFO
- Documentation:
  - Data sheet
  - Application notes
  - Technical notes
  - Articles
  - White papers

Please visit the M-Systems website (www.m-sys.com) for the most updated documentation, utilities and drivers.

9.2 System Interface

Mobile DiskOnChip Plus uses an SRAM-like interface that can easily be connected to any microprocessor bus. With a standard interface, it requires 13 address lines, 8 data lines and basic memory control signals (CE#, OE#, WE#), as shown in Figure 12 below. Typically, Mobile DiskOnChip Plus can be mapped to any free 8KB memory space. In a PC compatible platform, it is usually mapped into the BIOS expansion area. If the allocated memory window is larger than 8KB, an automatic anti-aliasing mechanism prevents the firmware from being loaded more than once during the ROM expansion search.

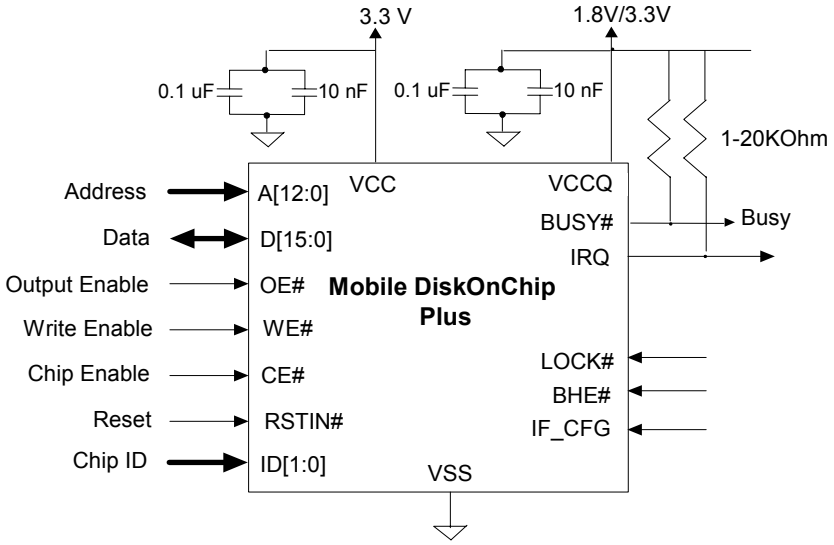


Figure 12: System Interface

Notes: 1. The 0.1 µF and the 10 nF low-inductance high-frequency capacitors must be attached to each of the device's VCC and VSS balls. These capacitors must be placed as close as possible to the package leads.

2. Mobile DiskOnChip Plus is an edge-sensitive device. CE#, OE# and WE# should be properly terminated (according to board layout, serial parallel or both terminations) to avoid signal ringing.

3. All capacities support the standard interface.

9.3 Connecting Signals

Mobile DiskOnChip Plus uses standard SRAM-like control signals, which should be connected as follows:

- Address (A[12:0]) – Connect these signals to the host address bus.
- Data (D[15:0]) – Connect these signals to the host data bus.
- Write (WE#) and Output Enable (OE#) – Connect these signals to the host WR# and RD# signals, respectively.
- Chip Enable (CE#) – Connect this signal to the memory address decoder.
- Chip Identification (ID[0:1]) –Both signals must be connected to GND if only one Mobile DiskOnChip Plus is being used. If more than one, refer to Section 9.6 for more information on cascaded configuration.
- Power-On Reset In (RSTIN#) – Connect this signal to the host Power-On Reset signal.
- Busy (BUSY#) – Connect this signal to an input port. It indicates when the device is ready for first access after hardware reset.
- Interrupt (IRQ#) – Connect this signal to the host interrupt to release the host of this task and improve performance.
- Byte High Enable (BHE#) – This signal definition is compatible with 16 bit platforms that use the BHE#/BLE# protocol. This signal is only relevant during the boot phase.
- Hardware Lock (LOCK#) – This signal prevents the use of the write protect key to disable the protection.
- 8/16 Bit Configuration (IF_CFG) – This signal is required for configuring the device for 8 or 16-bit access mode. When negated, the device is configured for 8-bit access mode. When asserted, 16-bit access mode is operative.

Mobile DiskOnChip Plus derives its internal clock signal from the CE#, OE# and WE# inputs. Since access to Mobile DiskOnChip Plus' registers is volatile, much like a FIFO or UART, ensure that these signals have clean rising and falling edges, and are free from ringing that can be interpreted as multiple edges. PC board traces for these three signals must either be kept short or properly terminated to guarantee proper operation.

9.4 Implementing the Interrupt Mechanism

9.4.1 Hardware Configuration

To configure the hardware, connect the IRQ# pin to the host interrupt input.

Note: A nominal 10 KΩ pull-up resistor must be connected to this pin.

9.4.2 Software Configuration

Configuring the software to support the IRQ# interrupt is performed in two stages.

Stage 1

Configure the software so that upon system initialization, the following steps occur:

1. The correct value is written to the Interrupt Control register to configure Mobile DiskOnChip Plus for:
   - Interrupt source: Flash ready and/or data protection
   - Output sensitivity: Either edge or level triggered

   Note: Refer to Section 7.9 for further information on the value to be written to this register.
2. The host interrupt is configured to the selected input sensitivity, either edge or level.
3. The handshake mechanism between the interrupt handler and the OS is initialized.
4. The interrupt service routine to the host interrupt is connected and enabled.

Stage 2

Configure the software so that for every long flash I/O operation, the following steps occur:

1. The correct value is written to the Interrupt Control register to enable the IRQ# interrupt.

   Note: Refer to Section 7.9 for further information on the value to be written to this register.

2. The flash I/O operation starts.
3. Control is returned to the OS to continue other tasks. When the IRQ# interrupt is received, other interrupts are disabled and the OS is flagged.
4. The OS either returns control immediately to the TrueFFS driver, or waits for the appropriate condition to return control to the TrueFFS driver.

For further information on implementing the interrupt mechanism, please refer to application note AP-DOC-063, *Improving the Performance of DiskOnChip Plus Devices Using the IRQ# Pin.*

9.5 Platform-Specific Issues

The following section describes hardware design issues.

9.5.1 Wait State

Wait states can be implemented only when Mobile DiskOnChip Plus is designed in a bus that supports a Wait state insertion, and supplies a WAIT signal.

9.5.2 Big and Little Endian Systems

Power PC, ARM, and other RISC processors can use either Big or Little Endian systems. Mobile DiskOnChip Plus uses the Little Endian system. Therefore, bytes D[7:0] are its Least Significant Byte (LSB) and bytes D[15:8] are its Most Significant Byte (MSB). Within the bytes, bit D0 and bit D8 are the least significant bits of their respective byte. When connecting Mobile DiskOnChip Plus to a device that supports the Big Endian system, make sure to that the bytes of the CPU and Mobile DiskOnChip Plus match.

Note: Processors like the Power PC also change the bit ordering within the bytes. Failing to follow these rules results in improper connection of Mobile DiskOnChip Plus and prevents the TrueFFS driver from identifying Mobile DiskOnChip Plus.

For further information on how to connect Mobile DiskOnChip Plus to support CPUs that use the Big Endian system, refer to the application note for the relevant CPU.

9.5.3 Busy Signal

The Busy signal (BUSY#) indicates that Mobile DiskOnChip Plus has not yet completed internal initialization. After reset, BUSY# is asserted while the IPL is downloaded into the internal boot block and the Data Protection Structures (DPS) are downloaded to the Protection State Machines. After the download process is completed, BUSY# is negated. It can be used to delay the first access to Mobile DiskOnChip Plus until it is ready to accept valid cycles.

Note: The TrueFFS driver does NOT use this signal to indicate that the flash is in busy state (e.g. program, read, or erase).

9.5.4 Working with 8/16/32-Bit Systems with a Standard Interface

When using a standard interface, Mobile DiskOnChip Plus can be configured for 8-bit, 16-bit or 32-bit bus operations.

8-Bit (Byte) Data Access Mode

When configured for 8-bit operation, IF_CFG should be negated. Data should then be driven only on the low data bus signals D[7:0]. D[15:8] and BHE# are internally pulled up and may be left floating.

16-Bit (Word) Data Access Mode

When configured for 16-bit operation, IF_CFG should be asserted. The following definition is compatible with 16-bit platforms using the BHE#/BLE# protocol:

- When the host BLE# signal asserts Mobile DiskOnChip Plus A0, data is valid on D[7:0].
- When the host BHE# signal asserts Mobile DiskOnChip Plus BHE#, data is valid on D[15:8].
- When both A[0] and BHE# are at logic 0, data is valid on D[15:0].
- No data is transferred when both BHE# and A0 are logic 1.
- 16-bit hosts that do not support byte transfers may hardwire the A0 and BHE# inputs to logic 0.

Table 3 shows the active data bus lanes in 16-bit configuration.

Table 3: Active Data Bus Lanes in 16-Bit Configuration

Inputs		Data Bus Activity		Transfer Type
BHE#	**A0**	**D[7:0]**	**D[15:8]**	
0	0	✓	✓	Word
0	1		✓	Odd Byte
1	0	✓		Even Byte
1	1			No Operation

32-Bit (Word) Data Access Mode

In a 32-bit bus system that cannot execute byte- or word-aligned accesses, the system address lines SA0 and SA1 are always zero. Consecutive long-words (32-bit) are differentiated by SA2 toggling. Therefore, in 32-bit systems that support only 32-bit data access cycles, DiskOnChip A1 is connected to the first system address bit that toggles, i.e. SA2. DiskOnChip A0 is connected to VSS to configure it for 16-bit operation (see Table 3).

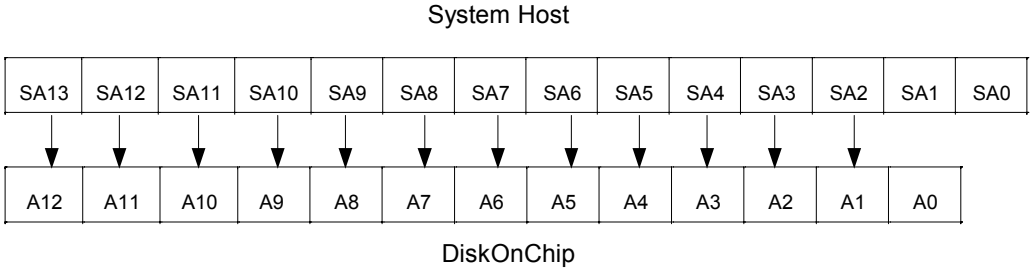


Figure 13: 32-Bit (Word) Data Access Mode

Note: The prefix "S" indicates system host address lines

TrueFFS Driver Modifications

TrueFFS supports a wide range of OSs (see Section 6.1.1). The TrueFFS driver is set to work in 8-bit data access mode as the default. To support 16-bit/32-bit data access modes and their related memory window allocations, TrueFFS must be modified. In Windows CE and Windows NT Embedded, these changes can be implemented through the Registry Entries. In all other cases, some minor customization is required in the driver. Please refer to the *readme* of each specific driver for further information.

9.6 Device Cascading

Up to four Mobile DiskOnChip Plus 32MB devices or up to two Mobile DiskOnChip Plus 64MB devices can be cascaded, for up to 128MB capacity. No external decoding circuitry or system redesign is required.

ID[1:0] ball values determine the identity of each device. Systems with only one device must configure it as device 0 by setting ID[1:0] to 00H. Additional devices should be configured as device 1, device 2 and device 3 by setting ID[1:0] to 01H, 10H and 11H, respectively.

Note: As Mobile DiskOnChip Plus 64MB is a dual-die comprised of two internally stacked Mobile DiskOnChip Plus 32MB devices, only two Mobile DiskOnChip Plus 64MB devices may be cascaded.

When devices are cascaded, all I/O balls must be wired in common, including the BUSY# output. The ID input balls should be strapped to VCC or VSS, according to the location of each device. To communicate with a particular device, its ID must be written into the Device ID Select register (see Section 7.7). Only the device whose ID corresponds with this value responds to read or write cycles to registers.

Figure 14 illustrates the configuration required to cascade four devices on the host bus. Only the relevant cascading signals are included in this figure, although all other signals must also be connected.

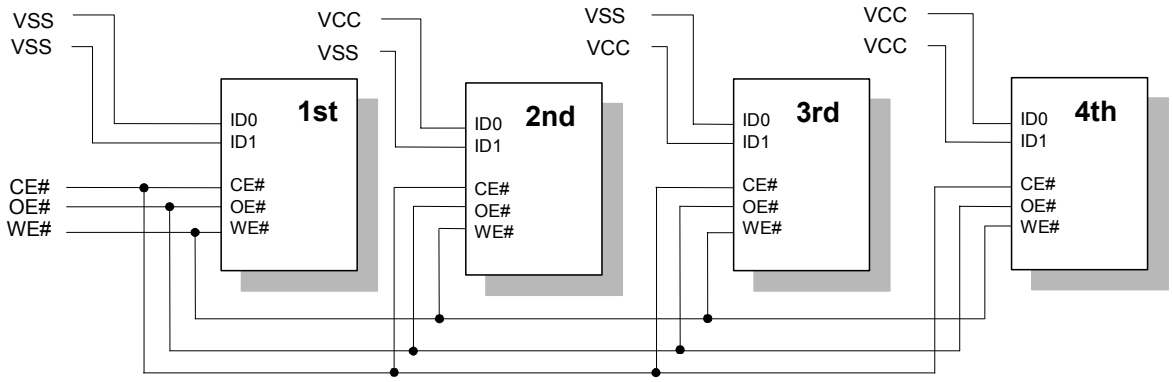


Figure 14: Cascading Configuration for Four Devices

9.6.1 Memory Map in a Cascaded Configuration

When cascading Mobile DiskOnChip Plus devices, the Programmable Boot Block size is enlarged by 1KB for each additional device in the configuration. When the maximum number of devices is connected in a cascaded configuration, a boot block size of 4KB is available.

The MAX_ID field of the Configuration register can be programmed with the maximum ID value used to enable access to the boot block of each device in a separate address space.

Initially at power-up, only device 0 responds to reads from the boot block address space with its 1KB of data aliased at addresses 0K, 1K, 6K and 7K. Figure 15 shows the memory map when four devices are connected in a cascaded configuration, and the location of each IPL.

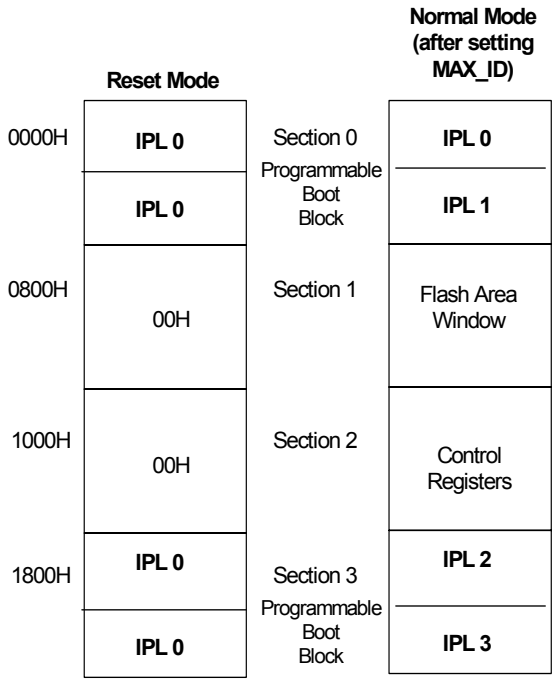


Figure 15: Memory Map in a Cascaded Configuration

10. Product Specifications

10.1 Environmental Specifications

10.1.1 Operating Temperature Ranges

Commercial Temperature Range: 0°C to 70°C

Extended Temperature Range: -40°C to +85°C

10.1.2 Thermal Characteristics

Table 4: Thermal Characteristics

Thermal Resistance (°C/W)	
Junction to Case (θ_{JC}): 30	Junction to Ambient (θ_{JA}): 85

10.1.3 Humidity

10% to 90% relative, non-condensing.

10.1.4 Endurance

Mobile DiskOnChip Plus is based on NAND flash technology, which guarantees a minimum of 300,000 erase cycles. Due to the TrueFFS wear-leveling algorithm, the life span of all DiskOnChip products is significantly prolonged. M-Systems' website (www.m-sys.com) provides an online life-span calculator to facilitate application-specific endurance calculations.

10.2 Disk Capacity

Table 5: Disk Capacity 32MB (in bytes)

DOS 6.22		VxWorks	
Formatted Capacity	**Sectors**	**Formatted Capacity**	**Sectors**
32,800,768	64,064	32,724,992	63,916

Table 6: Disk Capacity 64MB (in bytes)

DOS 6.22		VxWorks	
Formatted Capacity	**Sectors**	**Formatted Capacity**	**Sectors**
65,329,152	127,596	65,568,768	128,064

10.3 Electrical Specifications

10.3.1 Absolute Maximum Ratings

Table 7: Absolute Maximum Ratings

Parameter	Symbol	Rating[1]	Units	Notes
DC Core Supply Voltage	VCC	-0.6 to 4.6	V	
DC I/O Supply Voltage	VCCQ[3]	-0.6 to 4.6	V	
Input Pin Voltage	V_{IN}[2]	-0.6 to VCCQ+0.3, 4.6V max	V	
Input pin Current	I_{IN}	-10 to 10	mA	25 °C
Storage Temperature	T_{STG}	-55 to 150	°C	
Lead Temperature	T_{LEAD}	260	°C	10 sec

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The voltage on any pin may undershoot to -2.0 V or overshoot to 6.6V for less than 20 ns.

10.3.2 Capacitance

Table 8: Capacitance (32MB)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V			10	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V			10	pF

Capacitance is not 100% tested.

Table 9: Capacitance (64MB)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V			20	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V			20	pF

Capacitance is not 100% tested.

10.3.3 DC Electrical Characteristics Over Operating Range

Table 10: DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Core Supply Voltage	VCC		2.7	3.3	3.6	V
I/O Supply Voltage	VCCQ		2.7	3.3	3.6	V
High-level Input Voltage	V_{IH}		2.1			V
Low-level Input Voltage	V_{IL}				0.7	V
High-level Output Voltage	V_{OH}	$I_{Oh} = I_{Ohmax}$	2.4			V
Low-level Output Voltage	V_{OL}	$I_{Ol} = I_{Olmax}$			0.4	V
High-level Output Current	$I_{OHM\ AX}$	3.0V < VCCQ < 3.6V	-4			mA
		2.7V < VCCQ < 3.0V	-4			
Low-level Output Current	I_{OHMAX}	3.0V < VCCQ < 3.6V	8			mA
		2.7V < VCCQ < 3.0V	5			
Input Leakage Current[1,]	I_{ILK}				±10	µA
Output Leakage Current	I_{IOLK}				±10	µA
Active Supply Current[3]	I_{CC}	Cycle Time = 100 ns (32MB)		25	45	mA
		Cycle Time = 100 ns (64MB)		50	90	
Standby Supply Current VCC Pins[4]	I_{CCS}	Deep Power-Down mode[5] (32MB)		10	40	µA
		Deep Power-Down mode[5] (64MB)		20	80	

1. The CE# input includes a pull-up resistor which sources 0.3~1.4 uA at Vin=0V

2. The D[15:8] and BHE# inputs each include a pull-up resistor which sources 58 ~ 234 µA at Vin = 0V when IF_CFG is a logic-0

3. VCC = VCCQ = 3.3V, Outputs open

4. If DiskOnChip is not set to Deep Power-Down mode and is not accessed for read/write operation, standby supply current is 400 µA (typ.) to 600 µA (max.)

5. Deep Power-Down mode is achieved by asserting RSTIN# (when in Normal mode) or writing the proper write sequence to the DiskOnChip registers, and asserting the CE# input = VCCQ. See Section 5.3 for further details.

10.3.4 AC Operating Conditions

Environmental and timing specifications are based on the following conditions.

Table 11: AC Test Conditions

Parameter	VCCQ=2.7-3.6V
Ambient Temperature (TA)	-40°C to +85°C
Supply Voltage	2.7V to 3.6V
Input Pulse Levels	0V to 2.7V
Input Rise and Fall Times	3ns
Input Timing Levels	1.5V
Output Timing Levels	1.5V
Output Load	100pF

10.4 Timing Specifications

10.4.1 Read Cycle Timing Standard Interface

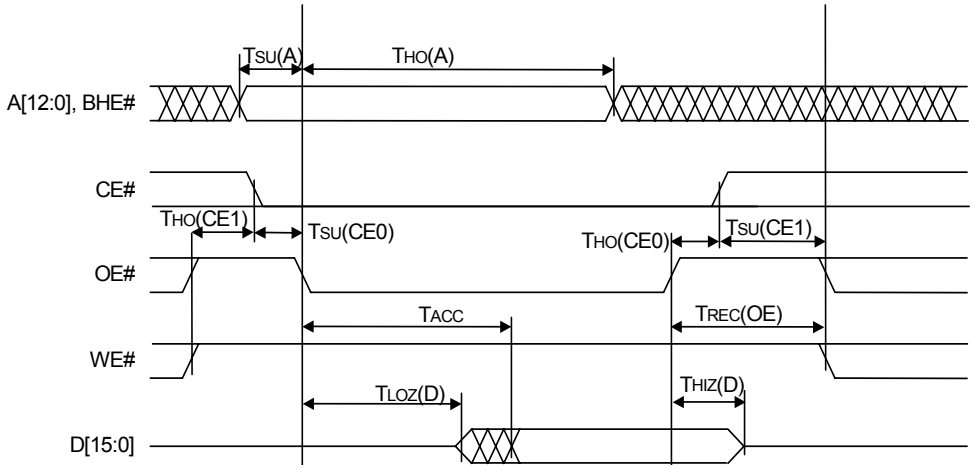


Figure 16: Standard Interface Read Cycle Timing

Table 12: Standard Interface Read Cycle Timing Parameters – Mobile DiskOnChip Plus 32/64MB

Symbol	Description	32MB/64 (256/512 Mb) VCC=VCCQ= 2.7 to 3.6V		Units
		Min	Max	
Tsu(A)	Address to OE# ↓ setup time	10		ns
Tho(A)	OE# ↓ to Address hold time	28		ns
Tsu(CE0)	CE# ↓ to OE# ↓ setup time[1]	—		ns
Tho(CE0)	OE# ↑ to CE# ↑ hold time[2]	—		ns
Tho(CE1)	OE# or WE# ↑ to CE# ↓ hold time	6		ns
Tsu(CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	6		ns
Trec(OE)	OE# negated to start of next cycle	20		ns
Tacc	Read access time (RAM)[3,4]		103	ns
	Read access time (all other addresses)[3]		85	ns
Tloz(D)	OE# ↓ to D driven[5]	10		ns
Thiz(D)	OE# ↑ to D Hi-Z delay		25	ns

1. CE# may be asserted any time before or after OE# is asserted. If CE# is asserted after OE#, all timing relative to when OE# was asserted will be referenced to the time CE# was asserted.

2. CE# may be negated any time before or after OE# is negated. If CE# is negated before OE#, all timing relative to when OE# was negated will be referenced to the time CE# was negated.

3. The boot block is located at addresses 0000~07FFH and 1800H~1FFFH. Registers located at addresses 0800H~17FFH have a faster access time than the boot block. Access to the boot block is not required after the boot process has completed.

4. Systems that do not access the boot block may implement only the read access timing for "all other registers". This will increase the systems performance, however it will prevent access to the boot block.

5. No load (C_L = 0 pF).

10.4.2 Write Cycle Timing Standard Interface

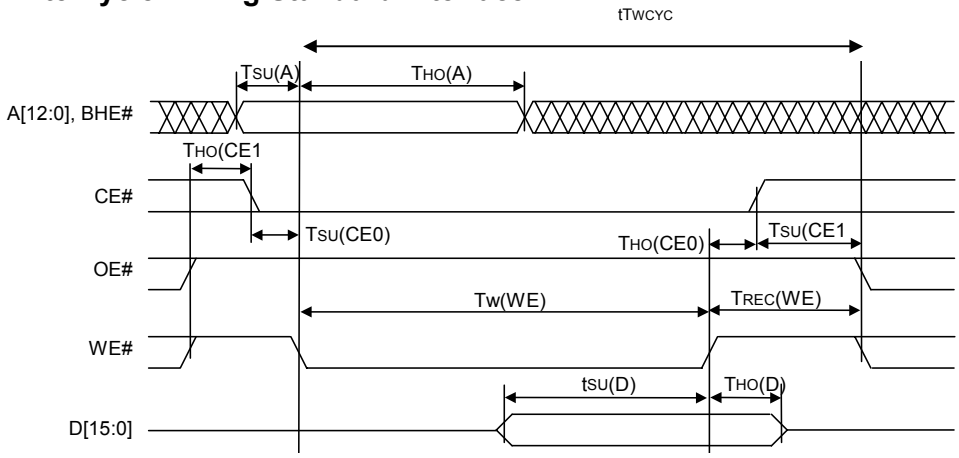


Figure 17: Standard Interface Write Cycle Timing

Table 13: Standard Interface Write Cycle Parameters

Symbol	Description	32/64MB (256/512Mb)		Units
		VCC=VCCQ= 2.7 to 3.6V		
		Min	Max	
tSU (A)	Address to WE# ↓ setup time	10		ns
tho (A)	WE# ↓ to Address hold time	28		ns
tw(WE)	WE# asserted width	47		ns
T_{WCYC}	Write Cycle Time	80		
tsu (CE0)	CE# ↓ to WE# ↓ setup time[1]	—		ns
tho (CE0)	WE# ↑ to CE# ↑ hold time[2]	—		ns
tho (CE1)	OE# or WE# ↑ to CE# ↓ hold time	6		ns
tsu (CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	6		ns
trec (WE)	WE# ↑ to start of next cycle	20		ns
tsu(D)	D to WE# ↑ setup time	51		ns
tho (D)	WE# ↑ to D hold time	0		ns

1. CE# may be asserted any time before or after WE# is asserted. If CE# is asserted after WE#, all timing relative to WE# asserted should be referenced to the time CE# was asserted.

2. CE# may be negated any time before or after WE# is negated. If CE# is negated before WE#, all timing relative to WE# negated will be referenced to the time CE# was negated.

10.4.3 Power-Up Timing

Mobile DiskOnChip Plus is reset by assertion of the RSTIN# input. When this signal is negated, DiskOnChip initiates a download procedure from the flash memory into the internal Programmable Boot Block. During this procedure, Mobile DiskOnChip Plus does not respond to read or write accesses.

Host systems must therefore observe the requirements described below for first access to Mobile DiskOnChip Plus. Any of the following methods may be employed to guarantee first-access timing requirements:

a. Use a software loop to wait at least Tp (BUSY1) before accessing the device after the reset signal is negated.

b. Poll the state of the BUSY# output.

c. Use the BUSY# output to hold the host CPU in wait state before completing the first access.

Host systems that boot from Mobile DiskOnChip Plus must employ option c), or use another method to guarantee the required timing for first-time access.

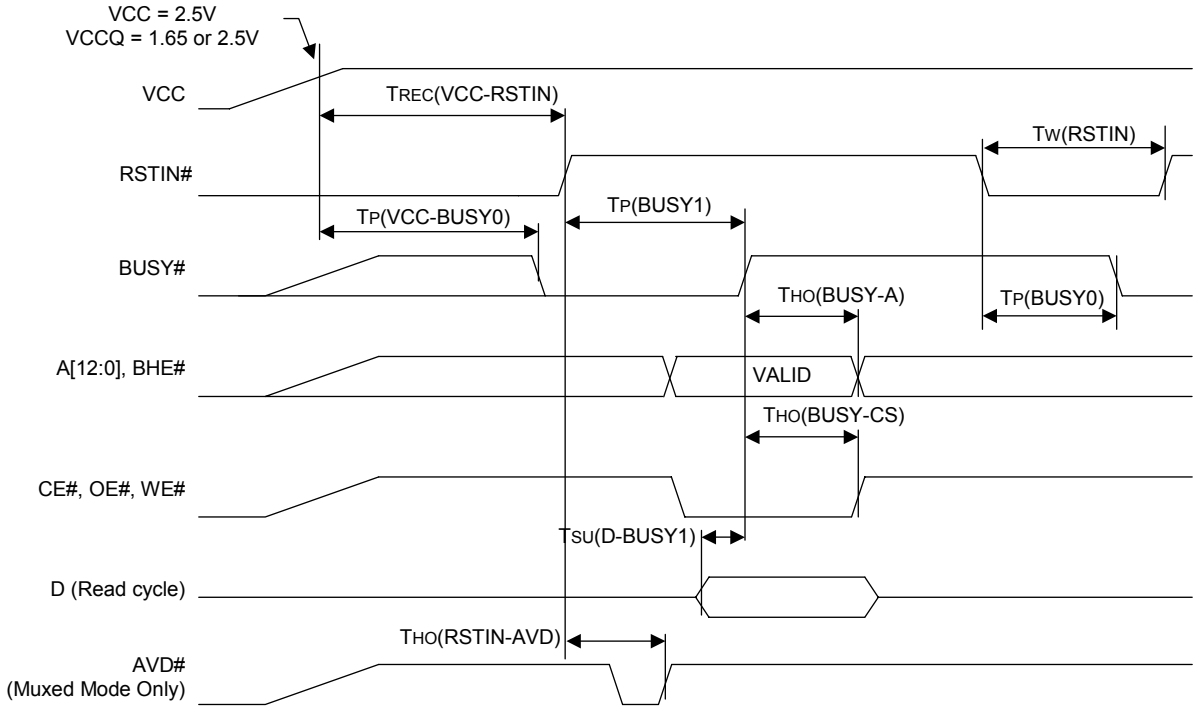


Figure 18: Reset Timing

Table 14: Power-Up Timing Parameters

Symbol	Description	Min	Max	Units
TREC (VCC-RSTIN)[1]	VCC/VCCQ stable to RSTIN# ↑	500		µs
Tp (VCC-BUSY0)[1]	VCC/VCCQ stable to BUSY# ↓		500	µs
TW (RSTIN)	RSTIN# asserted pulse width	30		ns
TP (BUSY0)	RSTIN# ↓ to BUSY# ↓		50	ns
TP (BUSY1)[2]	RSTIN# ↑ to BUSY# ↑		1.3	ms
THO (BUSY-CE)[3]	BUSY# ↑ to CE# ↑	0		ns
TSU (D-BUSY1)[3]	Data valid to BUSY# ↑	0		ns
Tho(RSTIN-AVD)[4]	RSTIN# ↑ to AVD# low hold	70		ns

1. Specified from the final positive crossing of Vcc above 2.7V.

2. If the assertion of RSTIN# occurs during a flash erase cycle, this time could be extended by up to 500 µS.

3. Normal read/write cycle timing applies. This parameter applies only when the cycle is extended until the negation of the BUSY# signal.

4. Applies to multiplexed interface only.

10.4.4 Interrupt Timing

The interrupt timing is illustrated in Figure 19, and described in Table 15.

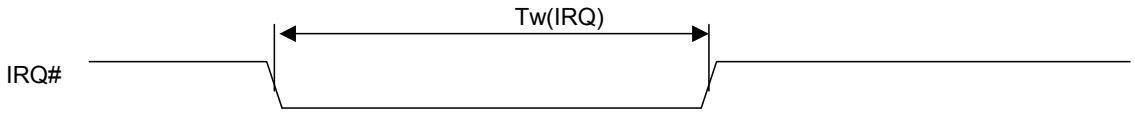


Figure 19: IRQ# Pulse Width in Edge Mode

Table 15: Interrupt Timing

Symbol	Description	Min	Max	Units
Tw(IRQ)	IRQ# asserted pulse width (edge mode)	300	800	nS

10.5 Mechanical Dimensions

See Figure 20 for the mechanical dimensions of the FBGA package.

FBGA Dimensions (32MB): 9.0±0.20 mm x 12.0±0.20 mm x 1.2±0.1 mm
FBGA Dimensions (64MB): 9.0±0.20 mm x 12.0±0.20 mm x 1.4±0.1 mm
Ball Pitch: 0.8mm

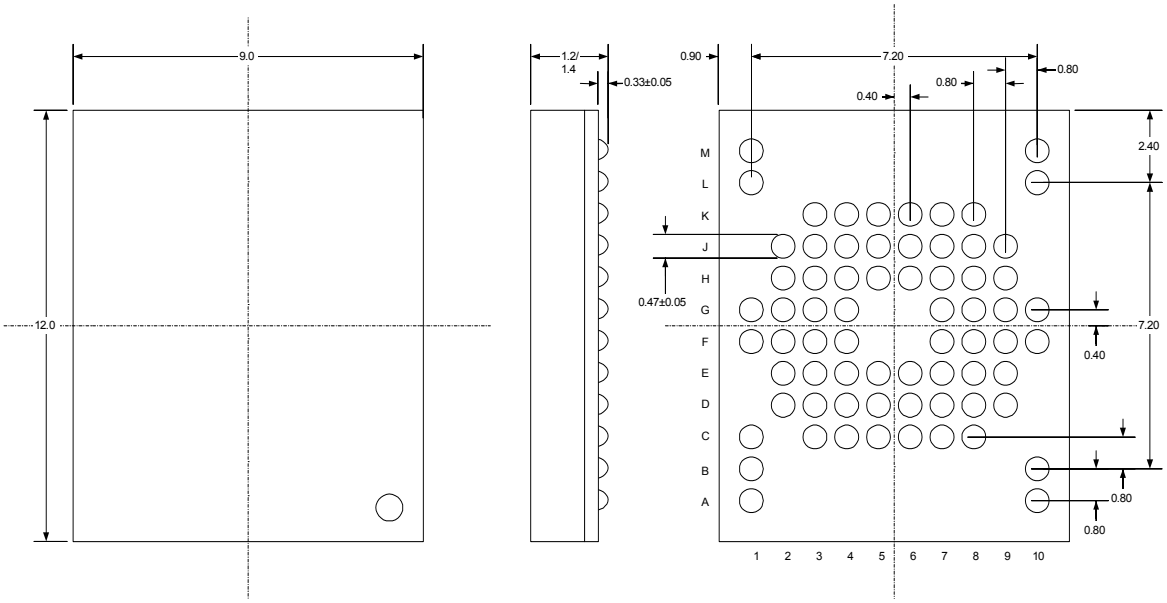


Figure 20: Mechanical Dimensions of the FBGA Package

11. Ordering Information

MD3831-Dxx-V3-T-C

MD: M-Systems DiskOnChip	MD3831 – Mobile DiskOnChip Plus FBGA	
	MD3331 – Mobile DiskOnChip Plus dual-die FBGA	
D: Capacity	32, 64	Capacity: 32MB (256Mb) or 64MB (512Mb)
V: Voltage	V3	Core and I/O Voltage: 3.3V
T: Temperature Range	Blank	Commercial: 0°C to +70°C
	X	Extended: –40°C to +85°C
C: Composition	Blank	Regular
	P	Lead-free

Summary of Supported Configurations

Capacity	Package	Temperature Range[1]	Type	Order Information
32 MByte (256 Mbit)	9x12 mm FBGA	Commercial	Regular	MD3831-D32-V3
		Extended	Regular	MD3831-D32-V3-X
		Commercial	Lead-free	MD3831-D32-V3-P
		Extended	Lead-free	MD3831-D32-V3-X-P
64 MByte (512 Mbit)		Commercial	Regular	MD3331-D64-V3
		Extended	Regular	MD3331-D64-V3-X
		Commercial	Lead-free	MD3331-D64-V3-P
		Extended	Lead-free	MD3331-D64-V3-X-P
N/A		N/A	Daisy-Chain	MD3831-D00-DAISY

1. Commercial (0°C - 70°C), Extended (-40°C - 85°C)

Appendix B: 32Mbit CMOS Pseudo Static RAM (PSRAM) Data Sheet

Note: Information regarding packaging, ball assignment and package-level specifications does not apply to DiskOnChip-based MCP. For DiskOnChip-based MCP specifications, refer to Sections 1 and 2 of this data sheet.

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

2,097,152-WORD BY 16-BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC51WHM516AXGN is a 33,554,432-bit pseudo static random access memory(PSRAM) organized as 2,097,152 words by 16 bits. Using Toshiba's CMOS technology and advanced circuit techniques, it provides high density, high speed and low power. The device operates single power supply. The device also features SRAM-like W/R timing whereby the device is controlled by $\overline{CE1}$, $\overline{OE}$, and $\overline{WE}$ on asynchronous. The device has the page access operation. Page size is 8 words. The device also supports deep power-down mode, realizing low-power standby.

FEATURES

- Organized as 2,097,152 words by 16 bits
- Single power supply voltage of 2.6 to 3.1 V
- Direct TTL compatibility for all inputs and outputs
- Deep power-down mode: Memory cell data invalid
- Page operation mode :
  Page read operation by 8 words
- Logic compatible with SRAM R/W($\overline{WE}$) pin
- Standby current
  Standby 70 μA
  Deep power-down standby 5 μA
- Access Times:

	TC51WHM516AXGN	
	65	70
Access Time	65 ns	70 ns
$\overline{CE1}$ Access Time	65 ns	70 ns
$\overline{OE}$ Access Time	25 ns	25 ns
Page Access Time	30 ns	30 ns

- Packages:
  P-TFBGA48-6mm×7mm 0.75mm pitch
  (Weight: g typ.)

PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CE1}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	V_{SS}	I/O12	A17	A7	I/O4	V_{DD}
E	V_{DD}	I/O13	NC	A16	I/O5	V_{SS}
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	A19	A12	A13	$\overline{WE}$	I/O8
H	A18	A8	A9	A10	A11	A20

(FBGA48)

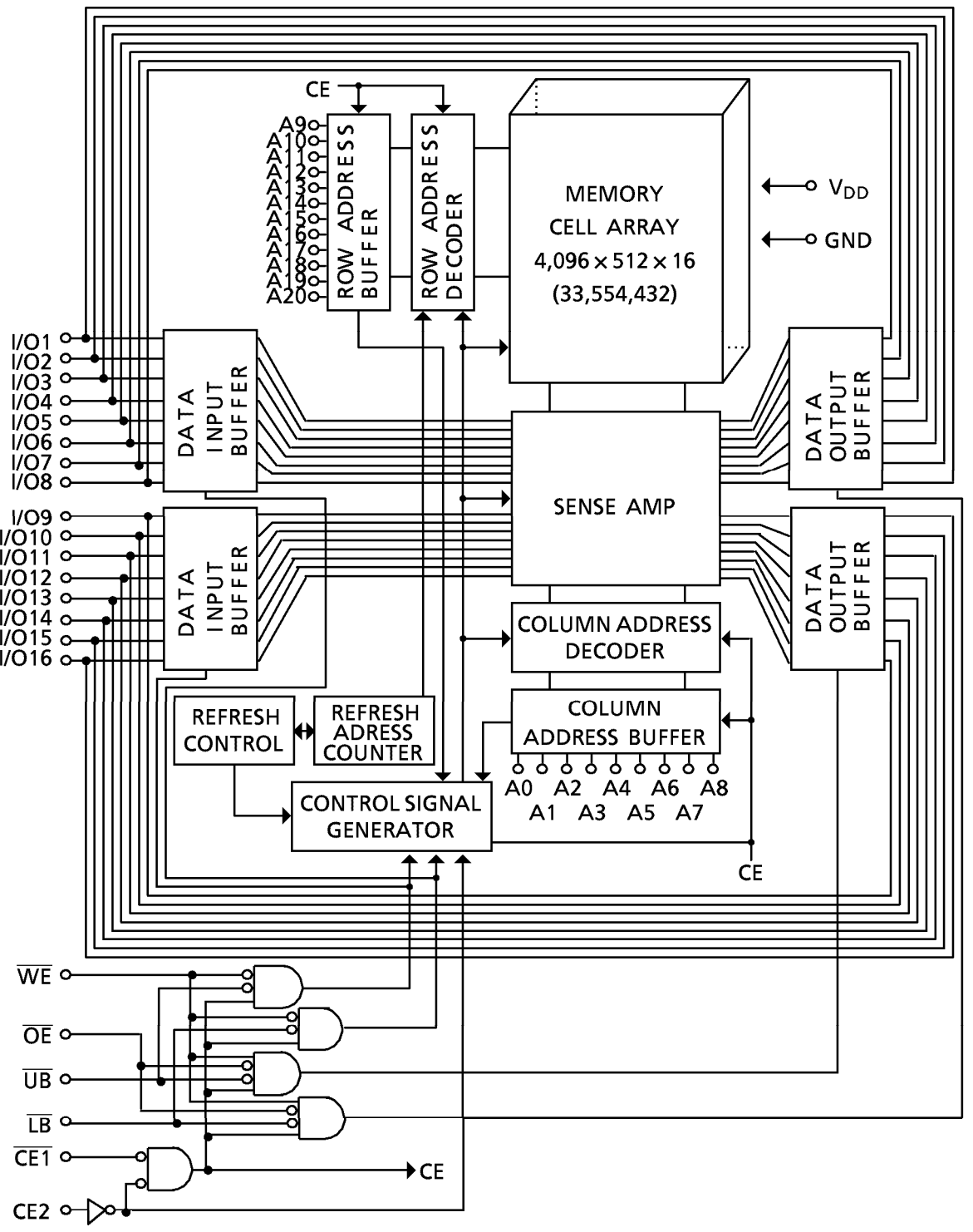
PIN NAMES

A0 to A20	Address Inputs
A0 to A2	Page Address Inputs
I/O1 to I/O16	Data Inputs / Outputs
$\overline{CE1}$	Chip Enable Input
CE2	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
V_{DD}	Power
GND	Ground
NC	No Connection

000707EBA2

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BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Add	I/O1 to I/O8	I/O9 to I/O16	POWER
Read(Word)	L	H	L	H	L	L	×	D_{OUT}	D_{OUT}	I_{DDO}
Read(Lower Byte)	L	H	L	H	L	H	×	D_{OUT}	High-Z	I_{DDO}
Read(Upper Byte)	L	H	L	H	H	L	×	High-Z	D_{OUT}	I_{DDO}
Write(Word)	L	H	×	L	L	L	×	D_{IN}	D_{IN}	I_{DDO}
Write(Lower Byte)	L	H	×	L	L	H	×	D_{IN}	Invalid	I_{DDO}
Write(Upper Byte)	L	H	×	L	H	L	×	Invalid	D_{IN}	I_{DDO}
Outputs Disabled	L	H	H	H	×	×	×	High-Z	High-Z	I_{DDO}
Standby	H	H	×	×	×	×	×	High-Z	High-Z	I_{DDS}
Deep Power-down Standby	H	L	×	×	×	×	×	High-Z	High-Z	I_{DDSD}

L = Low-level Input(V_{IL}), H = High-level Input(V_{IH}), × = V_{IH} or V_{IL}, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS (See Note 1)

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	− 1.0 to 3.6	V
V_{IN}	Input Voltage	− 1.0 to 3.6	V
V_{OUT}	Output Voltage	− 1.0 to 3.6	V
Topr.	Operating Temperature	− 25 to 85	°C
Tstrg.	Storage Temperature	− 55 to 150	°C
Tsolder	Soldering Temperature (10 s)	260	°C
P_D	Power Dissipation	0.6	W
I_{OUT}	Short Circuit Output Current	50	mA

DC RECOMMENDED OPERATING CONDITIONS (Ta = − 25°C to 85°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{DD}	Power Supply Voltage	2.6	2.75	3.1	V
V_{IH}	Input High Voltage	2.0	−	V_{DD} + 0.3*	V
V_{IL}	Input Low Voltage	− 0.3*	−	0.4	V
V_{DH}	Data Retention Supply Voltage	2.6	−	3.1	V

* : V_{IH}(Max) V_{DD} + 1.0 V with 10 ns pulse width
V_{IL}(Min) −1.0 V with 10 ns pulse width

DC CHARACTERISTICS (Ta = − 25°C to 85°C, V_{DD} = 2.6 to 3.1 V) (See Note 3 to 4)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{DD}		−1.0	−	+ 1.0	μA
I_{LO}	Output Leakage Current	Output disable, V_{OUT} = 0 V to V_{DD}		−1.0	−	+ 1.0	μA
V_{OH}	Output High Voltage	I_{OH} = − 0.5 mA		2.0	−	−	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0 mA		−	−	0.4	V
I_{DDO1}	Operating Current	$\overline{CE1}$ = V_{IL} CE2 = V_{IH}, I_{OUT} = 0 mA	t_{RC} = min	−	−	40	mA
I_{DDO2}	Page Access Operating Current	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} Page add. cycling I_{OUT} = 0 mA	t_{PC} = min	−	−	25	mA
I_{DDS}	Standby Current (MOS)	$\overline{CE1}$ = V_{DD} − 0.2 V, CE2 = V_{DD} − 0.2 V		−	−	70	μA
I_{DDSD}	Deep Power-down Standby Current	CE2 = 0.2 V		−	−	5	μA

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is sampled periodically and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = −25°C to 85°C, V_{DD} = 2.6 to 3.1 V) (See Note 5 to 11)

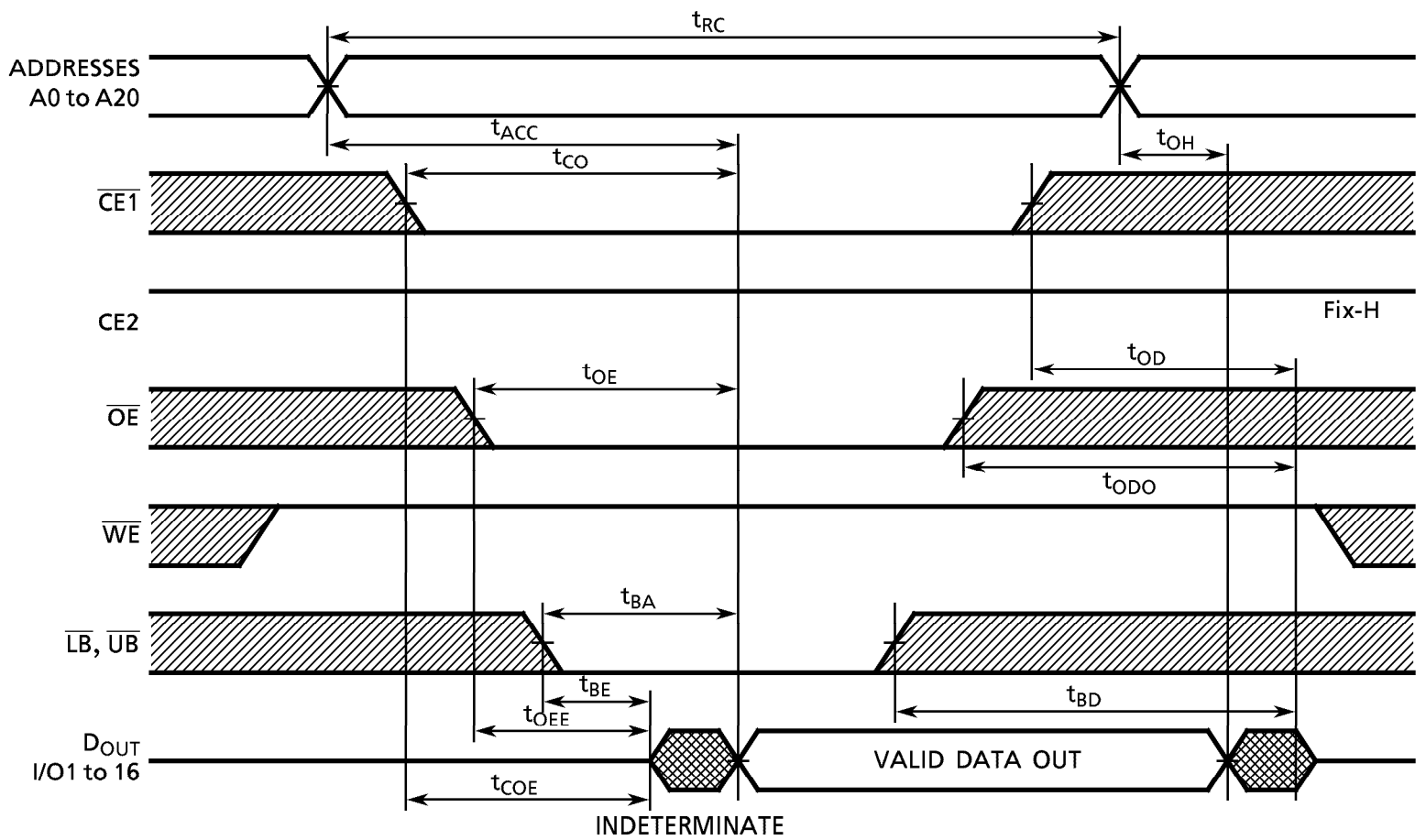
SYMBOL	PARAMETER	TC51WKM516AXGN				UNIT
		65		70		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	65	10000	70	10000	ns
t_{ACC}	Address Access Time	–	65	–	70	ns
t_{CO}	Chip Enable ($\overline{CE1}$) Access Time	–	65	–	70	ns
t_{OE}	Output Enable Access Time	–	25	–	25	ns
t_{BA}	Data Byte Control Access Time	–	25	–	25	ns
t_{COE}	Chip Enable Low to Output Active	10	–	10	–	ns
t_{OEE}	Output Enable Low to Output Active	0	–	0	–	ns
t_{BE}	Data Byte Control Low to Output Active	0	–	0	–	ns
t_{OD}	Chip Enable High to Output High-Z	–	20	–	20	ns
t_{ODO}	Output Enable High to Output High-Z	–	20	–	20	ns
t_{BD}	Data Byte Control High to Output High-Z	–	20	–	20	ns
t_{OH}	Output Data Hold Time	10	–	10	–	ns
t_{PM}	Page Mode Time	65	10000	70	10000	ns
t_{PC}	Page Mode Cycle Time	30	–	30	–	ns
t_{AA}	Page Mode Address Access Time	–	30	–	30	ns
t_{AOH}	Page Mode Output Data Hold Time	10	–	10	–	ns
t_{WC}	Write Cycle Time	65	10000	70	10000	ns
t_{WP}	Write Pulse Width	50	–	50	–	ns
t_{CW}	Chip Enable to End of Write	60	–	60	–	ns
t_{BW}	Data Byte Control to End of Write	60	–	60	–	ns
t_{AS}	Address Setup Time	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	ns
t_{ODW}	$\overline{WE}$ Low to Output High-Z	–	20	–	20	ns
t_{OEW}	$\overline{WE}$ High to Output Active	0	–	0	–	ns
t_{DS}	Data Setup Time	30	–	30	–	ns
t_{DH}	Data Hold Time	0	–	0	–	ns
t_{CS}	CE2 Set-up Time	0	–	0	–	ns
t_{CH}	CE2 Hold Time	300	–	300	–	μs
t_{DPD}	CE2 Pulse Width	10	–	10	–	ms
t_{CHC}	CE2 Hold from $\overline{CE1}$	0	–	0	–	ns
t_{CHP}	CE2 Hold from Power On	30	–	30	–	μs

AC TEST CONDITIONS

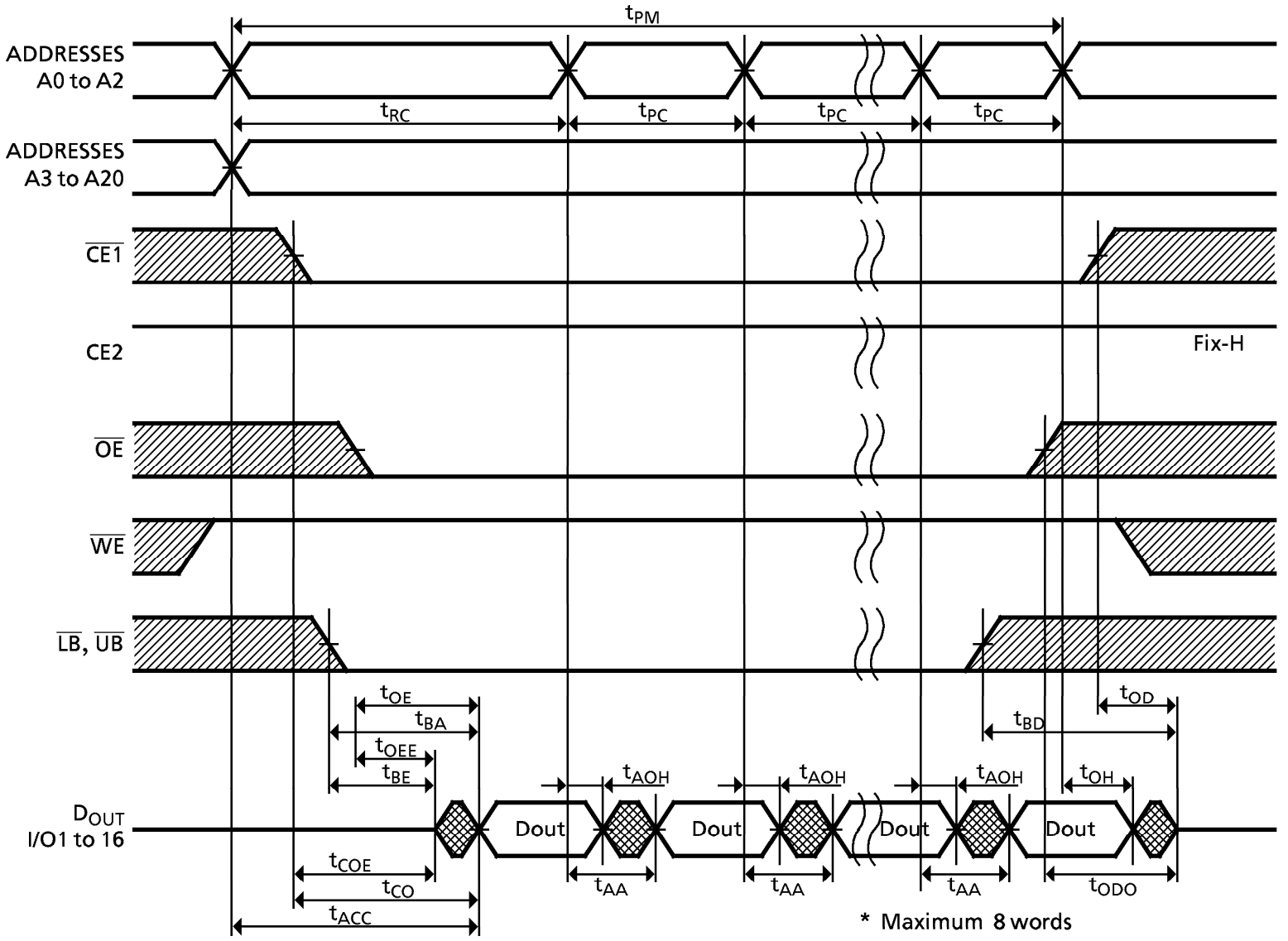
Output load: 30 pF + 1TTL Gate
Input pulse level: V_{DD} − 0.2V, 0.2V
Timing measurements: $V_{DD} \times 0.5$
Reference level: $V_{DD} \times 0.5$
t_R, t_F: 5 ns

TIMING DIAGRAMS

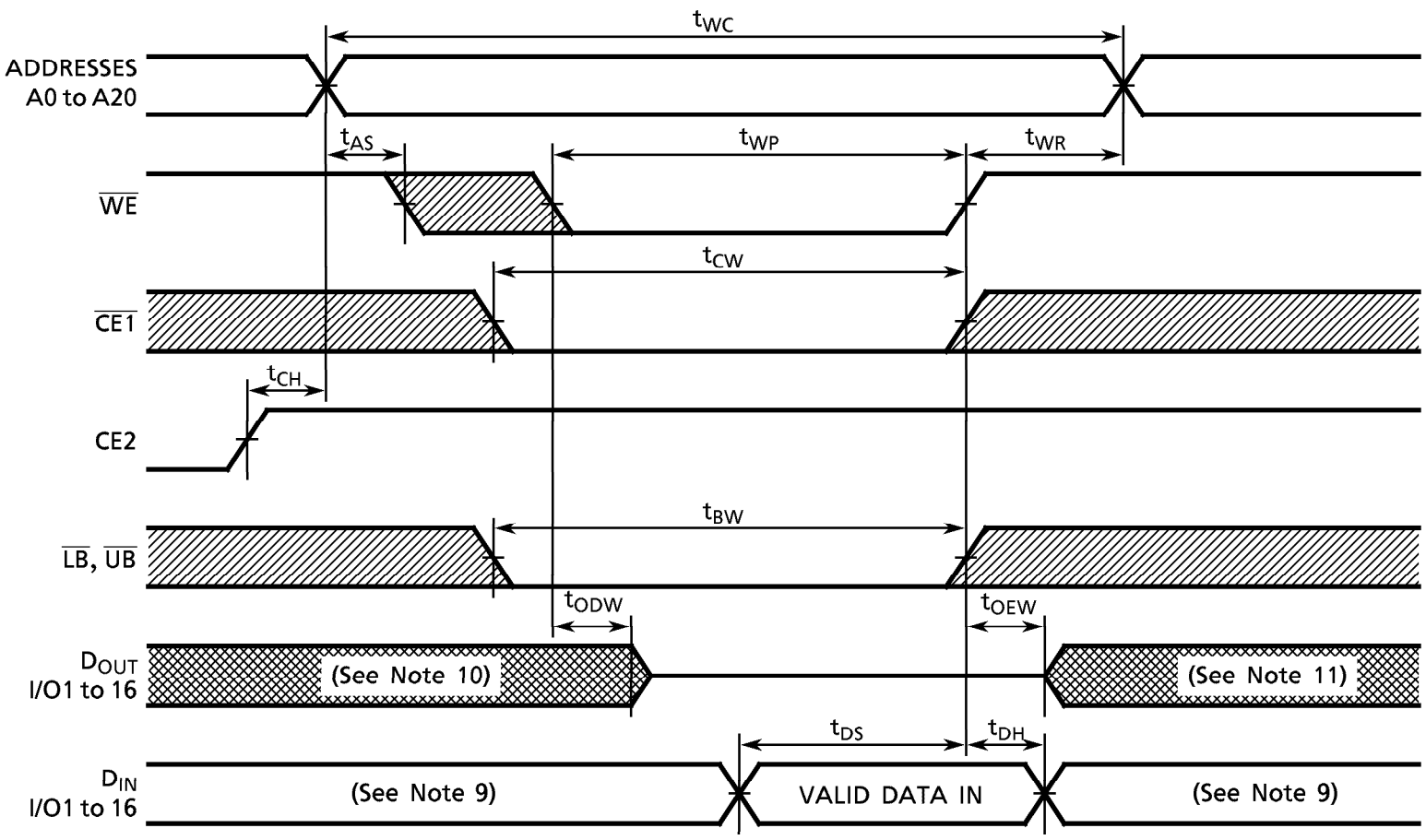
Read Timing



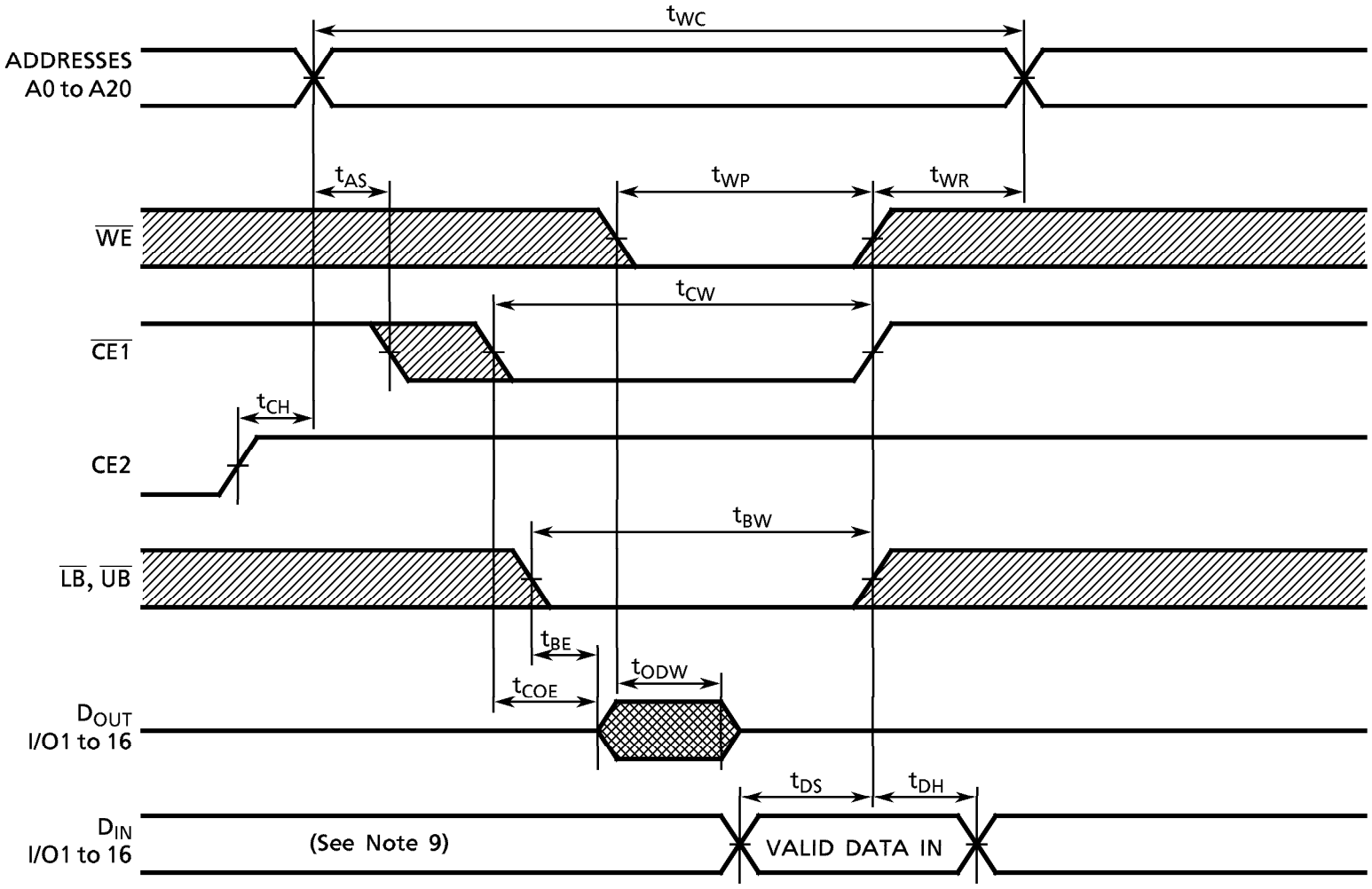
Page Read Timing(8 words access)



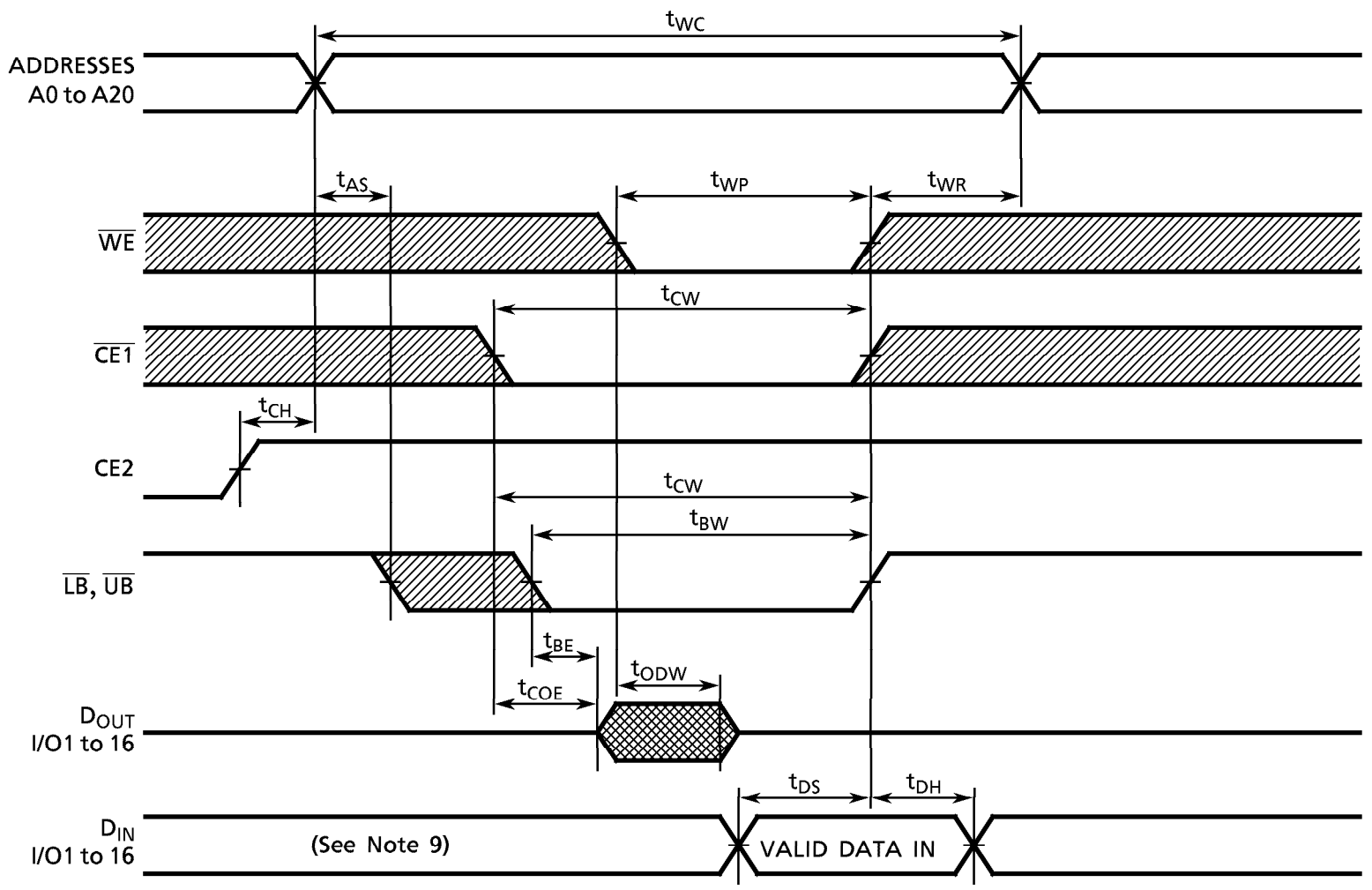
WRITE CYCLE 1 ($\overline{WE}$ CONTROLLED) (See Note 8)



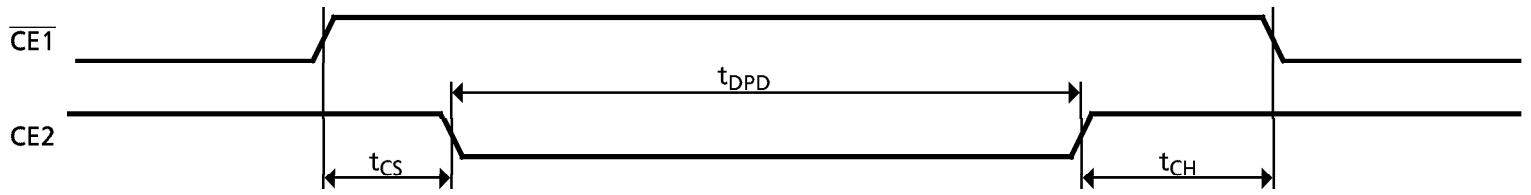
WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 8)



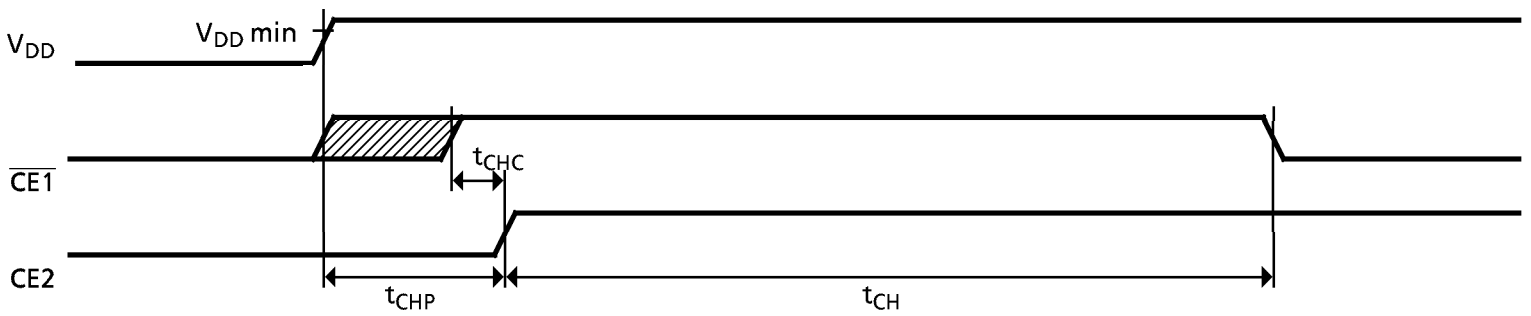
WRITE CYCLE 3 ($\overline{LB}$, $\overline{UB}$ CONTROLLED) (See Note 8)



Deep Power-down Timing



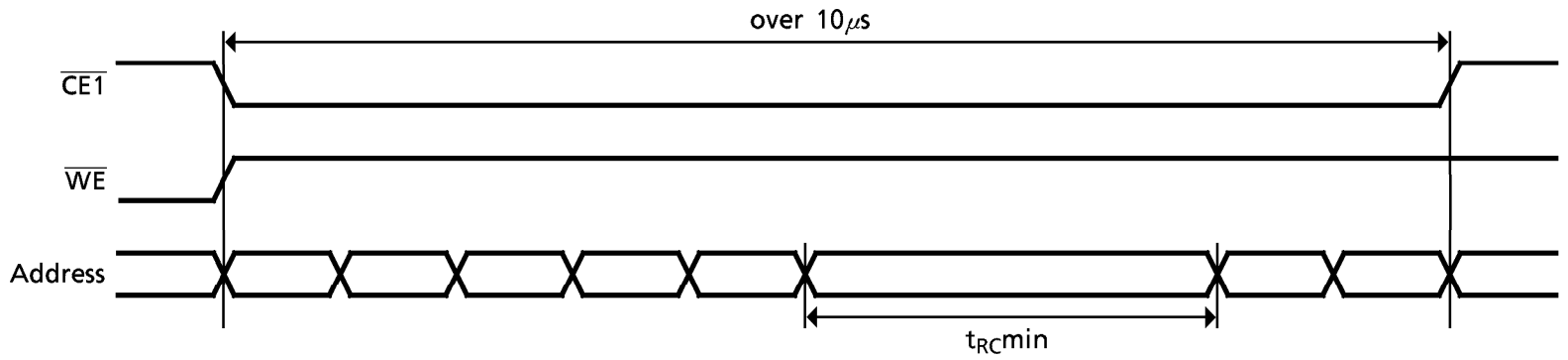
Power-on Timing



Provisions of Address Skew

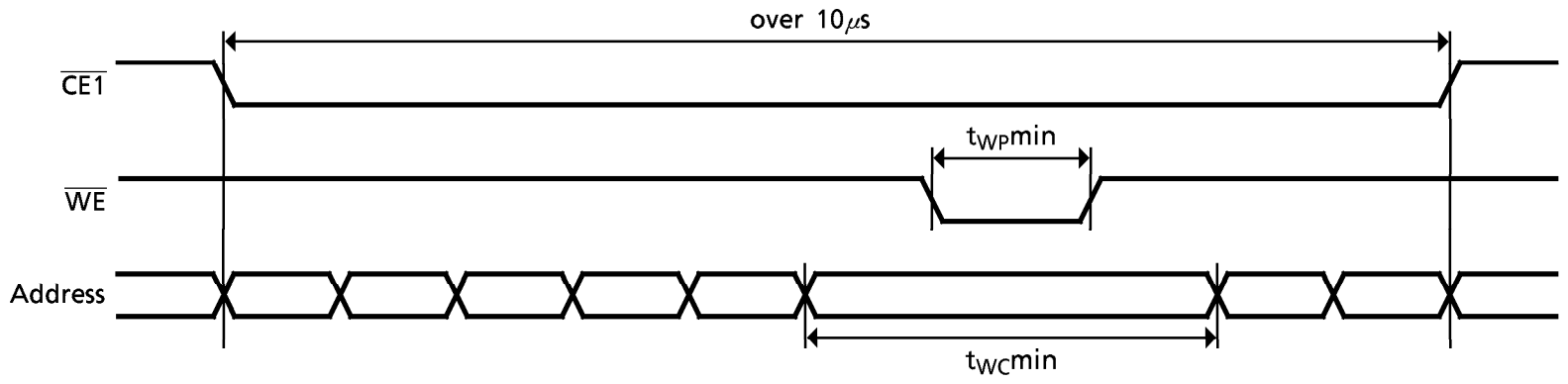
Read

If multiple invalid address cycles shorter than t_{RC}min sustain over 10μs, as least one valid address cycle over tRCmin must be needed during 10μs.



Write

If multiple invalid address cycles shorter than t_{WC}min sustain over 10μs, as least one valid address cycle over t_{WC}min with t_{WP}min must be needed during 10μs.



Notes: (1) Stresses greater than listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

(2) All voltages are reference to GND.

(3) I_{DDO} depends on the cycle time.

(4) I_{DDO} depends on output loading. Specified values are defined with the output open condition.

(5) AC measurements are assumed $t_R, t_F = 5ns$.

(6) Parameters t_{OD}, t_{ODO}, t_{BD} and t_{ODW} define the time at which the output goes the open condition and are not output voltage reference levels.

(7) Data cannot be retained at deep power-down stand-by mode.

(8) If $\overline{OE}$ is high during the write cycle, the outputs will remain at high impedance.

(9) During the output state of I/O signals, input signals of reverse polarity must not be applied.

(10) If $\overline{CE1}$ or $\overline{LB}/\overline{UB}$ goes LOW coincident with or after $\overline{WE}$ goes LOW, the outputs will remain at high impedance.

(11) If $\overline{CE1}$ or $\overline{LB}/\overline{UB}$ goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the outputs will remain at high impedance.

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