M-Systems
Flash Disk Pioneers

DiskOnChip

DiskOnChip-Based MCP

Including DiskOnChip G3 and Mobile RAM

Data Sheet, August 2004

Highlights

DiskOnChip-based MCP (Multi-Chip Package) is a complete memory solution. Efficiently packed in a small Fine-Pitch Ball Grid Array (FBGA) package, it is ideal for data and code storage inside 2.5G and 3G mobile handsets and Personal Digital Assistants (PDAs). DiskOnChip-based MCP consists of:

- M-Systems' DiskOnChip G3
- Elpida's Low Power SDRAM

Using such an MCP configuration reduces overall memory costs, saves PCB real estate and maintains efficient power consumption levels. It may also have far-reaching implications on the mobile handset memory architecture, supporting a NOR-less memory system by providing boot functionality at a much less expensive cost than NOR.

General Features

- Small 9x12x1.4 mm 107-ball FBGA package
- 64MB (512Mb) DiskOnChip G3
- 16MB (128Mb) Low Power SDRAM
- High performance 16-bit interface to all devices
- Deep Power-Down mode for low power consumption
- Operating voltage
  DiskOnChip: 2.5V to 3.6V
  Low Power SDRAM: 2.8V ± 0.2V
- Operating temperature: -25°C to +85°C



DiskOnChip G3

Highlights

DiskOnChip G3 is one of the industry's most efficient storage solutions, using Toshiba's 0.13 micron Multi-Level Cell (MLC) NAND flash technology and x2 technology from M-Systems. MLC NAND flash technology provides the smallest die size by storing 2 bits of information in a single memory cell. x2 technology enables MLC NAND to achieve highly reliable, high-performance data and code storage with a specially designed error detection and correction mechanism, optimized file management, and proprietary algorithms for enhanced performance.

Further cost benefits derive from the cost-effective architecture of DiskOnChip G3, which includes a boot block that can replace expensive NOR flash, and incorporates both the flash array and an embedded thin controller in a single die.

DiskOnChip G3 provides:

- Flash disk for both code and data storage
- Low voltage: 1.8V or 3.3 I/O (auto-detect), 3V Core
- Hardware protection and security-enabling features

- Enhanced Programmable Boot Block enabling eXecute In Place (XIP) functionality using 16-bit interface
- Enhanced performance by implementation of:
  - Multi-plane operation
  - DMA support
  - MultiBurst operation
  - Turbo operation
- Unrivaled data integrity with a robust Error Detection Code/Error Correction Code (EDC/ECC) tailored for MLC NAND flash technology
- Maximized flash endurance with TrueFFS® 6.x
- Support for major mobile operating systems (OSs), including Symbian OS, Pocket PC 2002/3, Smartphone 2002/3, Palm OS, Nucleus, Linux, Windows CE, and more.
- Compatible with major mobile CPUs, including TI OMAP, XScale, Motorola DragonBall MX1 and Qualcomm MSMxxxx.

Low Power SDRAM

- Organization: 2M × 16 bits × 4 banks
- Refresh
  - Auto-refresh
  - Self-refresh
  - Programmable partial self-refresh
  - Programmable temperature-compensated self-refresh (optional)
- Power dissipation
  - Operating: 65 mA maximum
  - Refresh: 155 mA maximum
  - Self refresh: 350 µA maximum
- 4,096 refresh cycles/64 ms
- Programmable driver strength
- Deep power down mode
- Fully synchronous DRAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Option to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1
- Byte control by LDQM and UDQM
- Wrap sequence: Sequential/ Interleave
- /CAS latency (CL): 2, 3
- Automatic and controlled precharge
- Burst termination by Burst stop command and Precharge command

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1. PRODUCT OVERVIEW

1.1 Ballout

M-Systems' DiskOnChip-based MCP is packaged in a 107-ball FBGA 9x12 mm package. See Figure 1 for the ball assignments.

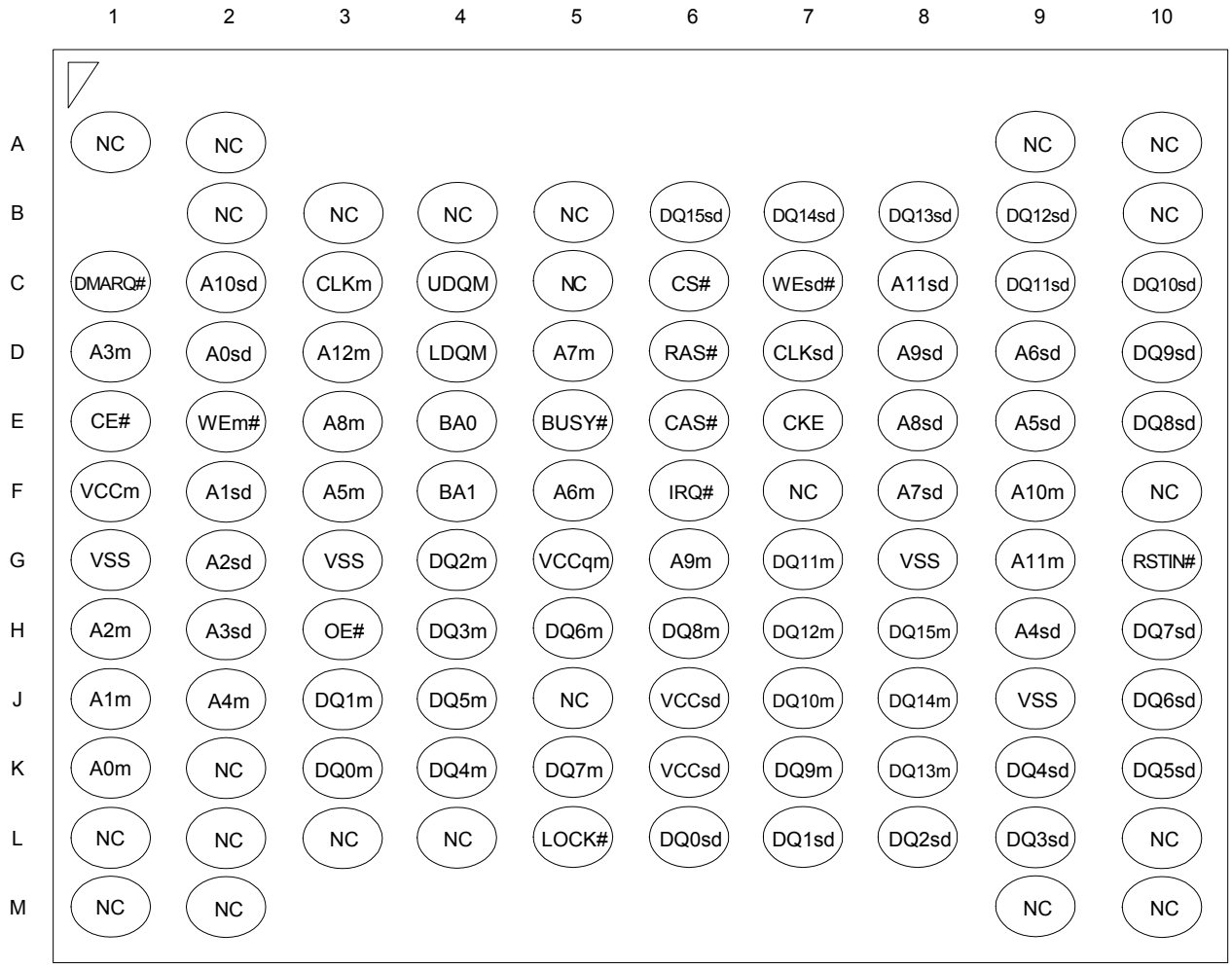


Figure 1: DiskOnChip-Based MCP Ball Diagram – Top View

1.2 Signal Descriptions

Table 1 contains signal descriptions based on the ball diagram in Figure 1.

Table 1: DiskOnChip-Based MCP Signal Descriptions

Signal	Description
A0sd to A11sd	Address inputs for Low Power SDRAM
DQ0sd to DQ15sd	Data inputs/outputs for Low Power SDRAM
CLKsd	Clock for Low Power SDRAM
CKE	Clock Enable for Low Power SDRAM
CS#	Chip Select for Low Power SDRAM
RAS#	Row Address Strobe for Low Power SDRAM
CAS#	Column Address Strobe for Low Power SDRAM
WEsd#	Write Enable for Low Power SDRAM
UDQM	Upper Data Mask enable for Low Power SDRAM
LDQM	Lower Data Mask enable for Low Power SDRAM
A0m to A12m	Address inputs for DiskOnChip G3
DQ0m to DQ15m	Data inputs / outputs for DiskOnChip G3
CE#	Chip Enable for DiskOnChip G3
OE#	Output Enable for DiskOnChip G3
WEm#	Write Enable for DiskOnChip G3
CLKm	Clock for DiskOnChip G3
RSTIN#	Reset Input for DiskOnChip G3
LOCK#	Hardware data protect input for DiskOnChip G3
IRQ#	Interrupt Request, required for DiskOnChip G3
BUSY#	Busy output for DiskOnChip G3
DMARQ#	DMA Request for DiskOnChip G3
VCCsd	Main power supply for Low Power SDRAM
VCCqm	I/O power supply for DiskOnChip G3
VCCm	Power supply for DiskOnChip G3
VSS	Ground
NC	Not connected

1.3 Internal Connections

All the components in DiskOnChip-based MCP behave like separate devices. Each component has a separate ball for its Chip Enable (CE#) signal, as well as a separate ball for power supply. Table 2 shows the internal connections.

Note: Some signals described in the individual data sheets have been internally connected to VSS or VCC. Other signals are shared and therefore have been renamed.

Table 2: Internal Connections

Internal Connection		16MB (128Mb) Low Power SDRAM	64MB (512Mbit) DiskOnChip G3
FBGA Location	Signal		
A1	NC	--	--
A2	NC	--	--
A9	NC	--	--
A10	NC	--	--
B2	NC	--	--
B3	NC	--	--
B4	NC	--	--
B5	NC	--	--
B6	DQ15sd	DQ15	--
B7	DQ14sd	DQ14	--
B8	DQ13sd	DQ13	--
B9	DQ12sd	DQ12	--
B10	NC	--	--
C1	DMARQ#	--	DMARQ#
C2	A10sd	A10	--
C3	CLKm	--	CLK
C4	UDQM	UDQM	--
C5	NC	--	--
C6	CS#	CS#	--
C7	WEsd#	WE#	--
C8	A11sd	A11	--
C9	DQ11sd	DQ11	--
C10	DQ10sd	DQ10	--
D1	A3m	--	A3
D2	A0sd	A0	--
D3	A12m	--	A12
D4	LDQM	LDQM	--

Internal Connection		16MB (128Mb) Low Power SDRAM	64MB (512Mbit) DiskOnChip G3
FBGA Location	Signal		
D5	A7m	--	A7
D6	RAS#	RAS#	--
D7	CLKsd	CLK	--
D8	A9sd	A9	--
D9	A6sd	A6	--
D10	DQ9sd	DQ9	--
E1	CE#	--	CE#
E2	WEm#	--	WE#
E3	A8m	--	A8
E4	BA0	BA0	--
E5	BUSY#	--	BUSY#
E6	CAS#	CAS#	--
E7	CKE	CKE	--
E8	A8sd	A8	--
E9	A5sd	A5	--
E10	DQ8sd	DQ8	--
F1	VCCm	--	VCC
F2	A1sd	A1	--
F3	A5m	--	A5
F4	BA1	BA1	--
F5	A6m	--	A6
F6	IRQ#	--	IRQ#
F7	A12sd	A12	--
F8	A7sd	A7	--
F9	A10m	--	A10m
F10	NC	--	--
G1	VSS	VSS, VSSQ	VSS
G2	A2sd	A2	--
G3	VSS	VSS, VSSQ	VSS
G4	DQ2m	--	D2
G5	VCCqm	--	VCCQ
G6	A9m	--	A9
G7	DQ11m	--	D11
G8	VSS	VSS, VSSQ	VSS
G9	A11m	--	A11

Internal Connection		16MB (128Mb) Low Power SDRAM	64MB (512Mbit) DiskOnChip G3
FBGA Location	Signal		
G10	RSTIN#	--	RSTIN#
H1	A2m	--	A2
H2	A3sd	A3	--
H3	OE#	--	OE#
H4	DQ3m	--	D3
H5	DQ6m	--	D6
H6	DQ8m	--	D8
H7	DQ12m	--	D12
H8	DQ15m	--	D15
H9	A4sd	A4	--
H10	DQ7sd	DQ7	--
J1	A1m	--	A1
J2	A4m	--	A4
J3	DQ1m	--	D1
J4	DQ5m	--	D5
J5	NC	--	--
J6	VCCsd	VDD	--
J7	DQ10m	--	D10
J8	DQ14m	--	D14
J9	VSS	VSS, VSSQ	VSS
J10	DQ6sd	DQ6	--
K1	A0m	--	A0
K2	NC	--	--
K3	DQ0m	--	D0
K4	DQ4m	--	D4
K5	DQ7m	--	D7
K6	VCCsd	VDDQ	--
K7	DQ9m	--	D9
K8	DQ13m	--	D13
K9	DQ4sd	DQ4	--
K10	DQ5sd	DQ5	--
L1	NC	--	--
L2	NC	--	--
L3	NC	--	--
L4	NC	--	--

Internal Connection		16MB (128Mb) Low Power SDRAM	64MB (512Mbit) DiskOnChip G3
FBGA Location	Signal		
L5	LOCK#	--	LOCK#
L6	DQ0sd	DQ0	--
L7	DQ1sd	DQ1	--
L8	DQ2sd	DQ2	--
L9	DQ3sd	DQ3	--
L10	NC	--	--
M1	NC	--	--
M2	NC	--	--
M9	NC	--	--
M10	NC	--	--

1.4 Block Diagram

Figure 2 shows a block diagram of the components that comprise DiskOnChip-Based MCP, including their special and interconnected signals.

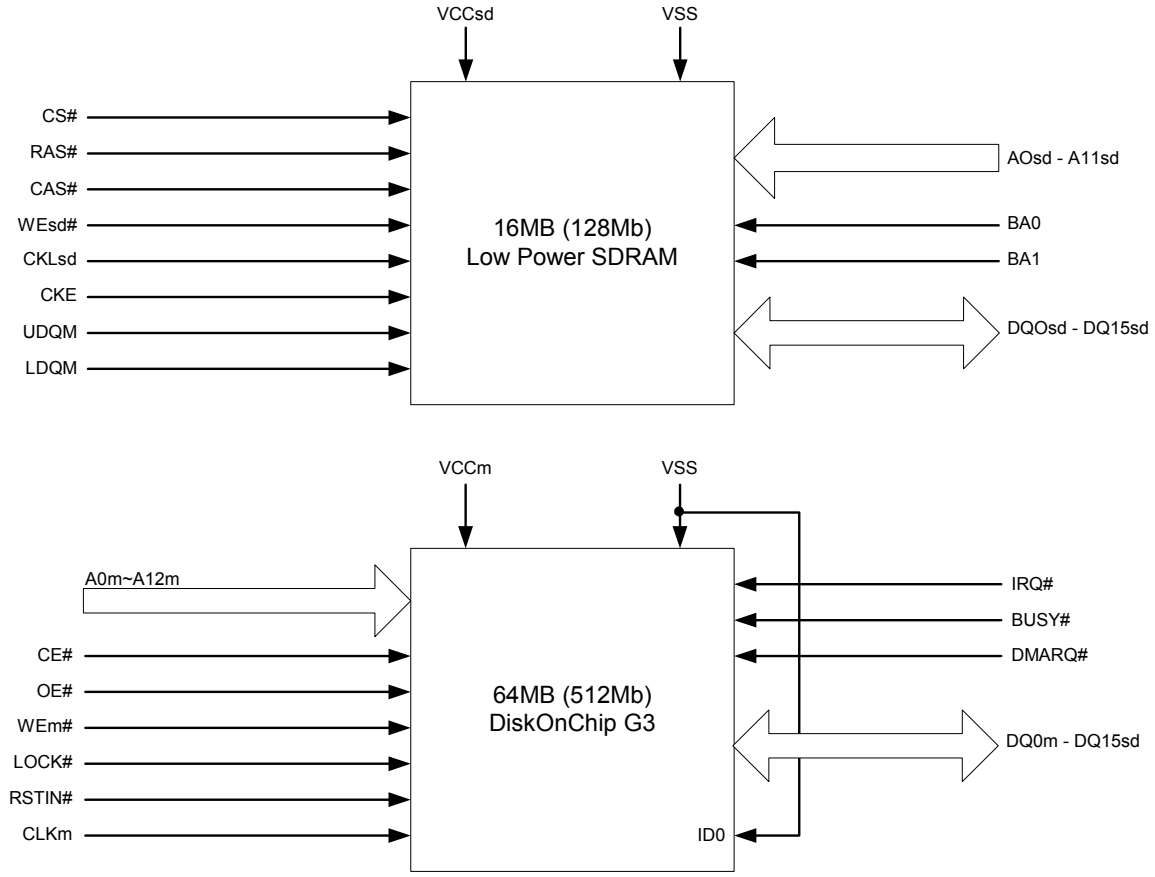


Figure 2: DiskOnChip-Based MCP Block Diagram

2. SPECIFICATIONS

2.1 Electrical

2.1.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Symbol	Parameter		Range	Unit
VCCsd	VCCsd Supply Voltage		-0.5 ~3.5	V
VCCm	VCCm Supply Voltage		-0.6 ~4.6	V
VCCqm	VCCm IO Supply Voltage		-0.6 ~4.6	V
VIN	Input Voltage	LPSDRAM	-0.5 ~3.6	V
		DiskOnChip G3	-0.6 ~4.6	V
VDQ	Input/Output Voltage	LPSDRAM	-0.5 ~VCCQ – 0.5 (≤ 3.6)	V
		DiskOnChip G3	-0.6 ~4.6	V
Topr	Operating Temperature		-25 ~85	°C
PD	Power Dissipation		0.6	W
Tsolder	Soldering Temperature (10 s)		240	°C
IOSHORT	Output Short Circuit Current [1]		50	mA
Tstg	Storage Temperature		-55 ~125	°C

1. Output shorted for no more than one second. No more than one output shorted at a time.

2.1.2 DC Operating Conditions

Table 4: Recommended DC Operating Conditions (Ta = -25 ~85°C, VCCqm=1.65V-2.0V)

Symbol	Parameter		Min.	Typ.	Max.	Unit
VCCsd	VCCsd Supply Voltage		2.6	2.8	3.0	V
VCCm	VCCm Supply Voltage		2.5	3.0	3.6	
VCCqm	VCCm IO Supply Voltage		1.65	1.8	2.0	
VIH	Input High-Level Voltage	LPSDRAM	0.8 x VCCsd	--	VCCsd + 0.3[1]	
		DiskOnChip G3	VCCqm–0.4	--		
VIL	Input Low-Level Voltage	LPSDRAM	0.3[2]	--	0.3	
		DiskOnChip G3	--	--	0.4	

1. VCCsd = 1.5V for pulse width ≤ 5 ns.

2. –1.5V for pulse width ≤ 5 ns.

Table 5: Recommended DC Operating Conditions (Ta = -25 ~85°C, VCCqm=2.5V-3.6V)

Symbol	Parameter		Min.	Typ.	Max.	Unit
VCCsd	VCCsd Supply Voltage		2.6	2.8	3.0	V
VCCm	VCCm Supply Voltage		2.5	3.0	3.6	
VCCqm	VCCm IO Supply Voltage		2.5	3.0	3.6	
VIH	Input High-Level Voltage	LPSDRAM	0.8 x VCCsd	--	VCCsd + 0.3[1]	
		DiskOnChip G3	2.1	--	--	
VIL	Input Low-Level Voltage	LPSDRAM	0.3[2]	--	0.3	
		DiskOnChip G3	--	--	0.7	

1. VCCsd = 1.5V for pulse width ≤ 5 ns.

2. –1.5V for pulse width ≤ 5 ns.

2.1.3 Capacitance

Table 6: Capacitance (Ta = 25°C, f = 1 MHz)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = GND	--	--	TBD	pF
COUT	Output Capacitance	VOUT = GND	--	--	TBD	pF

Note: These parameters are sampled periodically and are not tested for every device.

2.1.4 DC Characteristics of Low Power SDRAM

Table 7: DC Characteristics (Low Power SDRAM)

Symbol	Parameter	Condition		Min.	Max.	Unit
ICC1sd	Operating current [1]	Burst length=1, tRC min, IOUT=0 mA, one bank active	CAS# latency=2	--	65	mA
			CAS# latency=3	--	65	mA
ICC2Psd	Standby current in Power Down mode	CKE = VIL, tCK = 15 ns		--	1	mA
ICC2PSsd	Standby current in Power Down mode (input signal stable)	CKE = VIL, tCK = ∞		--	0.8	mA
ICC2Nsd	Standby current in Non-Power Down mode	CKE = VIH, tCK = 15 ns, CS# -= VIH Input signals are changed one time during 30 ns		--	5.5	mA
ICC2NSsd	Standby current in Non-Power Down mode (input signal stable)	CKE = VIH, tCK = ∞, input signals are stable		--	2.5	mA
ICC3Psd	Active standby current in Power Down mode	CKE = VIH, tCK = 15 ns, CS# -= VIH Input signals are changed one time during 30 ns		--	1.5	mA
ICC3PSsd	Active standby current in Power Down mode (input signal stable)	CKE = VIH, tCK = ∞		--	1	mA
ICC3Psd	Active standby current in Non-Power Down mode	CKE = VIH, tCK = 15 ns, CS# = VIH Input signals are changed one time during 30 ns		--	17	mA
IC3PSsd	Active standby current in Non-Power Down mode (input	CKE = VIH, tCK = ∞, input signals are stable		--	12	mA

Symbol	Parameter	Condition		Min.	Max.	Unit
	signal stable)					
ICC4sd	Burst operating current [2]	Burst length=1, tCK min, IOUT-0 mA, all banks active	CAS# latency=2	--	60	mA
			CAS# latency=3	--	80	mA
ICC5sd	Refresh current [3]	tRC min	CAS# latency=2	--	155	mA
			CAS# latency=3	--	155	mA
ICC6sd	Self-refresh current	TCSR="00" (Ts[4]≤70°C)	PASR="000" (Full)	--	0.35	mA
			PASR-"001" (2BK)	--	0.25	mA
			PASR="010" (1BK)	--	0.185	mA
		TCSR="01" (Ts[4]≤45°C)	PASR="000" (Full)	--	0.20	mA
			PASR-"001" (2BK)	--	0.165	mA
			PASR="010" (1BK)	--	0.14	mA
		TCSR="11" (Ts[4]≤85°C) CKE ≤ 0.2V	PASR="000" (Full)	--	0.35	mA
			PASR-"001" (2BK)	--	0.25	mA
			PASR="010" (1BK)	--	0.185	mA
ICC3PSsd	Standby current in Deep Power Down mode	CKE ≤ 0.2V		--	10	µA
IILsd	Input leakage current	VIN = 0V ~VCCsd		--	±10	µA
ILOsd	Output leakage current	VOUT = 0v ~VCCsd, DQ disable		--	±10	µA
IOHsd	Output high current	VOH = VCCsd –0.2V		-0.1	--	mA
IOLsd	Output low current	VOL = 0.2V		0.1	--	mA

1. ICC1sd depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, ICC1sd is measured condition that addresses are changed only one time during tCK (min.).

2. ICC4sd depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, ICC4sd is measured condition that addresses are changed only one time during tCK (min.).

3. ICC5sd is measured on condition that addresses are changed only one time during tCK (min.).

4. Ts is the surface temperature.

2.2 DC Characteristics of DiskOnChip G3

Table 8: DC Characteristics (DiskOnChip G3)

Symbol	Parameter	Condition	Min.	Max.	Unit
ICCOm	Active supply current	Cycle time = 100 ns	--	25	mA
ICCSm	Standby supply current	Deep Power-Down mode	--	20	µA
IILm	Input leakage current	VIN = 0V ~VCCsd	--	±20	µA
ILOm	Output leakage current	VOUT = 0V ~VCCsd, DQ disable	--	±20	µA
IOHm	Output high current	VOH = VCCm –0.3V	-4	--	mA
IOLm	Output low current	VOL = 0.4V ; VCCqm = 3.0V-3.6V	8	--	mA
		VOL = 0.4V ; VCCqm = 2.5V-3.0V	5	--	mA

2.3 Environmental

Temperature Range -25°C to +85°C

2.4 Mechanical

Dimensions 9.0 ± 0.10 x 12.0 ± 0.10 mm

Height 1.30 ± 0.10 mm

Ball Count 107 balls

Ball Pitch 0.80 mm

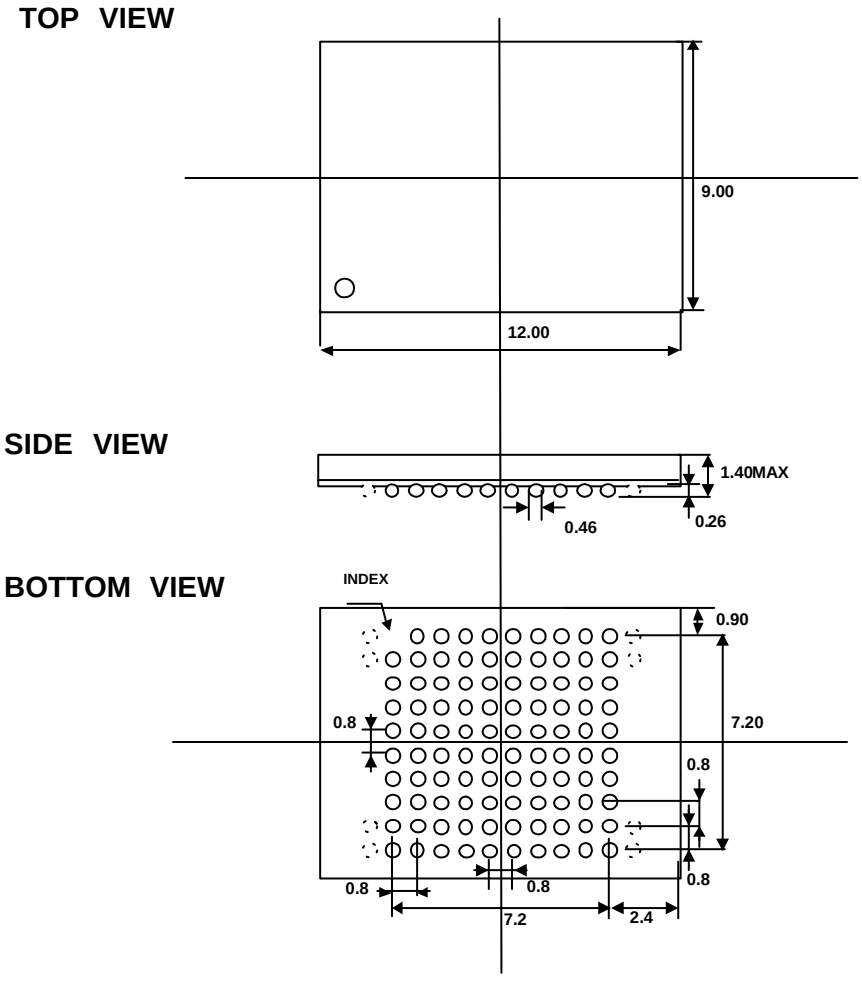


Figure 3: DiskOnChip-Based MCP Dimensions (in mm)

3. ORDERING INFORMATION

MS08-D9SD7-B3

MS08: M-Systems' DiskOnChip-Based MCP

D9: DiskOnChip G3 64MB (512Mbit) (2^9 Mbit)

SD7: Low Power SDRAM 16MB (128Mbit) (2^7 Mbit)

B3: 107-ball FBGA; 9x12x1.4 mm

4. MARKINGS

First row: Product name – DiskOnChip MCP

Second row: Ordering information

Third row: Production information:

yyww - Year and week

zzz - Product status: Engineering samples "-ES", Customer samples "-CS" or FAB marking

$$$$$$$$ - Internal marking



Figure 4: DiskOnChip-Based MCP Product Marking

A. DISKONCHIP G3 64MB (512MBIT) DATA SHEET

M-Systems
Flash Disk Pioneers

DiskOnChip

DiskOnChip G3 64MB (512Mb)

Flash Disk with MLC NAND and M-Systems' x2 Technology

Data Sheet, March 2004

Highlights

DiskOnChip G3 is one of the industry's most efficient storage solutions, using Toshiba's 0.13 µm Multi-Level Cell (MLC) NAND flash technology and x2 technology from M-Systems. MLC NAND flash technology provides the smallest die size by storing 2 bits of information in a single memory cell. x2 technology enables MLC NAND to achieve highly reliable, high-performance data and code storage with a specially designed error detection and correction mechanism, optimized file management, and proprietary algorithms for enhanced performance.

Further cost benefits derive from the cost-effective architecture of DiskOnChip G3, which includes a boot block that can replace expensive NOR flash, and incorporates both the flash array and an embedded thin controller in a single die.

DiskOnChip G3 provides:

- Flash disk for both code and data storage
- Low voltage: 1.8V or 3.3 I/O (auto-detect), 3V Core
- Hardware protection and security-enabling features
- High capacity: single die - 512Mb (64MB)
- Device cascade capacity: up to 2Gb (256MB)
- Enhanced Programmable Boot Block enabling eXecute In Place (XIP) functionality using 16-bit interface
- Small form factors:

  512Mb (64MB) capacity (single die):
  - 85-ball FBGA 7x10 mm package
- Enhanced performance by implementation of:
  - Multi-plane operation
  - DMA support
  - MultiBurst operation
  - Turbo operation
- Unrivaled data integrity with a robust Error Detection Code/Error Correction Code (EDC/ECC) tailored for MLC NAND flash technology
- Maximized flash endurance with TrueFFS® 6.1 (and higher)
- Support for major operating systems (OSs), including Symbian OS, Pocket PC 2002/3, Smartphone 2002/3, Palm OS, Nucleus, Linux, Windows CE,ThreadX, VxWorks, and more.
- Compatible with major CPUs, including TI OMAP, XScale, Motorola MX, and Qualcomm MSMxxxx.

Note: This data sheet is correct for Mobile DiskOnChip G3 and mDiskOnChip G3.

Performance

- MultiBurst read: 80 MB/sec
- Erase: 30 MB/sec
- Sustained read: 5 MB/sec
- Sustained write: 1.1 MB/sec
- Cycle Time
  - MultiBurst: Up to 25 nsec
- Access time:
  - Normal: 55 nsec
  - Turbo: 33 nsec

Protection & Security-Enabling Features

- 16-byte Unique Identification (UID) number
- 6KByte user-controlled One Time Programmable (OTP) area
- Two configurable hardware-protected partitions for data and code:
  - Read-only mode
  - Write-only mode
  - One-Time Write mode (ROM-like) partition
  - Protection key and LOCK# signal
  - Sticky Lock (SLOCK) to lock boot partition
  - Protected Bad Block Table

Reliability and Data Integrity

- Hardware- and software-driven, on-the-fly EDC and ECC algorithms
- 4-bit Error Detection Code/Error Correction Code (EDC/ECC), based on a patented combination of BCH and Hamming code algorithms, tailored for MLC NAND flash technology
- Guaranteed data integrity after power failure
- Transparent bad-block management
- Dynamic and static wear-leveling

Boot Capability

- Programmable Boot Block with XIP capability to replace boot NOR
  - 2KB for 512Mb (64MB) devices
- Download Engine (DE) for automatic download of boot code from Programmable Boot Block
- Boot options:
  - CPU initialization
  - Platform initialization
  - OS boot
- Asynchronous Boot mode to boot from ARM-based CPUs, e.g. XScale, TI OMAP, Motorola MX without the need for external glue logic
- Exceptional boot performance with MultiBurst operation and DMA support enhanced by external clock

Hardware Compatibility

- Configurable interface: simple NOR-like
- CPU compatibility, including:
  - ARM-based CPUs
  - Texas Instruments OMAP
  - Intel StrongARM/XScale
  - Motorola MX family
  - Emblaze ER4525
  - Renesas SH mobile
  - Qualcomm MSMxxxx
  - AMD Alchemy
  - Motorola PowerPC™ MPC8xx
  - Philips PR31700
  - Hitachi SuperH™ SH-x
  - NEC VR Series
- Supports 8-, 16- and 32-bit architectures

TrueFFS® Software

- Full hard-disk read/write emulation for transparent file system management
- Patented TrueFFS
  - Flash file system management
  - Automatic block management
  - Data management to maximize the limit of typical flash life expectancy
  - Dynamic virtual mapping
- Dynamic and static wear-leveling
- Programming, duplicating, testing and debugging tools available in source code

Operating Environment

- Wide OS support, including:
  - Symbian OS (EPOC)
  - Pocket PC 2002/3
  - Smartphone 2002/3
  - Palm OS
  - Nucleus
  - Windows CE
  - Linux
  - ThreadX
  - OSE
  - VxWorks
- TrueFFS Software Development Kit (SDK) for quick and easy support for proprietary OSs, or OS-less environment
- TrueFFS Boot Software Development Kit (BDK)

Power Requirements

- Operating voltage
  - Core: 2.5V to 3.6V
  - I/O: 1.65 to 2.0V; or 2.5V to 3.6V (auto-detect)
- Current Consumption
  - Active mode:
    Read: 4.2 mA
    Program/erase: 7.2 mA
  - Deep Power-Down mode:
    10 µA (512Mb/64MB)

Capacity and Packaging

- 64MB (512Mb) capacity (single die):
  - 85-ball FBGA package:
    7x10x1.2 mm (width x length x height)

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1. INTRODUCTION

This data sheet includes the following sections:

Section 1: Overview of data sheet contents

Section 2: Product overview, including a brief product description, ball diagrams and signal descriptions

Section 3: Theory of operation for the major building blocks

Section 4: Major features and benefits of x2 technology

Section 5: Detailed description of hardware protection and security-enabling features

Section 6: Detailed description of modes of operation and TrueFFS technology, including power failure management and 8KByte memory window

Section 7: DiskOnChip G3 register descriptions

Section 8: Overview of how to boot from DiskOnChip G3

Section 9: Hardware and software design considerations

Section 10: Environmental, electrical, timing and product specifications

Section 11: Information on ordering DiskOnChip G3

For additional information on M-Systems' flash disk products, please contact one of the offices listed on the back page.

2. PRODUCT OVERVIEW

2.1 Product Description

DiskOnChip G3 is the latest addition to M-Systems' DiskOnChip product family. DiskOnChip G3, packed in the smallest available FBGA package with 64MB (512Mb) capacity, is a single-die device with an embedded thin flash controller and flash memory. It uses Toshiba's cutting-edge, 0.13 µ NAND-based Multi-Level Cell (MLC) flash technology, enhanced by M-Systems' proprietary x2 technology.

MLC NAND technology enables two bits of data to be stored on a single cell, cutting in half the physical die size. M-Systems' proprietary x2 technology overcomes MLC-related error patterns and slow transfer rates by using a robust error detection and correction (EDC/ECC) mechanism. Furthermore, it provides performance enhancement with multi-plane operation, DMA support, turbo operation and MultiBurst operation. The combination of MLC and x2 technology results in a low-cost, minimal-sized flash disk that achieves unsurpassed reliability levels and enhanced performance.

This breakthrough in performance, size and cost makes DiskOnChip G3 the ideal solution for product manufacturers who require high-capacity, small size, high-performance, and above all, high-reliability storage to enable applications such as Digital TVs (DTVs), rugged handheld terminals, Digital Still Cameras (DSCs), Mobile Point of Sale (POS), telecom equipment, multimedia phones, camera and Video on Demand (VOD) phones, enhanced Multimedia Messaging Service (MMS), gaming, video and Personal Information Management (PIM) on mobile handsets, and Personal Digital Assistants (PDAs).

As with the DiskOnChip Plus family (G2), DiskOnChip G3 content protection and security-enabling features offer several benefits. Two write- and read-protected partitions, with both software- and hardware-based protection, can be configured independently for maximum design flexibility. The 16-byte Unique ID (UID) identifies each flash device, eliminating the need for a separate ID device on the motherboard. The 6KB One Time Programmable (OTP) area, written to once and then locked to prevent data and code from being altered, is ideal for storing customer and product-specific information.

DiskOnChip G3 64MB (512Mb) has a 2KB Programmable Boot Block. This block provides eXecute In Place (XIP) functionality, enabling DiskOnChip G3 to replace the boot device and function as the only non-volatile memory device on-board. Eliminating the need for an additional boot device reduces hardware expenditures, board real estate, programming time, and logistics.

M-Systems' patented TrueFFS software technology fully emulates a hard disk to manage the files stored on DiskOnChip G3. This transparent file system management enables read/write operations that are identical to a standard, sector-based hard disk. In addition, TrueFFS employs patented methods, such as virtual mapping, dynamic and static wear-leveling, and automatic block management to ensure high data reliability and to maximize flash life expectancy.

2.2 64MB (512Mb) Standard Interface

2.2.1 System Interface

See Figure 1 for a simplified I/O diagram for a standard interface of DiskOnChip G3 64MB (512Mb).

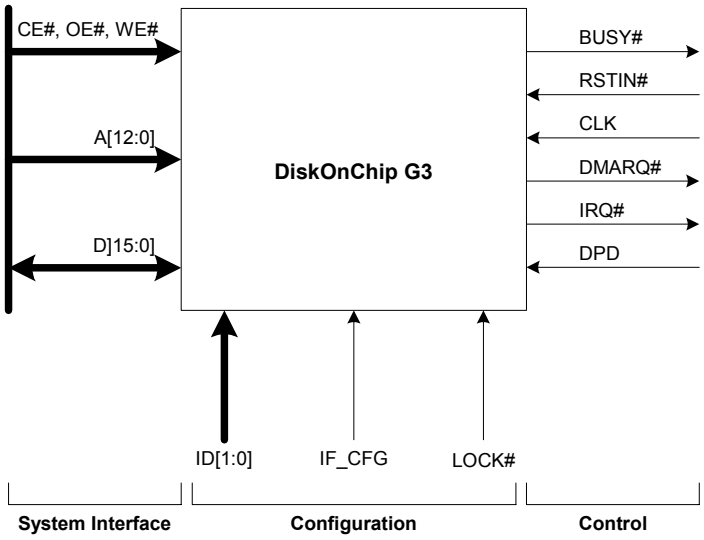


Figure 1: Standard Interface Simplified I/O Diagram (DiskOnChip G3 64MB/512Mb)

2.2.2 Signal Description

DiskOnChip G3 FBGA packages support identical signals. The related ball designations are listed in the signal descriptions, presented in logic groups, in **Error! Reference source not found.**.

7x10 FBGA Package

Table 1: Signal Descriptions for Standard Interface (DiskOnChip 64MB/512Mb G3 7x10 FBGA Package)

Signal	Ball No.	Input Type	Description	Signal Type
System Interface				
A[12:11] A[10:8] A[7:4] A[3:0]	D7, C7 F6, E6, C6 C2, D2, E2, F2 D1, E1, F1, G1	ST	Address bus. A0 is multiplexed with the DPD ball.	Input
D[15:14] D[13:12] D[11:8]	H7, K7 H6, J6 K4, J3, H3, K2	ST, R8	Data bus, high byte. Not used and may be left floating when IF_CFG is set to 0 (8-bit mode).	Input/ Output
D[7:6] D[5:3] D[2:0]	J7, G6 K6, H5, H4 K3, G3, J2	ST	Data bus, low byte.	Input/ Output
CE#	H1	ST	Chip Enable, active low	Input
OE#	H2	ST	Output Enable, active low	Input
WE#	C5	ST	Write Enable, active low	Input
Configuration				
ID[1:0]	G8, F7	ST	Identification. Configuration control to support up to four chips cascaded in the same memory window. Chip 1 = ID1, ID0 = VSS, VSS (0,0); must be used for single chip configuration Chip 2 = ID1, ID0 = VSS, VCCQ (0,1) Chip 3 = ID1, ID0 = VCCQ, VSS (1,0) Chip 4 = ID1, ID0 = VCCQ, VCCQ (1,1)	Input
LOCK#	E7	ST	Lock, active low. When active, provides full hardware data protection of selected partitions.	Input
IF_CFG	F3	ST	Interface Configuration, 1 (VCCQ) for 16-bit interface mode, 0 (VSS) for 8-bit interface mode.	Input
Control				
BUSY#	E4	OD	Busy, active low, open drain. Indicates that DiskOnChip is initializing and should not be accessed. A 10 KΩ pull-up resistor is required if this ball drives an input. A 10 KΩ pull-up resistor is recommended even if this ball is not used.	Output
RSTIN#	D4	ST	Reset, active low.	Input
CLK	K5	ST	System Clock.	Input

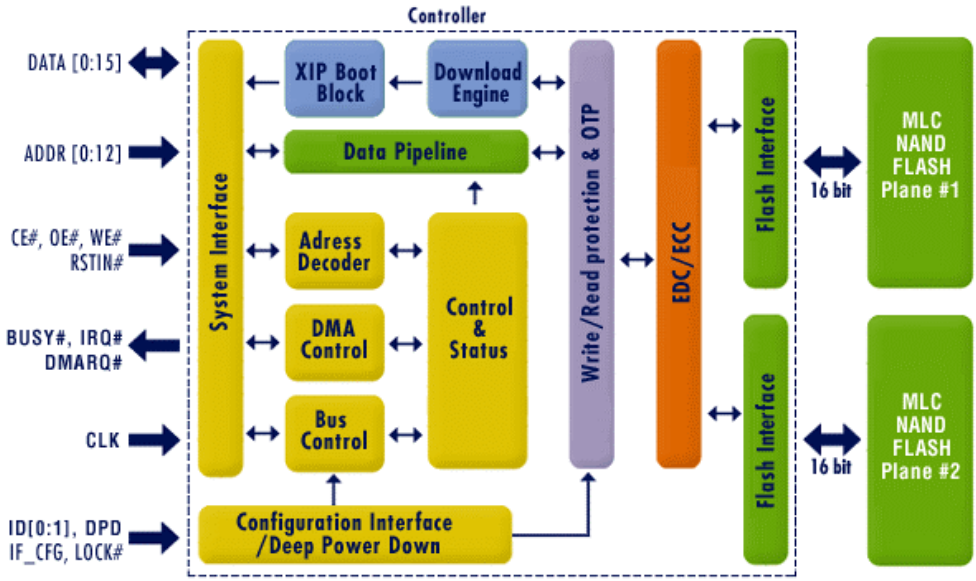
Signal	Ball No.	Input Type	Description	Signal Type
DMARQ#	G7	OD	DMA Request, active low. A 10 KΩ pull-up resistor is required if this ball drives an input. A 10 KΩ pull-up resistor is recommended even if this ball is not used.	Output
IRQ#	F8	OD	Interrupt Request, active low. A 10 KΩ pull-up resistor is required if this ball drives an input. A 10 KΩ pull-up resistor is recommended even if this ball is not used.	Output
DPD	G1	ST	Deep Power-Down. Used to enter and exit Deep Power-Down mode. This ball is assigned A0 instead of DPD when working in 8-bit mode.	Input
Power				
VCC	J4	-	Device supply. Requires a 10 nF and 0.1 µF capacitor.	Supply
VCCQ	J5	-	I/O power supply. Sets the logic **1** voltage level range of I/O balls. VCCQ may be either 2.5V to 3.6V or 1.65V to 2.0V. Requires a 10 nF and 0.1 µF capacitor.	Supply
VSS	G2, J8	-	Ground. All VSS balls must be connected.	Supply
Other				
RSRVD	E3	-	Reserved. If compatibility with previous DiskOnChip versions is necessary: In 16-bit mode (IF_CFG = 1) this ball must be connected to GND for compatibility with G2 devices. In 8-bit mode (IF_CFG = 0) may be left floating. Refer to the *DiskOnChip Plus (G2) to DiskOnChip G3/P3* migration guide for design guidelines when migrating from previous DiskOnChip versions (G2).	
	See **Error! Reference source not found.**	-	Reserved. Other reserved signals are not connected internally and must be left floating to guarantee forward compatibility with future products.	
	M	-	Mechanical. These balls are for mechanical placement, and are not connected internally.	
	A	-	Alignment. This ball is for device alignment and is not connected internally.	

The following abbreviations are used: IN - Standard (non-Schmidt) input, ST - Schmidt Trigger input, OD - Open drain output, R8 - Nominal 22K pull-up resistor, enabled only for 8-bit interface mode (IF_CFG input is 0)

3. THEORY OF OPERATION

3.1 Overview

DiskOnChip G3 consists of the following major functional blocks, as shown in Figure 2.



*ADDR[0] and DPD are multiplexed on the same ball.

Figure 2: DiskOnChip G3 Simplified Block Diagram, Standard Interface

These components are described briefly below and in more detail in the following sections.

- **System Interface** for the host interface.
- **Configuration Interface** for configuring DiskOnChip G3 to operate in 8-bit, 16-bit mode, cascaded configuration, hardware read/write protection and entering/exiting Deep Power-Down mode.
- **Read/Write Protection and OTP** for advanced data/code security and protection.
- **Programmable Boot Block with XIP** functionality enhanced with a **Download Engine (DE)** for system initialization capability.
- **Error Detection and Error Correction Code (EDC/ECC)** for on-the-fly error handling.
- **Data Pipeline** through which the data flows from the system to the NAND flash arrays.
- **Control & Status** block that contains registers responsible for transferring the address, data and control information between the TrueFFS driver and the flash media.
- **Flash Interface** that interfaces to two NAND flash planes.
- **Bus Control** for translating the host bus address, and data and control signals into valid NAND flash signals.
- **Address Decoder** to enable the relevant unit inside the DiskOnChip controller, according to the address range received from the system interface.

3.2 System Interface

3.2.1 Standard (NOR-Like) Interface

The system interface block provides an easy-to-integrate NOR-like (also SRAM and EEPROM-like) interface to DiskOnChip G3, enabling it to interface with various CPU interfaces, such as a local bus, ISA bus, NOR interface, SRAM interface, EEPROM interface or any other compatible interface. In addition, the EEPROM-like interface enables direct access to the Programmable Boot Block to permit XIP (Execute-In-Place) functionality during system initialization.

A 13-bit wide address bus enables access to the DiskOnChip G3 8KB memory window (as shown in Section 6.5). A 32-bit internal data bus is supported by parallel access to two 32MB (256Mb) flash planes (for 64MB/512Mb single-die devices), each of which enables 16-bit access. This 16-bit data bus permits 16-bit wide access to the host.

The Chip Enable (CE#), Write Enable (WE#) and Output Enable (OE#) signals trigger read and write cycles. A write cycle occurs while both the CE# and the WE# inputs are asserted. Similarly, a read cycle occurs while both the CE# and OE# inputs are asserted. Note that DiskOnChip G3 does not require a clock signal. It features a unique analog static design, optimized for minimal power consumption. The CE#, WE# and OE# signals trigger the controller (e.g., system interface block, bus control and data pipeline) and flash access.

The Reset In (RSTIN#) and Busy (BUSY#) control signals are used in the reset phase.

The Interrupt Request (IRQ#) signal can be used when long I/O operations, such as Block Erase, delay the CPU resources. The signal is also asserted when a Data Protection violation has occurred. This signal frees the CPU to run other tasks, continuing read/write operations with DiskOnChip G3 only after the IRQ# signal has been asserted and an interrupt handling routine (implemented in the OS) has been called to return control to the TrueFFS driver.

The DMARQ# output is used to control multi-page DMA operations, and the CLK input is used to support MultiBurst operation when reading flash data. See Section 4.1 for further information.

3.3 Configuration Interface

The Configuration Interface block enables the designer to configure DiskOnChip G3 to operate in different modes. The ID[1:0] signals are used in a cascaded configuration (refer to Section 9.5), the DPD signal is used to enter and exit Deep Power-Down mode (see Section 6.3), the LOCK# signal is used for hardware write/read protection, and the IF_CFG signal is used to configure 8/16-bit access.

3.4 Protection and Security-Enabling Features

The Protection and Security-Enabling block, consisting of read/write protection, UID and an OTP area, enables advanced data and code security and content protection. Located on the main route of traffic between the host and the flash, this block monitors and controls all data and code transactions to and from DiskOnChip G3.

3.4.1 Read/Write Protection

Data and code protection is implemented through a Protection State Machine (PSM). The user can configure one or two independently programmable areas of the flash memory as read protected, write protected, or read/write protected.

A protected partition may be protected by either/both of these hardware mechanisms:

- 64-bit protection key
- Hard-wired LOCK# signal

If the Lock option is enabled (by means of software) and the LOCK# signal is asserted, the protected partition has an additional hardware lock that prevents read/write access to the partition, even with the use of the correct protection key.

The size and protection attributes of the protected partition are defined during the media-formatting stage.

In the event of an attempt to bypass the protection mechanism, illegally modify the protection key or in any way sabotage the configuration parameters, the entire DiskOnChip G3 becomes both read and write protected, and is completely inaccessible.

For further information on hardware protection, please refer to the *TrueFFS Software Development Kit (SDK)* developer guide.

3.4.2 Unique Identification (UID) Number

Each DiskOnChip G3 is assigned a 16-byte UID number. Burned onto the flash during production, the UID cannot be altered and is unique worldwide. The UID is essential in security-related applications, and can be used to identify end-user products in order to fight fraudulent duplication by imitators.

3.4.3 One-Time Programmable (OTP) Area

The 6KB OTP area is user programmable for complete customization. The user can write to this area once, after which it is automatically and permanently locked. After it is locked, the OTP area becomes read only, just like a ROM device.

Typically, the OTP area is used to store customer and product information such as: product ID, software version, production data, customer ID and tracking information.

3.4.4 One-Time Write (ROM-Like) Partition

A partition in the DiskOnChip G3 can be set as One-Time Write. After it is locked, this partition becomes read only, just like a ROM device. Its capacity is defined during the media-formatting stage.

3.4.5 Sticky Lock (SLOCK)

The boot partition can be locked automatically by hardware after the boot phase is completed and the device is in Normal mode. This is done by setting the Sticky Lock (SLOCK) bit in the Output Control register to 1. This has the same effect as asserting the LOCK# signal. Once set, SLOCK can only be cleared by asserting the RSTIN# input. Like the LOCK# input, assertion of this bit prevents

the protection key from disabling the protection for a given partition. There is no need to mount the partition before calling a hardware protection routine.

This feature can be useful when the boot code in the boot partition must be read/write protected. Upon power-up, the boot code must be unprotected so the CPU can boot directly from DiskOnChip. At the end of the boot process, protection can be set until the next power-up or reset.

3.5 Programmable Boot Block with eXecute In Place (XIP) Functionality

The Programmable Boot Block with XIP functionality enables DiskOnChip G3 to act as a boot device in addition to performing flash disk data storage functions. This eliminates the need for expensive, legacy NOR flash or any other boot device on the motherboard.

The Programmable Boot Block on DiskOnChip G3 64MB (512Mb) is 2KB in size. The Download Engine (DE), described in the next section, expands the functionality of this block by copying the boot code from the flash into the boot block.

DiskOnChip G3 64MB (512Mb) devices may be cascaded in order to form a larger flash disk. When DiskOnChip G3 512Mb (64MB) is connected with a standard NOR-like interface, up to four devices may be cascaded to create a 2Gb flash disk.

Note: When more than one DiskOnChip G3 64MB (512Mb) device is cascaded, a maximum boot block of 4KB is available. The Programmable Boot Block of each device is mapped to a unique address space.

3.6 Download Engine (DE)

Upon power-up or when the RSTIN# signal is asserted, the DE automatically downloads the Initial Program Loader (IPL) to the Programmable Boot Block. The IPL is responsible for starting the booting process. The download process is quick, and is designed so that when the CPU accesses DiskOnChip G3 for code execution, the IPL code is already located in the Programmable Boot Block. During the download process, DiskOnChip G3 does not respond to read or write accesses. Host systems must therefore observe the requirements described in Section 10.3.6.

In addition, the DE downloads the data protection rules from the flash to the Protection State Machines (PSM), so that DiskOnChip G3 is secure and protected from the first moment it is active.

During the download process, DiskOnChip G3 asserts the BUSY# signal to indicate to the system that it is not yet ready to be accessed. Once BUSY# is negated, the system can access DiskOnChip G3.

A failsafe mechanism prevents improper initialization due to a faulty VCC or invalid assertion of the RSTIN# input. Another failsafe mechanism is designed to overcome possible NAND flash data errors. It prevents internal registers from powering up in a state that bypasses the intended data protection. In addition, any attempt to sabotage the data structures causes the entire DiskOnChip to become both read and write protected, and completely inaccessible.

3.7 Error Detection Code/Error Correction Code (EDC/ECC)

Because NAND-based MLC flash is prone to errors, it requires unique error-handling capability. M-Systems' x2 technology implements 4-bit Error Detection Code/Error Correction Code (EDC/ECC),

based on a patented combination of Bose, Chaudhuri and Hocquenghem (BCH) and Hamming code algorithms. Error Detection Code (EDC) is implemented in hardware to optimize performance, while Error Correction Code (ECC) is performed in software, when required, to save silicon costs.

Each time a 512-byte page is written, additional parity bits are calculated and written to the flash. Each time data is read from the flash, the parity bits are read and used to calculate error locations.

The Hamming code can detect 2 errors per page and correct 1 error per page. The BCH code can detect and correct 4 errors per page. It can detect 5 errors per page with a probability of 99.9%. It ensures that the minimal amount of code required is used for detection and correction to deliver the required reliability without degrading performance.

3.8 Data Pipeline

DiskOnChip G3 uses a two-stage pipeline mechanism, designed for maximum performance while enabling on-the-fly data manipulation, such as read/write protection and Error Detection/Error Correction. Refer to technical note TN-DOC-014, *Pipeline Mechanism in DiskOnChip*, for further information.

3.9 Control and Status

The Control and Status block contains registers responsible for transferring address, data and control information between the DiskOnChip TrueFFS driver and the flash media. Additional registers are used to monitor the status of the flash media (ready/busy) and the DiskOnChip controller. For further information on the DiskOnChip registers, refer to Section 7.

3.10 Flash Architecture

DiskOnChip G3 64MB (512Mb) consists of two 32MB (256Mb) flash planes that consist of 1024 blocks each, organized in 64 pages, as follows:

- **Page** – Each page contains 512 bytes of user data and a 16-byte extra area that is used to store flash management and EDC/ECC signature data, as shown in Figure 3.
- **Block (Erase Unit)** – Each block contains 64 pages (total of 256Kb), as shown in Figure 4. A block is the minimal unit that can be erased, and is sometimes referred to as an erase block.

  Note: Since the device works with multiple planes, the operational block size is 512Kb, as described in the next section.

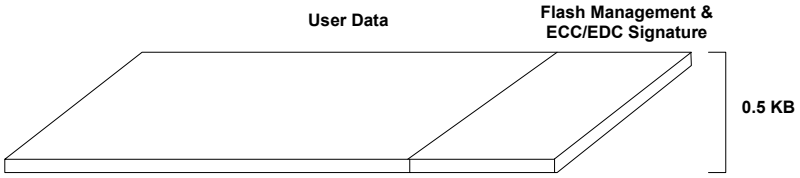


Figure 3: Page Structure

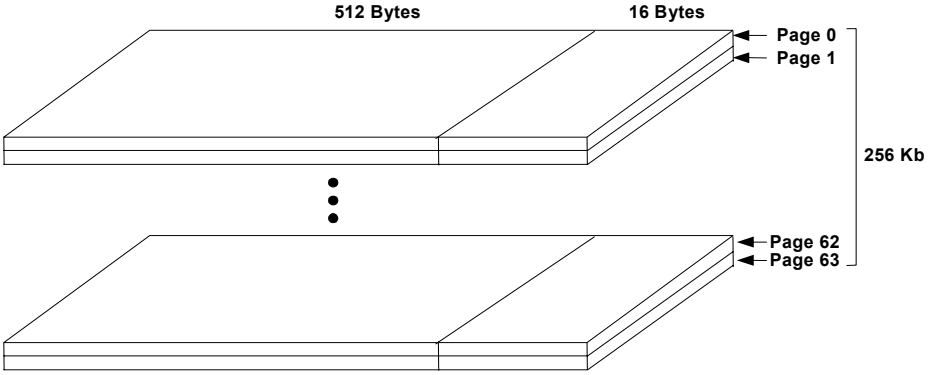


Figure 4: Block Structure

Parallel Multi-Plane Access

The two 32MB (256Mb) flash planes operate in parallel, thereby providing a true 32-bit internal data bus and four times the read, write and erase performance. Two pages on different planes can be concurrently read or written if they have the same offset within their respective units, even if the units are unaligned.

Bad units are mapped individually on each plane by enabling unaligned unit access, as shown in Figure 5. Good units can therefore be aligned or unaligned, minimizing the effects of bad units on the media. Without this capability, a bad unit in one plane would cause a good unit in the second plane to be tagged as a bad unit, making it unusable. This customized method of bad unit handling for two planes enhances data utilization without adversely affecting performance.

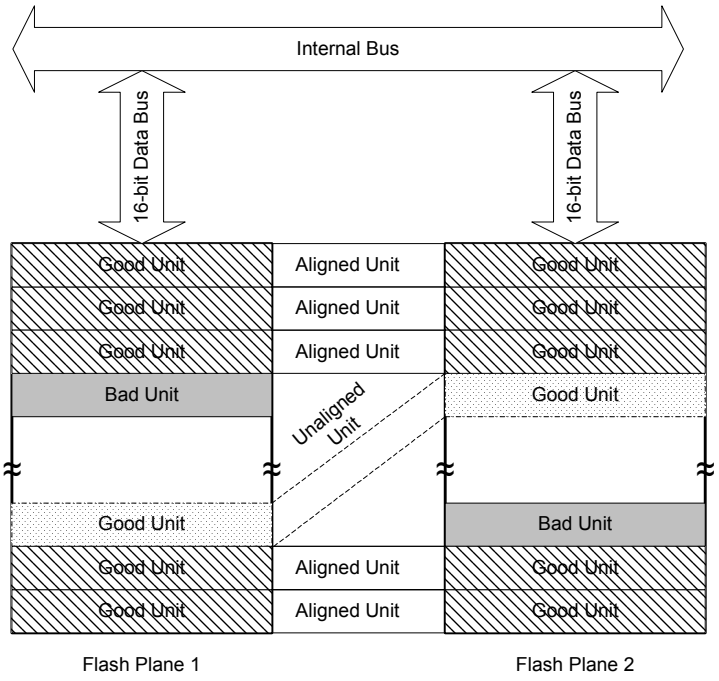


Figure 5: Unaligned Multi-Plane Access

4. X2 TECHNOLOGY

DiskOnChip G3 enhances performance using various proprietary techniques:

- Parallel access to the separate 32MB (256Mb) flash planes, thereby providing an internal 32-bit data bus. See Section 3.10 for further information.
- MultiBurst operation to read large chunks of data, providing a MultiBurst read speed of up to 80 MB/sec.
- DMA operation to release the CPU for other tasks in coordination with the platform's DMA controller. This is especially useful during the boot stage. Up to 64KB of data can be transferred during a DMA operation.
- Turbo operation to enhance read access time from 55 ns to 33 ns (standard interface, access to flash addresses).

4.1 MultiBurst Operation

MultiBurst operation is especially effective for large file reads that are typical during boot-up. During MultiBurst operation, data is read from the two flash planes in parallel through a 32-bit wide internal flash interface. Data is read by the host one 16-bit word after another using the CLK input, resulting in a MultiBurst read mode of up to 80 MB/sec. MultiBurst operation can only be performed on hosts that support burst reads. See Figure 6 below.

Note: A 25 nsec cycle time during MultiBurst can be achieved at Vcc = Vccq = 2.7 ~ 3.6V).

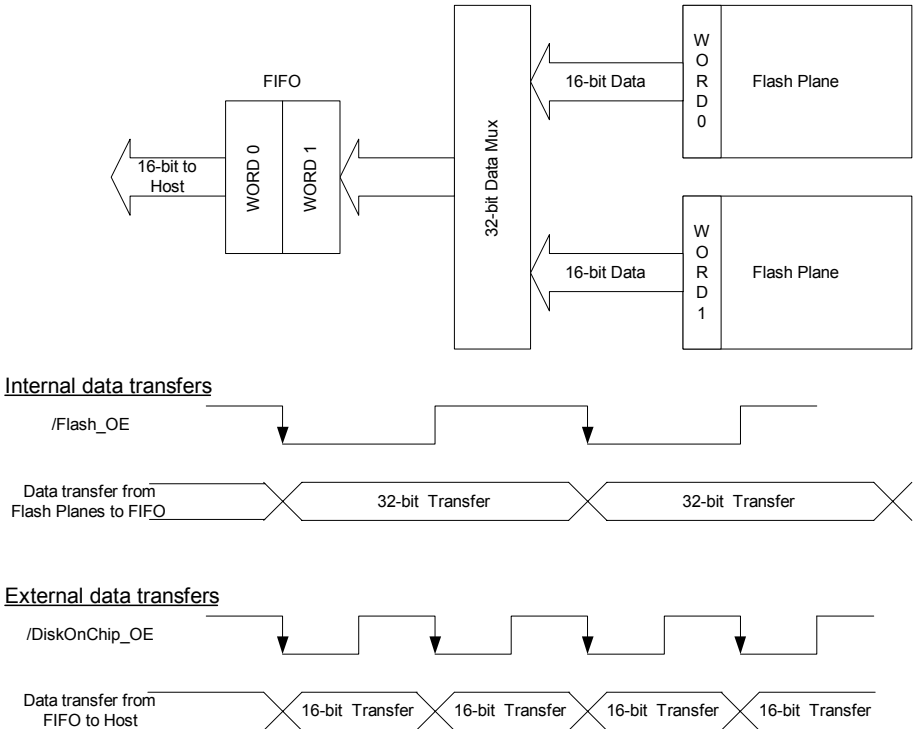


Figure 6: MultiBurst Operation

Note: DiskOnChip G3 does not support MultiBurst write operations.

MultiBurst operation is controlled by 5 bits in the MultiBurst Mode Control register: BURST_EN, CLK_INV, LATENCY, HOLD and LENGTH. For full details on this register, please refer to Section 7.

MultiBurst mode read cycles are supported via the CLK input, which is enabled by setting the BURST_EN bit in the MultiBurst Mode Control register.

To determine whether the rising or falling edge of the CLK input is sampled (called CLK0), the CLK_INV bit in the MultiBurst Mode Control register must be specified. When the CLK_INV bit is set to 0, CE# and OE# are sampled on the rising edge of CLK; when the CLK_INV bit is set to 1, sampling is done on the falling edge of CLK.

Notes: 1. When the CLK_INV bit is set to 1, sampling is done on the falling edge of CLK, and an additional half-clock cycle of latency is incurred. Data continues to be output on D[15:0] on the rising edge of CLK.

2. Burst mode is disabled upon assertion of the RSTIN# input, and the signal may therefore be left floating.

The LATENCY field is the third field that must be set in the MultiBurst Mode Control register. When the LATENCY field is set to 0, the host can latch the first 16-bit data word two clock cycles after CLK0. This time can be extended by up to seven clock cycles by programming the LATENCY field. After latching the first word, additional 16-bit data words can be latched on each subsequent clock cycle.

The HOLD bit in the MultiBurst Mode Control register can be set to hold each data word valid for two clock cycles rather than one.

The LENGTH field in the MultiBurst Mode Control register must be programmed with the length of the burst to be performed. As read cycles from the flash are volatile, each burst cycle must read exactly this number of words.

The CLK input can be toggled continuously or can be halted. When halting the CLK input, the following guidelines must be observed:

- After asserting OE# and CE#, LATENCY + 2 CLK cycles are required prior to latching the first word (2.5 CLK cycles if CLK_INV is set to 1).
- If the HOLD bit is set to 0, the host must provide one rising CLK edge for each word read, except for the last word latched, for which CLK does not need to be toggled.
- If the HOLD bit is set to 1, the host must provide two rising CLK edges for each word read, except for the last word, for which the second of the two CLK rising edges is not required.
- Subsequent toggling of the CLK is optional.

4.2 DMA Operation

DiskOnChip G3 provides a DMARQ# output that enables up to 64KB to be read from the flash by the host DMA controller. During DMA operation, the DMARQ# output is used to notify the host DMA controller that the next flash page is ready to be read, and the IRQ# pin indicates whether an error occurred while reading the data from the flash or the end of the DMA transfer was reached.

The DMARQ# output sensitivity is chosen by setting the EDGE bit in the DMA Control register[0]:

- **Edge** – The DMARQ# output pulses to logic 0 for 250~500 nsec to indicate to the DMA controller that a flash page is ready to be read. The EDGE bit is set to 1 for this mode.
- **Level** – The DMARQ# output is asserted to initiate the block transfer and returns to the negated state at the end of each block transfer. The EDGE bit is set to 0 for this mode.

The following steps are required to initiate a DMA operation:

1. Initialize the platform's DMA controller to transfer 512 bytes upon each assertion of the DMARQ# output. If the DMA controller supports an edge-sensitive DMARQ# signal, then initialize the DMA controller to transfer 512 bytes upon each DMA request. If the DMA controller supports a level-sensitive DMARQ# signal, then initialize the DMA controller to transfer data while DMARQ# is asserted.
2. Set the bits in the Interrupt Control register (see Section 7) to enable interrupts on an ECC error and at the end of the DMA operation.
3. Write to the DMA Control register[0] to set the DMA_EN bit, the EDGE bit and the number of sectors (SECTOR_COUNT field) to be transferred to the host. At this point, DiskOnChip G3 generates a DMA request to indicate to the host that it is ready to transfer data.
4. The host DMA controller reads one sector (512 bytes) of data from DiskOnChip G3.
5. If an ECC error is detected, an interrupt is generated (IRQ# signal asserted), the transfer of data is halted and control is returned to the host. If no ECC error is detected, a DMA request is initiated (DMARQ# signal asserted) and the next sector is read by the host.
6. The process continues until the last sector is read, after which DiskOnChip G3 generates an interrupt (IRQ# signal asserted) to indicate that it has transferred the last byte.

Notes: 1. DiskOnChip G3 generates a DMA request (DMARQ# signal asserted) after the last byte is read. It may therefore be necessary to clear the final DMA request from the DMA controller.

2. DMA operation may be aborted after transferring each 512-byte block (step 4) by clearing the DMA_EN bit in the DMA Control register[0].

4.3 Combined MultiBurst Mode and DMA Operation

When using MultiBurst mode and DMA operation together, and an interrupt is generated (IRQ# signal asserted), the Download Status register cannot be polled, as it will not comply with the MultiBurst mode timing specification. The following sequence is therefore required to respond to an interrupt request while in MultiBurst mode:

- Perform 7 write cycles to the NOP register.
- Turn off MultiBurst mode by writing to the MultiBurst Mode Control register.

4.4 Turbo Operation

In order to provide faster read access time, DiskOnChip G3 can be configured for Turbo operation by enabling the D[15:0] output buffers immediately after the assertion of OE# and CE#.

Enter Turbo operation by setting the TURBO bit in the Output Control register. For timing specifications for Turbo operation, see Section 10.3.

The read access time for the Programmable Boot Block is slower than the read access time for the registers. When DiskOnChip G3 is used for booting and data storage, the CPU therefore must be able to change the timing of system to achieve the access time of Turbo mode after the system is up.

5. HARDWARE PROTECTION

5.1 Method of Operation

DiskOnChip G3 enables the user to define two partitions that are protected (in hardware) against any combination of read or write operations. The two protected areas can be configured as read protected or write protected, and are protected by a protection key (i.e. password) defined by the user. Each of the protected areas can be configured separately and can function separately, providing maximum flexibility for the user.

The size and protection attributes (protection key, read, write, changeable, lock) of the protected partition are defined in the media formatting stage (DFORMAT utility or the format function in the TrueFFS SDK).

In order to set or remove read/write protection, the protection key (i.e., password) must be used, as follows:

- Insert the protection key to remove read/write protection.
- Remove the protection key to set read/write protection.

DiskOnChip G3 has an additional hardware safety measure. If the Lock option is enabled (by means of software) and the LOCK# signal is asserted, the protected partition has an additional hardware lock that prevents read/write access to the partition, even with the use of the correct protection key. It is possible to set the Lock protection for one session only; that is, until the next power-up or reset. This Sticky Lock feature can be useful when the boot code in the boot partition must be read/write protected. Upon power-up, the boot code must be unprotected so the CPU can run it directly from DiskOnChip G3. At the end of the boot process, protection can be set until the next power-up or reset.

Setting the Sticky Lock (SLOCK) bit in the Output Control register to 1 has the same effect as asserting the LOCK# signal. Once set, SLOCK can only be cleared by asserting the RSTIN# input. Like the LOCK# input, the assertion of this bit prevents the protection key from disabling the protection for a given partition. For more information, see Section 3.4.5. The target partition does require mounting before calling a hardware protection routine.

The only way to read or write from a protected partition is to insert the key (even DFORMAT cannot remove the protection). This is also true for modifying its attributes (protection key, read, write and lock). Read/write protection is disabled (the key is automatically removed) in each of the following events:

- Power-down
- Change of any protection attribute (not necessarily in the same partition)
- Write operation to the IPL area
- Removal of the protection key.

For further information on hardware protection, please refer to the *TrueFFS Software Development Kit (SDK)* developer guide.

5.2 Low-Level Structure of the Protected Area

The first five blocks in DiskOnChip G3 contain foundry information, the Data Protect structures, IPL code, and bad block mapping information. See Figure 7.

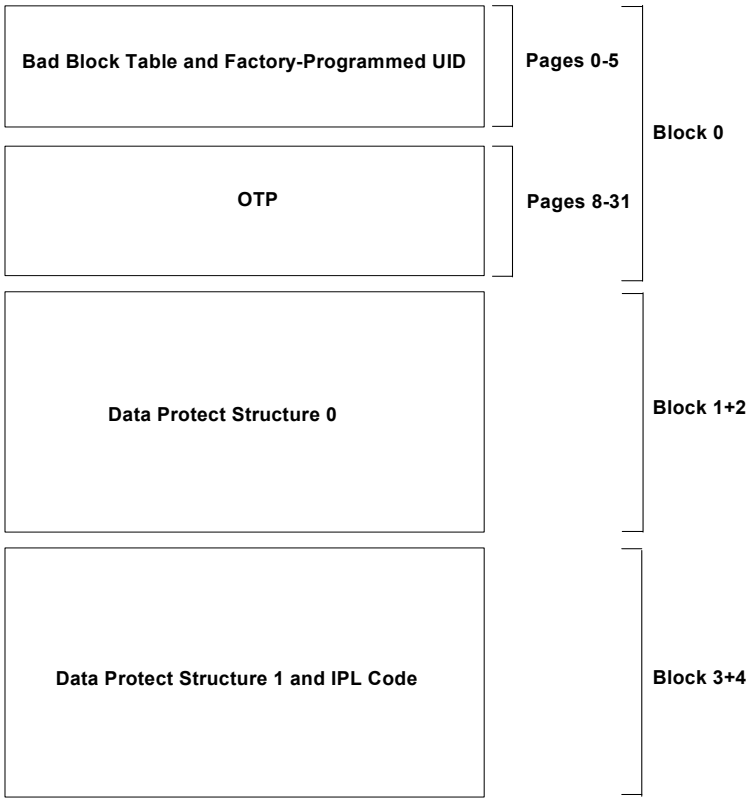


Figure 7: Low Level Structure of DiskOnChip G3

Blocks 0-4 in DiskOnChip G3 contain the following information:

Block 0

- Bad Block Table (page 4). Contains the information on unusable erase units on the flash media.
- UID (16 bytes). This number is written during the manufacturing stage, and cannot be altered at a later time.
- Customer OTP (occupies pages 8-31). The OTP area is written once and then locked.

Block 1 and 2

- Data Protect Structure 0. This structure contains configuration information on one of the two user-defined protected partitions. Block 2 is a copy of Block 1 for redundancy purposes.

Block 3 and 4

- Data Protect Structure 1. This structure contains configuration information on one of the two user-defined protected partitions.
- IPL Code (2KB). This is the boot code that is downloaded by the DE to the internal boot block.
- Block 4 is a copy of Block 3 for redundancy purposes.

6. MODES OF OPERATION

DiskOnChip G3 operates in one of three basic modes:

- Normal mode
- Reset mode
- Deep Power-Down mode

The current mode of the chip can always be determined by reading the DiskOnChip Control register. Mode changes can occur due to any of the following events:

- Assertion of the RSTIN# signal sets the device in Reset mode.
- During host power-up, boot detector circuitry sets the device in Reset mode.
- A valid write sequence to DiskOnChip G3 sets the device in Normal mode. This is done automatically by the TrueFFS driver on power-up (reset sequence end).
- Switching back from Normal mode to Reset mode can be done by a valid write sequence to DiskOnChip G3, or by triggering the boot detector circuitry (via a soft reset).
- Deep Power-Down
- A valid write sequence, initiated by software, sets the device from Normal mode to Deep Power-Down mode. Twelve read cycles from offset 0x1FFF set the device back to Normal mode. Alternately, the device can be set back to Normal mode with an extended access time during a read from the Programmable Boot Block.
- Asserting the RSTIN# signal and holding it in this state puts the device in Deep Power-Down mode. When RSTIN# is released, the device is left in Reset mode.
- Toggling the DPD signal as defined by the DPD Control register.

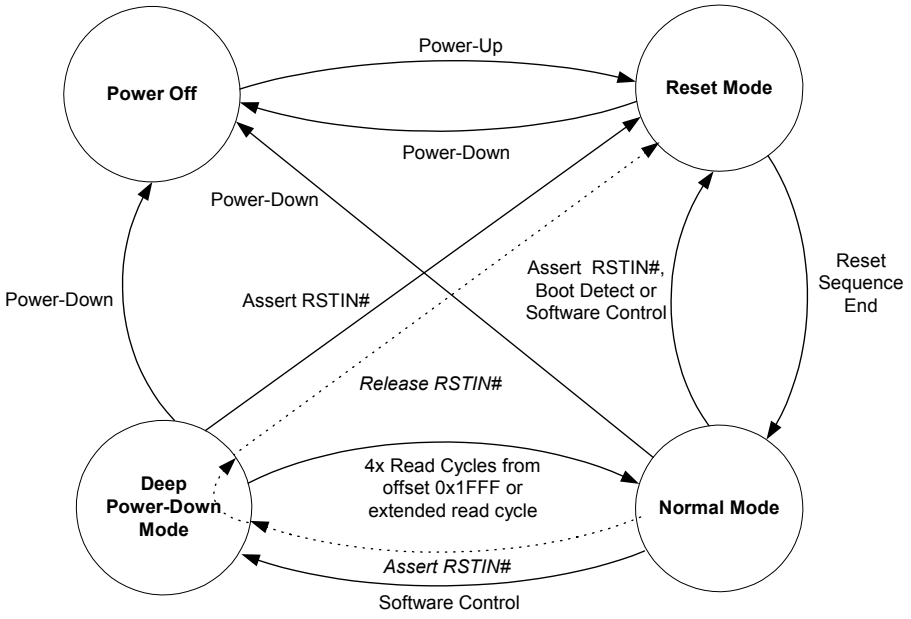


Figure 8: Operation Modes and Related Events

6.1 Normal Mode

This is the mode in which standard operations involving the flash memory are performed. Normal mode is entered when a valid write sequence is sent to the DiskOnChip Control register and Control Confirmation register. A write cycle occurs when both the CE# and WE# inputs are asserted. Similarly, a read cycle occurs when both the CE# and OE# inputs are asserted. Because the flash controller generates its internal clock from these CPU bus signals and some read operations return volatile data, it is essential that the timing requirements specified in Section 10.3 be met. It is also essential that read and write cycles not be interrupted by glitches or ringing on the CE#, WE#, and OE# inputs. All inputs to DiskOnChip G3 are Schmidt Trigger types to improve noise immunity.

6.2 Reset Mode

In Reset mode, DiskOnChip G3 ignores all write cycles, except for those to the DiskOnChip Control register and Control Confirmation register. All register read cycles return a value of 00H.

Before attempting to perform any operation, the device is set to Normal mode by TrueFFS software.

6.3 Deep Power-Down Mode

While in Deep Power-Down mode, DiskOnChip G3's quiescent power dissipation is reduced by disabling internal high current consumers (e.g. voltage regulators, input buffers, oscillator etc.). The following signals are also disabled in this mode:

- **Standard interface**: Input buffers A[12:0], WE#, D[15:0] and OE# (when CE# is negated)

To enter Deep Power-Down mode, a proper sequence must be written to the DiskOnChip G3 Control registers and the CE# input must be negated. All other inputs should be VSS or VCC.

Asserting the RSTIN# signal and holding it in low state puts the device in Deep Power-Down mode. When the RSTIN# signal is released, the device is left in Reset mode.

In Deep Power-Down mode, write cycles have no effect and read cycles return indeterminate data (DiskOnChip G3 does not drive the data bus). Entering Deep Power-Down mode and then returning to the previous mode does not affect the value of any register.

To exit Deep Power-Down mode, use one of the following methods:

- Read twelve times from address 1FFFH (Programmable Boot Block). The data returned is undefined.
- Perform a single read cycle from the Programmable Boot Block with an extended access time and address hold time as specified in the timing diagrams. The data returned will be correct.
- Toggle the DPD input as defined by the DPD Control register, wait a minimum of 600 nS, and then perform a read/write cycle with normal timing, as specified in the timing diagrams.

Applications that use DiskOnChip G3 as a boot device must ensure that the device is not in Deep Power-Down mode before reading the Boot vector/instructions. This can be done by pulsing RSTIN# to the asserted state and waiting for the BUSY# output to be negated, or by entering Reset mode via software (the Programmable Boot Block addresses can be accessed in Deep Power-Down mode).

6.4 TrueFFS Technology

6.4.1 General Description

M-Systems' patented TrueFFS technology was designed to maximize the benefits of flash memory while overcoming inherent flash limitations that would otherwise reduce its performance, reliability and lifetime. TrueFFS emulates a hard disk, making it completely transparent to the OS. In addition, since it operates under the OS file system layer (see Figure 9), it is completely transparent to the application.

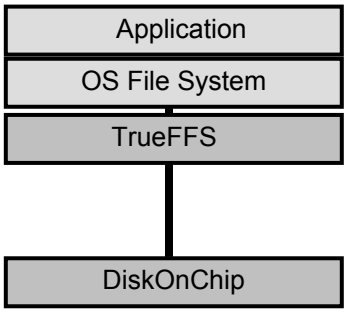


Figure 9: TrueFFS Location in System Hierarchy

TrueFFS technology support includes:

- Binary driver support for all major OSs
- TrueFFS Software Development Kit (TrueFFS SDK)
- Boot Software Development Kit (BDK)
- Support for all major CPUs, including 8, 16 and 32-bit bus architectures.

TrueFFS technology features:

- Block device API
- Flash file system management
- Bad-block management
- Dynamic virtual mapping
- Dynamic and static wear-leveling
- Power failure management
- Implementation of MLC-tailored EDC/ECC
- Performance optimization
- Compatibility with all DiskOnChip products

6.4.2 Built-In Operating System Support

The TrueFFS driver is integrated into all major OSs, including Symbian, Palm OS, Pocket PC 2002/3, Smartphone 2002/3, Windows CE/NT, Linux (various kernels), Nucleus, and others. For a complete listing of all available drivers, please refer to M-Systems' website, www.m-systems.com. It is advised to use the latest driver versions that can be downloaded from the website.

6.4.3 TrueFFS Software Development Kit (SDK)

The basic *TrueFFS Software Development Kit (SDK)* developer guide provides the source code for the TrueFFS driver. It can be used in an OS-less environment or when special customization of the driver is required for proprietary OSs.

When using DiskOnChip G3 as the boot replacement device, TrueFFS SDK also incorporates in its source code the boot software that is required for this configuration (this package is also available separately). Please refer to the *DiskOnChip Boot Software Development Kit (BDK)* developer guide for further information on using this software package.

Note: DiskOnChip G3 is supported by TrueFFS 6.1 and above.

6.4.4 File Management

TrueFFS accesses the flash memory within DiskOnChip G3 through an 8KB window in the CPU memory space. TrueFFS provides block device API by using standard file system calls, identical to those used by a mechanical hard disk, to enable reading from and writing to any sector on DiskOnChip G3. This makes DiskOnChip G3 compatible with any file system and file system utilities, such as diagnostic tools and applications.

Note: DiskOnChip G3 is shipped unformatted and contains virgin media.

6.4.5 Bad-Block Management

Since NAND flash is an imperfect storage media, it can contain bad blocks that cannot be used for storage because of their high error rates. TrueFFS automatically detects and maps out bad blocks upon system initialization, ensuring that they are not used for storage. This management process is completely transparent to the user, who is unaware of the existence and location of bad blocks, while remaining confident of the integrity of data stored.

6.4.6 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the *erase cycle limit*, or *write endurance limit*, and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device. In DiskOnChip G3, the erase cycle limit of the flash is 100,000 erase cycles. This means that after approximately 100,000 erase cycles, the erase block begins to generate storage errors at a rate significantly higher than the error rate that is typical to the flash.

In a typical application, and especially if a file system is used, specific pages are constantly updated (e.g., the page/s that contain the FAT, registry, etc.). Without any special handling, these pages would wear out more rapidly than other pages, reducing the lifetime of the entire flash.

To overcome this inherent deficiency, TrueFFS uses M-Systems' patented wear-leveling algorithm. This wear-leveling algorithm ensures that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime.

Dynamic Wear-Leveling

TrueFFS uses statistical allocation to perform dynamic wear-leveling on newly written data. This minimizes the number of erase cycles per block. Because a block erase is the most time-consuming operation, dynamic wear-leveling has a major impact on overall performance. This impact cannot be noticed during the first write to flash (since there is no need to erase blocks beforehand), but it is more and more noticeable as the flash media becomes full.

Static Wear-Leveling

Areas on the flash media may contain static files, characterized by blocks of data that remain unchanged for very long periods of time, or even for the whole device lifetime. If wear-leveling were only applied on newly written pages, static areas would never be cycled. This limited application of wear-leveling would lower life expectancy significantly in cases where flash memory contains large static areas. To overcome this problem, TrueFFS forces data transfer in static areas as well as in dynamic areas, thereby applying wear-leveling to the entire media.

6.4.7 Power Failure Management

TrueFFS uses algorithms based on "erase after write" instead of "erase before write" to ensure data integrity during normal operation and in the event of a power failure. Used areas are reclaimed for erasing and writing the flash management information into them only *after* an operation is complete. This procedure serves as a check on data integrity.

The "erase after write" algorithm is also used to update and store mapping information on the flash memory. This keeps the mapping information coherent even during power failures. The only mapping information held in RAM is a table pointing to the location of the actual mapping information. This table is reconstructed during power-up or after reset from the information stored in the flash memory.

To prevent data from being lost or corrupted, TrueFFS uses the following mechanisms:

- When writing, copying, or erasing the flash device, the data format remains valid at all intermediate stages. Previous data is never erased until the operation has been completed and the new data has been verified.
- A data sector cannot exist in a partially written state. The operation is either successfully completed, in which case the new sector contents are valid, or the operation has not yet been completed or has failed, in which case the old sector contents remain valid.

6.4.8 Error Detection/Correction

TrueFFS implements a unique MLC-tailored Error Correction Code (ECC) algorithm to ensure data reliability. Refer to Section 3.7 for further information on the EDC/ECC mechanism.

6.4.9 Special Features Through I/O Control (IOCTL) Mechanism

In addition to standard storage device functionality, the TrueFFS driver provides extended functionality. This functionality goes beyond simple data storage capabilities to include features such as: formatting the media, read/write protection, boot partition(s) access, flash defragmentation and other options. This unique functionality is available in all TrueFFS-based drivers through the standard I/O control command of the native file system.

6.4.10 Compatibility

DiskOnChip G3 requires TrueFFS driver 6.x or higher. Since this driver does not support some of DiskOnChip products, migrating from other than DiskOnChip G3 to DiskOnChip G3 requires changing the TrueFFS driver.

When using different drivers (e.g. TrueFFS SDK, BDK, BIOS extension firmware, etc.) to access DiskOnChip G3, verify that all software is based on the same code base version. It is also important to use only tools (e.g. DFORMAT, DINFO, GETIMAGE, etc.) from the same version as the TrueFFS drivers used in the application. Failure to do so may lead to unexpected results, such as lost or corrupted data. The driver version can be verified by the sign-on messages displayed, or by the version information presented by the driver or tool.

6.5 8KB Memory Window

TrueFFS utilizes an 8KB memory window in the CPU address space, consisting of four 2KB sections as depicted in Figure 10. When in Reset mode, read cycles from sections 1 and 2 always return the value 00H to create a fixed and known checksum. When in Normal mode, these two sections are used for the internal registers. The 2KB Programmable Boot Block is in section 0 and section 3, to support systems that search for a checksum at the boot stage both from the top and bottom of memory. The addresses described here are relative to the absolute starting address of the 8KB memory window.

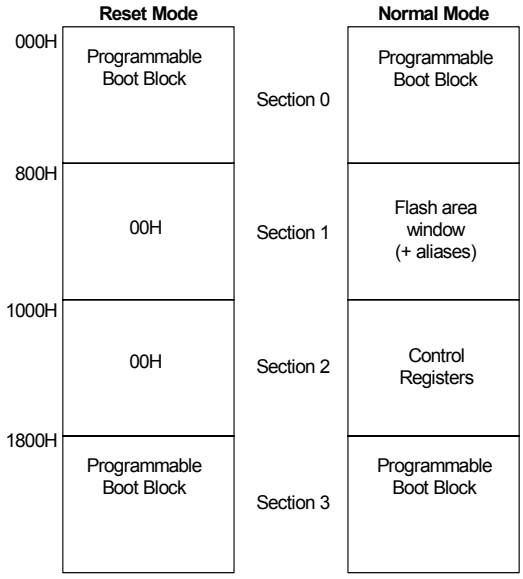


Figure 10: DiskOnChip G3 Memory Map

7. REGISTER DESCRIPTIONS

This section describes various DiskOnChip G3 registers and their functions, as listed in Table 2. Most DiskOnChip G3 registers are 8-bit, unless otherwise denoted as 16-bit.

Table 2: DiskOnChip G3 Registers

Address (Hex)	Register Name
103E	No Operation (NOP)
1000/1074	Chip Identification [1:0]
1004	Test
1008	Endian Control
100C	DiskOnChip Control
1072	DiskOnChip Control Confirmation
100A	Device ID Select
100E	Configuration
1010	Interrupt Control
1020	Interrupt Status
1014	Output Control
107C	DPD Control
1078/107A	DMA Control [1:0]
101A	Read Address Register
101C	MultiBurst Mode Control

7.1 Definition of Terms

The following abbreviations and terms are used within this section:

RFU — Reserved for future use. This bit is undefined during a read cycle and “don’t care” during a write cycle.

RFU_0 — Reserved for future use; when read, this bit always returns the value 0; when written, software should ensure that this bit is always set to 0.

RFU_1 — Reserved for future use; when read, this bit always returns the value 1; when written, software should ensure that this bit is always set to 1.

Reset Value — Refers to the value immediately present after exiting from Reset mode to Normal mode.

7.2 Reset Values

All registers return 00H while in Reset mode. The Reset value written in the register description is the register value after exiting Reset mode and entering Normal mode. Some register contents are undefined at that time (N/A).

7.3 Read Address Register

Description: This 16-bit register is used to specify the next 13-bit address to be read from DiskOnChip G3.

Address (hex): 101A

Type: Read/Write

Bit No	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Description	INC	ONE_BYTE	RFU_0	REG_ADDR[12:8]				
Reset Value	0	0	0	See explanation below				

Bit No	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Description	REG_ADDR[7:0]							
Reset Value	See explanation below							

Bit No.	Description
0-12	REG_ADDR[12:0]. Specifies the address of the register that will be read on the following read cycle. For 16-bit hosts, the LSB must be 0.
13	Reserved for future use.
14	ONE_BYTE. This bit is set when it is necessary to read/write only one byte of data from/to the Data Register. This bit is automatically cleared after the access to the Data Register.
15	INC (Increment). **1**: After each read cycle, the address is incremented by 1 byte (when IF_CFG = 0) or by 1 word (when IF_CFG = 1). **0**: The address is not automatically incremented, and the same address may be read repeatedly.

7.4 No Operation (NOP) Register

Description: A call to this 16-bit register results in no operation. To aid in code readability and documentation, software should access this register when performing cycles intended to create a time delay.

Address (hex): 103E

Type: Write

Reset Value: None

7.5 Chip Identification (ID) Register [0:1]

Description: These two 16-bit registers are used to identify the DiskOnChip device residing on the host platform. They always return the same value.

Address (hex): 1000/1074

Type: Read only

Reset Value: Chip Identification Register[0]: 0200H

Chip Identification Register[1]: FDFFH

7.6 Test Register

Description: This register enables software to identify multiple DiskOnChip G3 devices or multiple aliases in the CPUs memory space. Data written is stored but does not affect the behavior of DiskOnChip G3.

Address (hex): 1004

Type: Read/Write

Reset Value: 0

Bit No.	Description
7-0	D[7:0]: Data bits

7.7 Endian Control Register

Description: This 16-bit register is used to control the swapping of the low and high data bytes when reading or writing with a 16-bit host. This provides an Endian-independent method of enabling/disabling the byte swap feature.

Note: Hosts that support 8-bit access only do not need to write to this register.

Address (hex): 1008

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R							R/W
Description	RFU_0							SWAPL
Reset Value	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Read/Write	R							R/W
Description	RFU_0							SWAPH
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
0	SWAPL (Swap Low Byte): This bit must be set to enable byte swapping. If the bit is cleared, then byte swapping is disabled.
7-1	Reserved for future use.
8	SWAPH (Swap High Byte): This bit must be set to enable byte swapping. If the bit is cleared, then byte swapping is disabled.
15-9	Reserved for future use.

7.8 DiskOnChip Control Register/Control Confirmation Register

Description: These two registers are identical and contain information about the DiskOnChip G3 operational mode. After writing the required value to the DiskOnChip Control register, the complement of that data byte must also be written to the Control Confirmation register. The two writes cycles must not be separated by any other read or write cycles to the DiskOnChip G3 memory space, except for reads from the Programmable Boot Block space.

Address (hex): 100C/1072

Bit No	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Description	RFU_0			RST_LAT	BDET	MDWREN	Mode[1:0]	
Reset Value	0	0	0	1	0	0	0	0

Note: The DiskOnChip Control Confirmation register is write only

Bit No.	Description
1-0	Mode. These bits select the mode of operation, as follows: 00: Reset 01: Normal 10: Deep Power-Down
2	MDWREN (Mode Write Enable). The value 1 must be written to this bit when changing the mode of operation. It always returns 0 when read.
3	BDET (Boot Detect). This bit is set whenever the device has entered Reset mode as a result of the Boot Detector triggering. It is cleared by writing a 1 to this bit.
4	RST_LAT (Reset Latch). This bit is set whenever the device has entered the Reset mode as a result of the RSTIN# input signal being asserted or the internal voltage detector triggering. It is cleared by writing a 1 to this bit.
7-5	Reserved for future use.

7.9 Device ID Select Register

Description: In a cascaded configuration, this register controls which device provides the register space. The value of bits ID[0:1] is compared to the value of the ID configuration input pins/balls. The device whose ID input matches the value of bits ID[0:1] responds to read and write cycles.

Address (hex): 100A

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R						R/W	
Description	RFU_0						ID[1:0]	
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
1-0	ID[1:0] (Identification). The device whose ID input pins/balls match the value of bits ID[0:1] responds to read and write cycles to register space.
7-2	Reserved for future use.

7.10 Configuration Register

Description: This register indicates the current configuration of DiskOnChip G3. Unless otherwise noted, the bits are reset only by a hardware reset, and not upon boot detection or any other entry to Reset mode.

Address (hex): 100E

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R		R/W		R			
Description	IF_CFG	RFU_0	MAX_ID		RFU	RFU_0		VCCQ_3V
Reset Value	X	0	0	0	0	0	0	X

Bit No.	Description
0	VCCQ_3V: Reflects the level of VCCQ input. 0: VCCQ < 2.0V 1: VCCQ > 2.5V
6, 3-1	Reserved for future use.
5-4	MAX_ID (Maximum Device ID). This field controls the Programmable Boot Block address mapping when multiple devices are used in a cascaded configuration, using the ID[1:0] inputs. It should be programmed to the highest ID value that is found by software in order to map all available boot blocks into usable address spaces.
7	IF_CFG (Interface Configuration). Reflects the state of the IF_CFG input pin.

7.11 Interrupt Control Register

Description: This 16-bit register controls how interrupts are generated by DiskOnChip G3, and indicates which of the following five sources has asserted an interrupt:

0: Flash array is ready

1: Data protection violation

2: Reading or writing more flash data than was expected

3: BCH ECC error detected (this feature is provided to support multi-page DMA transfers)

4: Completion of a DMA operation

Address (hex): 1010

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R		R/W					
Description	RFU_0		ENABLE					
Reset Value	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Read/Write	R/W							
Description	GMASK	EDGE	MASK					
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
5-0	ENABLE. For each bit in this field: **1**: Enables the respective bit in the STATUS field of the Interrupt Status register to latch activity and cause an interrupt if the corresponding MASK bit is set. **0**: Holds the respective bit in the STATUS field in the cleared state. To clear a pending interrupt and re-enable further interrupts on that channel, the respective ENABLE bit must be cleared and then set.
7-6	Reserved for future use.
13-8	MASK. For each bit in this field: **1**: Enables the respective bit in the STATUS field of the Interrupt Status register to generate an interrupt by asserting the IRQ# output. **0**: Prevents the respective STATUS bit from generating an interrupt.
14	EDGE. Selects edge or level triggered interrupts: **0**: Specifies level-sensitive interrupts in which the IRQ# output remains asserted until the interrupt is cleared. **1**: Specifies edge-sensitive interrupts in which the IRQ# output pulses low and return to logic 1.

Bit No.	Description
15	GMASK (Global Mask). **1**: Enables the IRQ# output to be asserted. Setting this bit while one or more interrupts are pending will generate an interrupt. **0**: Forces the IRQ# output to the negated state.

7.12 Interrupt Status Register

Description: This register indicates which interrupt source created an interrupt.

Address (hex): 1020

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R		R/W					
Description	RFU_0		STATUS					
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
5-0	STATUS. Indicates which interrupt sources created an interrupt. For a list of the interrupt sources, please refer to the description of the Interrupt Control register.
7-6	Reserved for future use.

7.13 Output Control Register

Description: This register controls the behavior of certain output signals. This register is reset by a hardware reset, not by entering Reset mode.

Note: When multiple devices are cascaded, writing to this register will affect all devices regardless of the value of the ID[1:0] inputs.

Address (hex): 1014

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R					R/W		
Description	RFU_0					Turbo	PU_DIS	BUSY_EN
Reset Value	0	0	0	0	0	0	0	1

Bit No.	Description
0	BUSY_EN (Busy Enable). Controls the assertion of the BUSY# output during a download initiated by a soft reset. **1**: Enables the assertion of the BUSY# output **0**: Disables the assertion of the BUSY# output Upon the assertion of the RSTIN# input, this bit will be set automatically and the BUSY# output signal will be asserted until the completion of the download process.
1	PU_DIS (Pull-Up Disable). Controls the pull-up resistors D[15:8] as follows: **1**: Always disable the pull-ups **0**: Enable the pull-ups when IF_CFG = 0
2	TURBO. Activates turbo operation. **0**: DiskOnChip is used in normal operation, without improved access time. Output buffers are enabled only after a long enough delay to guarantee that there will be no more than a single transition on each bit. **1**. DiskOnChip is used in Turbo operation. Output buffers are enabled immediately after the assertion of OE# and CE#, resulting in improved access time. Read cycles from the Programmable Boot Block may result in additional noise and power dissipation due to multiple transitions on the data bus.
7-3	Reserved for future use.

7.14 DPD Control Register

Description: This register specifies the behavior of the DPD input signal.

Address (hex): 107C

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R				R/W			
Description	PD_OK	RFU_0			MODE[0:3]			
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
3-0	MODE[0:3]. Controls the behavior of the DPD input: 0000: DPD input is not used to control DPD mode 0001: DPD mode exited on rising edge of DPD input 0010: DPD mode exited on falling edge of DPD input 0100: DPD mode is entered when DPD=1 and exited when DPD=0 1000: DPD mode is entered when DPD=0 and exited when DPD=1
6-4	Reserved for future use.
7	PD_OK (Power- Down OK). This read-only bit indicates that it is currently possible to put DiskOnChip G3 in Deep Power-Down mode.

7.15 DMA Control Register [1:0]

Description: These two 16-bit registers specify the behavior of the DMA operation.

Address (hex): 1078/107A

DMA Control Register [o]								
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Read/Write	R	R/W						
Description	RFU_0	SECTOR_COUNT						
Reset Value	0	0	0	0	0	0	0	0

	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Read/Write	R	R/W			R			
Description	DMA_EN	PAUSE	EDGE	POLRTY	RFU_0			
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
6-0	SECTOR_COUNT. Specifies the number of 512-byte sectors to be transferred plus one. Writing a value of 0 indicates a transfer of one sector. Reading a value of 0 indicates that there is still one sector to be transferred). This field is decremented by DiskOnChip G3 after reading the ECC checksum from each sector. In the event of an ECC error, this field indicates the number of sectors remaining to be transferred.
11-7	Reserved for future use.
12	POLRTY (Polarity). Specifies the polarity of the DMARQ# output: **0**: DMARQ# is normally logic -1 and falls to initiate DMA **1**: DMARQ# is normally logic -0 and rises to initiate DMA
13	EDGE. Controls the behavior of the DMARQ# output: **1**: DMARQ# pulses to the asserted state for 250 nS (typical) to initiate the block transfer. **0**: DMARQ# switches to the active state to initiate the block transfer and returns to the negated state at the beginning of the cycle in which the DCNT field of the ECC Control register[0] reaches the value specified by the NEGATE_COUNT field of the DMA Control register[1].
14	PAUSE. This bit is set in the event of an ECC error during a DMA operation. After reading the ECC parity registers and correcting the errors, the software must clear this bit to resume the DMA operation.
15	DMA_EN (DMA Enable). Setting this bit enables DMA operation.

DMA Control Register [1]								
	Bits 15-10				**Bits 9-0**			
Read/Write	R				R/W			
Description	RFU_0				NEGATE_COUNT			
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
9-0	NEGATE_COUNT. When the EDGE bit of the DMA Control register[0] is 0, this field must be programmed to specify the bus cycle in which DMARQ# will be negated, as follows: NEGATE_COUNT = BYTES_REMAINING + 16 + BYTES_PER_CYCLE. Example: To negate DMARQ# at the beginning of the cycle in which the last word is to be transferred by a 16-bit host: NEGATE_COUNT = 2 + 16 + 2 = 20.
15-10	Reserved for future use.

7.16 MultiBurst Mode Control Register

Description: This 16-bit register controls the behavior of DiskOnChip G3 during MultiBurst mode read cycles.

Address (hex): 101C

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read/Write	R					R/W		
Description	RFU_0					HOLD	CLK_INV	BST_EN
Reset Value	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	12	Bit 11	Bit 10	Bit 9	Bit 8
Read/Write	R/W							
Description	LENGTH				LATENCY			
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Description
0	BST_EN (MultiBurst Mode Enable). Enables MultiBurst mode read cycles. **0**: The CLK input is disabled and may be left floating. Burst read cycles are not supported. **1**: The CLK input is enabled. Subsequent read cycles must be MultiBurst mode.
1	CLK_INV (Clock Invert). Selects the edge of the CLK input on which CE# and OE# are sampled. **0**: CE# and OE# are sampled on the rising edge of CLK. **1**: CE# and OE# are sampled on the falling edge of CLK, and there will be an additional ½ clock delay from CE#/OE# asserted until the first data word may be latched on D[15:0].
2	HOLD. Specifies if the data output on D[15:0] during MultiBurst mode read cycles should be held for an additional clock cycle. **0**: Data on the D[15:0] outputs is held for one clock cycle **1**: Data on the D[15:0] outputs is held for two clock cycles
3-7	Reserved for future use.
8-11	LATENCY. Controls the number of clock cycles between when DiskOnChip G3 samples OE# and CE# asserted and the first word of data is available to be latched by the host. This number of clock cycles is equal to 2 + LATECNCY. If HOLD = 1, then the data is available to be latched on this clock and on the subsequent clock.
12-15	LENGTH. Specifies the number of byte/words (depending on IF_CFG) to be transferred in each burst cycle: HOLD=0: Number of bytes/words = 2 ^ LENGTH HOLD=1: Number of bytes/words = 2 ^ (LENGTH – 1) Note: The maximum value of LENGTH is 10.

8. BOOTING FROM DISKONCHIP G3

8.1 Introduction

DiskOnChip G3 can function both as a flash disk and as the system boot device. DiskOnChip G3 default firmware contains drivers to enable it to perform as the OS boot device under DOS (see Section 8.2). For other OSs, please refer to the readme file of the TrueFFS driver.

If DiskOnChip G3 is configured as a flash disk and as the system boot device, it contains the boot loader, an OS image and a file system. In such a configuration, DiskOnChip G3 can serve as the only non-volatile device on board. Refer to Section 8.3.2 for further information on boot replacement.

8.2 Boot Procedure in PC-Compatible Platforms

When used in PC-compatible platforms, DiskOnChip G3 is connected to an 8KB memory window in the BIOS expansion memory range, typically located between 0C8000H to 0EFFFFH. During the boot process, the BIOS loads the TrueFFS firmware into the PC memory and installs DiskOnChip G3 as a disk drive in the system. When the operating system is loaded, DiskOnChip G3 is recognized as a standard disk. No external software is required to boot from DiskOnChip G3.

Figure 11 illustrates the location of the DiskOnChip G3 memory window in the PC memory map.

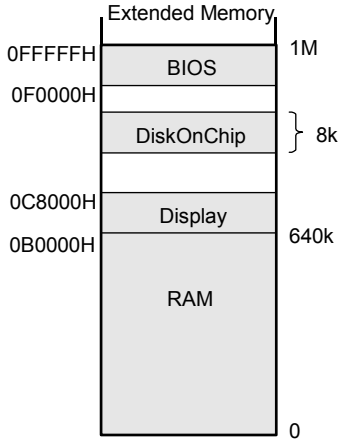


Figure 11: DiskOnChip G3 Memory Window in PC Memory Map

After reset, the BIOS code first executes the Power On Self-Test (POST) and then searches for all expansion ROM devices. When DiskOnChip G3 is located, the BIOS code executes from it the IPL code, located in the XIP portion of the Programmable Boot Block. This code loads the TrueFFS driver into system memory, installs DiskOnChip G3 as a disk in the system, and then returns control to the BIOS code. The operating system subsequently identifies DiskOnChip G3 as an available disk. TrueFFS responds by emulating a hard disk.

From this point onward, DiskOnChip G3 appears as a standard disk drive. It is assigned a drive letter and can be used by any application, without any modifications to either the BIOS set-up or the autoexec.bat/config.sys files. DiskOnChip G3 can be used as the only disk in the system, with or without a floppy drive, and with or without hard disks.

The drive letter assigned depends on how DiskOnChip G3 is used in the system, as follows:

- If DiskOnChip G3 is used as the only disk in the system, the system boots directly from it and assigns it drive C.
- If DiskOnChip G3 is used with other disks in the system:
    - DiskOnChip G3 can be configured as the last drive (the default configuration). The system assigns drive C to the hard disk and drive D to DiskOnChip G3.
    - Alternatively, DiskOnChip G3 can be configured as the system's first drive. The system assigns drive D to the hard disk and drive C to DiskOnChip G3.

If DiskOnChip G3 is used as the OS boot device when configured as drive C, it must be formatted as a bootable device by copying the OS files onto it. This is done by using the SYS command when running DOS.

8.3 Boot Replacement

8.3.1 PC Architectures

In current PC architectures, the first CPU fetch (after reset is negated) is mapped to the boot device area, also known as the *reset vector*. The reset vector in PC architectures is located at address FFFF0, by using a Jump command to the beginning of the BIOS chip (usually F0000 or E0000). The CPU executes the BIOS code, initializes the hardware and loads DiskOnChip G3 software using the BIOS expansion search routine (e.g. D0000). Refer to Section 8.2 for a detailed explanation on the boot sequence in PC-compatible platforms.

DiskOnChip G3 implements both disk and boot functions when it replaces the BIOS chip. To enable this, DiskOnChip G3 requires a location at two different addresses:

- After power-up, DiskOnChip G3 must be mapped in F segment, so that the CPU fetches the reset vector from address FFFF0, where DiskOnChip G3 is located.
- After the BIOS code is loaded into RAM and starts execution, DiskOnChip G3 must be reconfigured to be located in the BIOS expansion search area (e.g. D0000) so it can load the TrueFFS software.

This means that the CS# signal must be remapped between two different addresses. For further information on how to achieve this, refer to application note AP-DOC-047, *Designing DiskOnChip as a Flash Disk and Boot Device Replacement*.

8.3.2 Non-PC Architectures

In non-PC architectures, the boot code is executed from a boot ROM, and the drivers are usually loaded from the storage device.

When using DiskOnChip G3 as the system boot device, the CPU fetches the first instructions from the DiskOnChip G3 Programmable Boot Block, which contains the IPL. Since in most cases this block cannot hold the entire boot loader, the IPL runs minimum initialization, after which the Secondary Program Loader (SPL) is copied to RAM from flash. The remainder of the boot loader code then runs from RAM.

The SPL is located in a separate (binary) partition on DiskOnChip G3, and can be hardware protected if required. .

8.3.3 Asynchronous Boot Mode

Platforms that host CPUs that wake up in MultiBurst mode should use Asynchronous Boot mode when using DiskOnChip G3 as the system boot device.

During platform initialization, certain CPUs wake up in 32-bit mode and issue instruction fetch cycles continuously. An XScale CPU, for example, initiates a 16-bit read cycle, but after the first word is read, it continues to hold CE# and OE# asserted while it increments the address and reads additional data as a burst. A StrongARM CPU wakes up in 32-bit mode and issues double-word instruction fetch cycles.

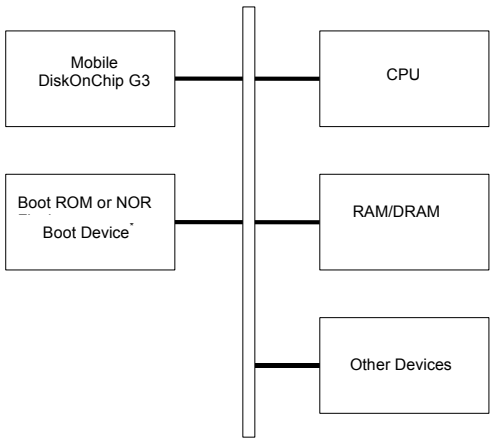
Once in Asynchronous Boot mode, the CPU can fetch its instruction cycles from the DiskOnChip G3 Programmable Boot Block. After reading from this block and completing boot, DiskOnChip G3 returns to derive its internal clock signal from the CE#, OE#, and WE# inputs. Please refer to Section 10.3 for read timing specifications for Asynchronous Boot mode.

9. DESIGN CONSIDERATIONS

9.1 General Guidelines

A typical RISC processor memory architecture is shown in Figure 12. It may include the following devices:

- **DiskOnChip G3**: Contains the OS image, applications, registry entries, back-up data, user files and data, etc. It can also be used to perform boot operation, thereby replacing the need for a separate boot device.
- **CPU**: DiskOnChip G3 is compatible with all major CPUs in the mobile phone, Digital TV (DTV) and Digital Still Camera (DSC) markets, including:
  - ARM-based CPUs
  - Texas Instruments OMAP
  - Intel StrongARM SA-1100/1 and XScale
  - Emblaze ER4525 application processor
  - Renesas SH mobile
  - SuperH SH-3/4
  - Motorola PowerPC MPC8xx and DragonBall MX1
  - Philips PR31700
  - NEC VRSeries VR3/4xxxx
- **Boot Device**: ROM or NOR flash that contains the boot code required for system initialization, kernel relocation, loading the operating systems and/or other applications and files into the RAM and executing them.
- **RAM/DRAM Memory**: This memory is used for code execution.
- **Other Devices**: A DSP processor, for example, may be used in a RISC architecture for enhanced multimedia support.

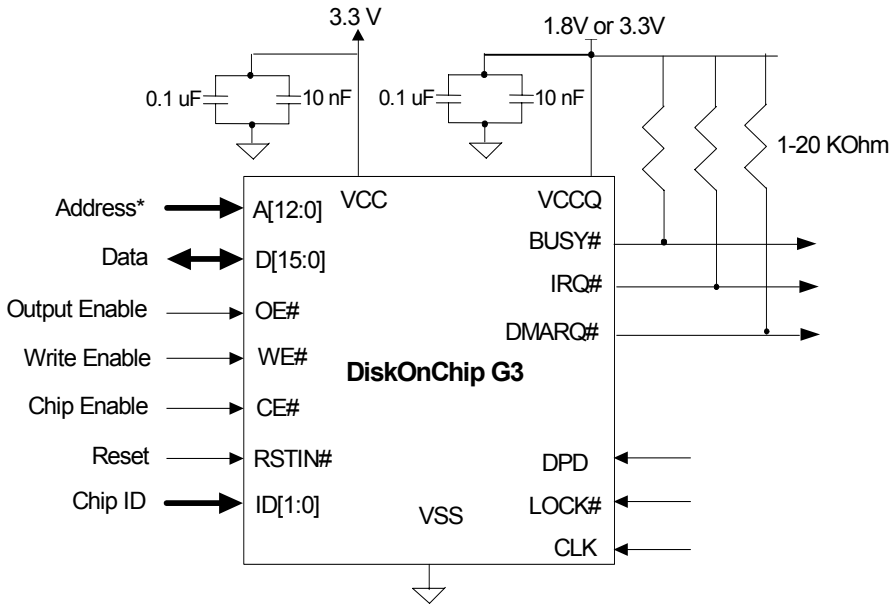


When used as a boot device, DiskOnChip G3 eliminates the need for a dedicated boot ROM/NOR device.

Figure 12: Typical System Architecture Using DiskOnChip G3

9.2 Standard NOR-Like Interface

DiskOnChip G3 uses a NOR-like interface that can easily be connected to any microprocessor bus. With a standard interface, it requires 13 address lines, 8 data lines and basic memory control signals (CE#, OE#, WE#), as shown in Figure 13 below. Typically, DiskOnChip G3 can be mapped to any free 8KB memory space. In a PC-compatible platform, it is usually mapped into the BIOS expansion area. If the allocated memory window is larger than 8KB, an automatic anti-aliasing mechanism prevents the firmware from being loaded more than once during the ROM expansion search.



(*) Address A0 is multiplexed with the DPD signal.

Figure 13: Standard System Interface

Notes: 1. The 0.1 µF and the 10 nF low-inductance, high-frequency capacitors must be attached to each of the device's VCC and VSS pins/balls. These capacitors must be placed as close as possible to the package leads.

2. DiskOnChip G3 is an edge-sensitive device. CE#, OE#, and WE# should be properly terminated (according to board layout, serial parallel or both terminations) to avoid signal ringing.

9.3 Connecting Control Signals

9.3.1 Standard Interface

When using a standard NOR-like interface, connect the control signals as follows:

- A[12:0] – Connect these signals to the host's address signals (see Section 9.7 for platform-related considerations). Address signal A[0] is multiplexed with the DPD signal.
- D[15:0] – Connect these signals to the host's data signals (see Section 9.7 for platform-related considerations).

- Output Enable (OE#) and Write Enable (WE#) – Connect these signals to the host RD# and WR# signals, respectively.
- Chip Enable (CE#) – Connect this signal to the memory address decoder. Most RISC processors include a programmable decoder to generate various Chip Select (CS) outputs for different memory zones. These CS signals can be programmed to support different wait states to accommodate DiskOnChip G3 timing specifications.
- Power-On Reset In (RSTIN#) – Connect this signal to the host active-low Power-On Reset signal.
- Chip Identification (ID[1:0]) – Connect these signals as shown in Figure 13. Both signals must be connected to VSS if the host uses only one DiskOnChip. If more than one device is being used, refer to Section 9.5 for more information on device cascading.
- Busy (BUSY#) – This signal indicates when the device is ready for first access after reset. It may be connected to an input port of the host, or alternatively it may be used to hold the host in a wait-state condition. The later option is required for hosts that boot from DiskOnChip G3.
- DMARQ# (DMA Request) – Output used to control multi-page DMA operations. Connect this output to the DMA controller of the host platform.
- IRQ# (Interrupt Request) – Connect this signal to the host interrupt.
- Lock (LOCK#) – Connect to a logical **0** to prevent the usage of the protection key to open a protected partition. Connect to logical **1** in order to enable usage of protection keys.
- Deep-Power Down (DPD) – multiplexed with A[0].
- 8/16 Bit Interface Configuration (IF_CFG) – This signal is required for configuring the device for 8- or 16-bit access mode. When negated, the device is configured for 8-bit access mode. When asserted, 16-bit access mode is operative.
- Clock (CLK) – This input is used to support MultiBurst operation when reading flash data. Refer to Section 4.1 for further information on MultiBurst operation.

9.4 Implementing the Interrupt Mechanism

9.4.1 Hardware Configuration

To configure the hardware for working with the interrupt mechanism, connect the IRQ# pin/ball to the host interrupt input.

Note: A nominal 10 KΩ pull-up resistor must be connected to this pin/ball.

9.4.2 Software Configuration

Configuring the software to support the IRQ# interrupt is performed in two stages.

Stage 1

Configure the software so that when the system is initialized, the following steps occur:

1. The correct value is written to the Interrupt Control register to configure DiskOnChip G3 for:
   - Interrupt source: Flash ready, data protection, last byte during DMA has been transferred, or BCH ECC error has been detected (used during multi-page DMA operations).
   - Output sensitivity: Either edge or level-triggered

   Note: Refer to Section 7 for further information on the value to write to this register.
2. The host interrupt is configured to the selected input sensitivity, either edge or level-triggered.
3. The handshake mechanism between the interrupt handler and the OS is initialized.
4. The interrupt service routine to the host interrupt is connected and enabled.

Stage 2

Configure the software so that for every long flash I/O operation, the following steps occur:

1. The correct value is written to the Interrupt Control register to enable the IRQ# interrupt.

   Note: Refer to Section 7 for further information on the value to write to this register.
2. The flash I/O operation starts.
3. Control is returned to the OS to continue other tasks. When the IRQ# interrupt is received, other interrupts are disabled and the OS is flagged.
4. The OS either returns control immediately to the TrueFFS driver, or waits for the appropriate condition to return control to the TrueFFS driver.

9.5 Device Cascading

When connecting DiskOnChip G3 64MB (512Mb) using a standard interface, up to four devices can be cascaded with no external decoding circuitry. Figure 14 illustrates the configuration required to cascade four devices on the host bus (only the relevant cascading signals are included in this figure, although all other signals must also be connected). All pins/balls of the cascaded devices must be wired in common, except for ID0 and ID1. The ID input pins/balls are strapped to VCC or VSS, according to the location of each DiskOnChip. The ID pin/ball values determine the identity of each device. For example, the first device is identified by connecting the ID pins/balls as 00, and the last device by connecting the ID pins/balls as 11. Systems that use only one DiskOnChip G3 64MB (512Mb) must connect the ID pins/balls as 00. Additional devices must be configured consecutively as 01, 10 and 11.

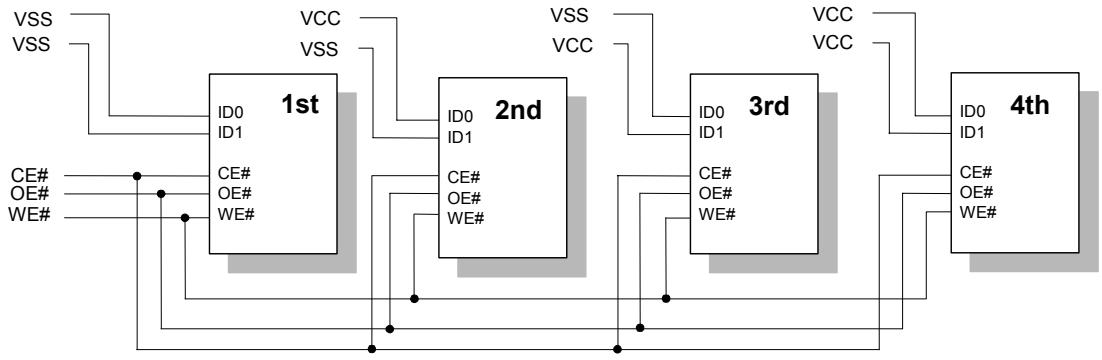


Figure 14: Standard Interface, Cascaded Configuration

Note: When more than one DiskOnChip G3 is cascaded, a boot block of 4KB is available. The Programmable Boot Block of each device is mapped to a unique address space.

9.6 Boot Replacement

A typical RISC architecture uses a boot ROM for system initialization. The boot ROM is also required to access DiskOnChip G3 during the boot sequence in order to load OS images and the device drivers.

M-Systems' Boot Software Development Kit (BDK) and DOS utilities enable full control of DiskOnChip G3 during the boot sequence. For a complete description of these products, refer to the *DiskOnChip Boot Software Development Kit (BDK)* developer guide and the *DiskOnChip Software Utilities* user manual. These tools enable the following operations:

- Formatting DiskOnChip G3
- Creating multiple partitions for different storage needs (OS images files, registry entry files, backup partitions, and FAT partitions)
- Loading the OS image file

Figure 15 illustrates the system boot flow using DiskOnChip G3 in a RISC architecture.

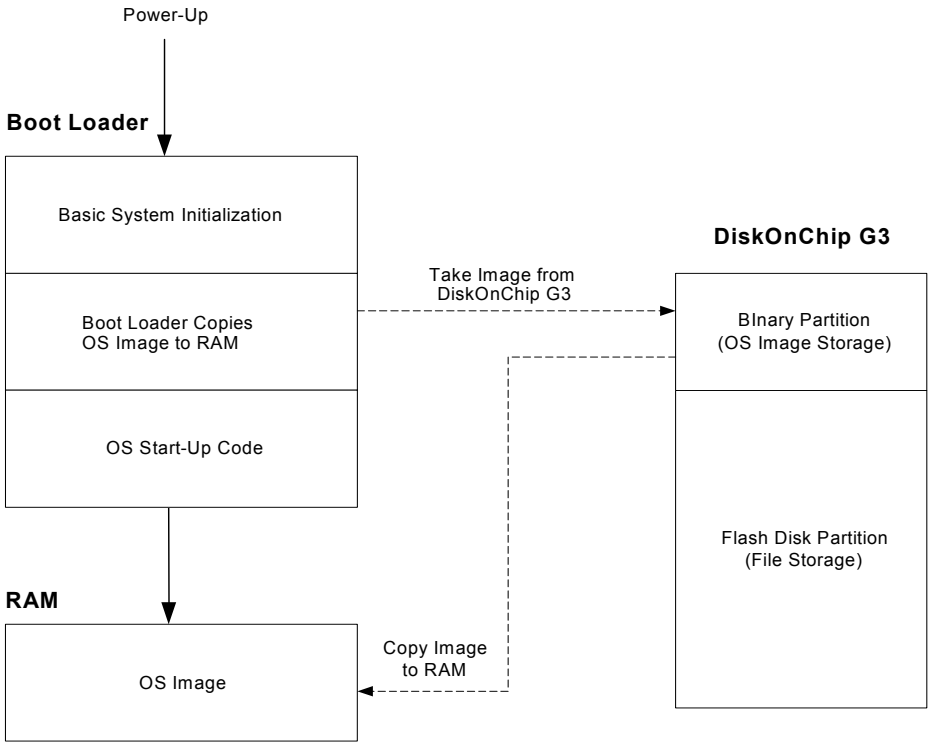


Figure 15: System Boot Flow with DiskOnChip G3

9.7 Platform-Specific Issues

This section discusses hardware design issues for major embedded RISC processor families.

9.7.1 Wait State

Wait states can be implemented only when DiskOnChip G3 is designed in a bus that supports a Wait state insertion, and supplies a WAIT signal.

9.7.2 Big and Little Endian Systems

DiskOnChip G3 is a Little Endian device. Therefore, byte lane 0 (D[7:0]) is its Least Significant Byte (LSB) and byte lane 1 (D[15:8]) is its Most Significant Byte (MSB). Within the byte lanes, bit D0 and bit D8 are the least significant bits of their respective byte lanes. DiskOnChip G3 can be connected to a Big Endian device in one of two ways:

1. Make sure to identify byte lane 0 and byte lane 1 of your processor. Then, connect the data bus so that the byte lanes of the CPU match the byte lanes of DiskOnChip G3. Pay special attention to processors that also change the bit ordering within the bytes (for example, PowerPC). Failing to follow these rules results in improper connection of DiskOnChip G3, and prevents the TrueFFS driver from identifying it.
2. Set the bits SWAPH and SWAPL in the Endian Control register. This enables byte swapping when used with 16-bit hosts.

9.7.3 Busy Signal

The Busy signal (BUSY#) indicates that DiskOnChip G3 has not yet completed internal initialization. After reset, BUSY# is asserted while the IPL is downloaded into the internal boot block and the Data Protection Structures (DPS) are downloaded to the Protection State Machines. Once the download process is completed, BUSY# is negated. It can be used to delay the first access to DiskOnChip G3 until it is ready to accept valid cycles.

Note: DiskOnChip G3 does NOT use this signal to indicate that the flash is in busy state (e.g. program, read, or erase).

9.7.4 Working with 8/16/32-Bit Systems

DiskOnChip G3 uses a 16-bit data bus and supports 16-bit data access by default. However, it can be configured to support 8 or 32-bit data access mode. This section describes the connections required for each mode.

The default of the TrueFFS driver for DiskOnChip G3 is set to work in 16-bit mode. It must be specially configured to support 8 and 32-bit mode. Please see TrueFFS documentation for further details.

Note: The DiskOnChip data bus must be connected to the Least Significant Bits (LSB) of the system. The system engineer must verify whether the matching host signals are SD[7:0], SD[15:8] or D[31:24].

8-Bit (Byte) Data Access Mode

When configured for 8-bit operation, pin/ball IF_CFG should be connected to VSS, and data lines D[15:8] are internally pulled up and may be left unconnected. The controller routes odd and even address accesses to the appropriate byte lane of the flash and RAM.

Host address SA0 must be connected to DiskOnChip G3 A0, SA1 must be connected to A1, etc.

16-Bit (Word) Data Access Mode

To set DiskOnChip G3 to work in 16-bit mode, the IF_CFG pin/ball must be connected to VCC.

In 16-bit mode, the Programmable Boot Block is accessed as a true 16-bit device. It responds with the appropriate data when the CPU issues either an 8-bit or 16-bit read cycle. The flash area is accessed as a 16/32-bit device, regardless of the interface bus width. This has no affect on the design of the interface between DiskOnChip G3 and the host. The TrueFFS driver handles all issues regarding moving data in and out of DiskOnChip G3.

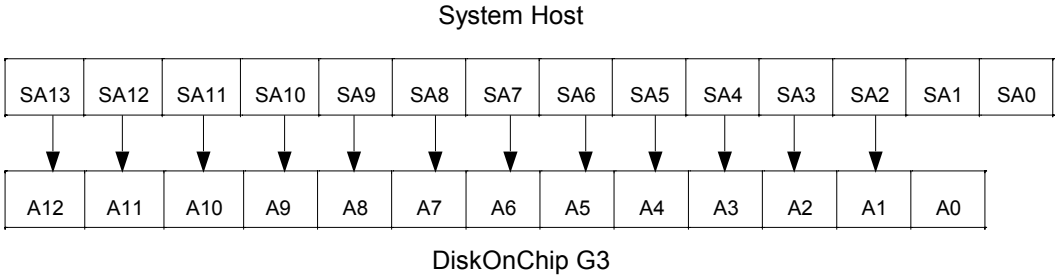
See Table 3 for A0 and IF_CFG settings for various functionalities with 8/16-bit data access.

Table 3: Active Data Bus Lines in 8/16-Bit Configuration

A0	IF_CFG	Functionality
0	1	16-bit access through both buses
0	0	8-bit access to even bytes through low 8-bit bus
1	0	8-bit access to odd bytes through low 8-bit bus
1	1	Illegal

32-Bit (Double Word) Data Access Mode

In a 32-bit bus system that cannot execute byte- or word-aligned accesses, the system address lines SA0 and SA1 are always 0. Consecutive double words (32-bit words) are differentiated by SA2 toggling. Therefore, in 32-bit systems that support only 32-bit data access cycles, DiskOnChip G3 signal A0 is connected to VSS and A1 is connected to the first system address bit that toggles; i.e., SA2.



Note: The prefix "S" indicates system host address lines

Figure 16: Address Shift Configuration for 32-Bit Data Access Mode

9.8 Design Environment

DiskOnChip G3 provides a complete design environment consisting of:

- Evaluation boards (EVBs) for enabling software integration and development with DiskOnChip G3, even before the target platform is available.
- Programming solutions:
  - GANG programmer
  - Programming house
  - On-board programming
- TrueFFS Software Development Kit (SDK) and Boot Software Development Kit (BDK)
- DOS utilities:
  - DFORMAT
  - DIMAGE
  - DINFO
- Documentation:
  - Data sheet
  - Application notes
  - Technical notes
  - Articles
  - White papers

Please visit the M-Systems website (www.m-systems.com) for the most updated documentation, utilities and drivers.

10. PRODUCT SPECIFICATIONS

10.1 Environmental Specifications

10.1.1 Operating Temperature

Commercial temperature range: 0°C to +70°C

Extended temperature range: -40°C to +85°C

10.1.2 Thermal Characteristics

Table 4: Thermal Characteristics

Thermal Resistance (°C/W)	
Junction to Case (θ_{JC}): 30	Junction to Ambient (θ_{JA}): 85

10.1.3 Humidity

10% to 90% relative, non-condensing

10.1.4 Endurance

DiskOnChip G3 is based on MLC NAND flash technology, which guarantees a minimum of 100,000 erase cycles. Due to the TrueFFS wear-leveling algorithm, the life span of all DiskOnChip products is significantly prolonged. M-Systems' website (www.m-systems.com) provides an online life-span calculator to facilitate application-specific endurance calculations.

10.2 Electrical Specifications

10.2.1 Absolute Maximum Ratings

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Rating1	Unit
VCC	DC core supply voltage	-0.6 to 4.6	V
VCCQ	DC I/O supply voltage	-0.6 to 4.6	V
$T_{1SUPPLY}$	Maximum duration of applying VCCQ without VCC, or VCC without VCCQ	1000	msec
I_{IN}	Input pin/ball current (25 °C)	-10 to 10	mA
V_{IN}[2]	Input pin/ball voltage	-0.6 to VCCQ+0.3V, 4.6V max	V
T_{STG}	Storage temperature	-55 to 150	°C
ESD: Charged Device Model	ESD_{CDM}	1000	V
ESD: Human Body Model	ESD_{HBM}	2000	V

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The voltage on any ball may undershoot to -2.0 V or overshoot to 6.6V for less than 20 ns.
3. When operating DiskOnChip G3 with separate power supplies for VCC and VCCQ, it is recommended to turn both supplies on and off simultaneously. Providing power separately (either at power-on or power-off) can cause excessive power dissipation. Damage to the device may result if this condition persists for more than 1 second.

10.2.2 Capacitance

Table 6: Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input capacitance (64MB/512Mb device)	V_{IN} = 0V		TBD	10	pF
C_{OUT}	Output capacitance (64MB/512Mb device)	V_O = 0V		TBD	10	pF

Capacitance is not 100% tested.

10.2.3 DC Electrical Characteristics over Operating Range

See Table 7 and Table 8 for DC characteristics for VCCQ ranges 1.65-2.0V and 2.5-3.6V I/O, respectively.

Table 7: DC Characteristics, VCCQ = 1.65-2.0V I/O

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC	Core supply voltage		2.5	3.0	3.6	V
VCCQ	Input/Output supply voltage		1.65	1.8	2.00	V
V_{IH}	High-level input voltage		VCCQ – 0.4			V
V_{IL}	Low-level input voltage				0.4	V
V_{OH}	High-level output voltage	I_{OH} = -100 µA	VCCQ – 0.1			V
V_{OL}	Low-level output voltage	D[15:0] I_{OL} = 100 µA			0.1	V
		IRQ#, BUSY#, DMARQ# 4 mA			0.3	V
I_{ILK}	Input leakage current[2] (64MB/512Mb device)				±10	µA
I_{IOLK}	Output leakage current (64MB/512Mb device)				±10	µA
I_{CC}	Active supply current[1]	Read Program Erase Cycle Time = 100 ns		4.2 7.2 7.2	25	mA
I_{CCS}	Standby supply current, (64MB/512Mb device)	Deep Power-Down mode[3]		10	40	µA

1. VCC = 3V, VCCQ = 1.8V, Outputs open
2. The CE# input includes a pull-up resistor which sources 0.3~1.4 (TBD) uA at Vin=0V
3. Deep Power-Down mode is achieved by asserting RSTIN# (when in Normal mode) or writing the proper write sequence to the DiskOnChip registers, and asserting the CE# input = VCCQ.

Table 8: DC Characteristics, VCCQ = 2.5V-3.6V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC	Core supply voltage		2.5	3.3	3.6	V
VCCQ	Input/Output supply voltage		2.5	3.3	3.6	V
V_{IH}	High-level input voltage		2.1			V
V_{IL}	Low-level input voltage				0.7	V
I_{OHmax}	Maximum high level output	3.0V < VCCQ < 3.6V	-4			mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	current	2.5V < VCCQ < 3.0V	-4			mA
I_{OLmax}	Maximum low-level output current	3.0V < VCCQ < 3.6V	8			mA
		2.5V < VCCQ < 3.0V	5			mA
I_{ILK}	Input leakage current[2] (64MB/512Mb device)				±10	µA
I_{IOLK}	Output leakage current (64MB/512Mb device)				±10	µA
V_{OH}	High-level output voltage	$I_{OH} = I_{Ohmax}$ 2.5V < VCCQ < 2.7V	VCCQ-0.3			V
		$I_{OH} = I_{Ohmax}$ 2.5V < VCCQ < 3.6V	2.4			
V_{OL}	Low-level output voltage	$I_{OL} = I_{OLmax}$			0.4	V
I_{CC}	Active supply current[1]	Read Program Erase Cycle Time = 100 ns		4.2 7.2 7.2	25	mA
I_{CCS}	Standby supply current, (64MB/512Mb single-die device)	Deep Power-Down mode[3]		10	40	µA

1. VCC = VCCQ = 3.3V, Outputs open
2. The CE# input includes a pull-up resistor which sources 0.3~1.4 (TBD) µA at Vin=0V
3. Deep Power-Down mode is achieved by asserting RSTIN# (when in Normal mode) or writing the proper write sequence to the DiskOnChip registers, and asserting the CE# input = VCCQ.

10.2.4 AC Operating Conditions

Timing specifications are based on the conditions defined below.

Table 9: AC Characteristics

Parameter	VCCQ = 1.65-2.0V	VCCQ = 2.5-3.6V
Ambient temperature (TA)	-40°C to +85°C	-40°C to +85°C
Core supply voltage (VCC)	2.5V to 3.6V	2.5V to 3.6V
Input pulse levels	0.2/VCCQ-0.2V	0V/2.5V
Input rise and fall times	3 ns	3 ns
Input timing levels	0.9V	1.5V
Output timing levels	0.9V	1.5V
Output load	30 pF	100 pF

10.3 Timing Specifications

10.3.1 Read Cycle Timing Standard Interface

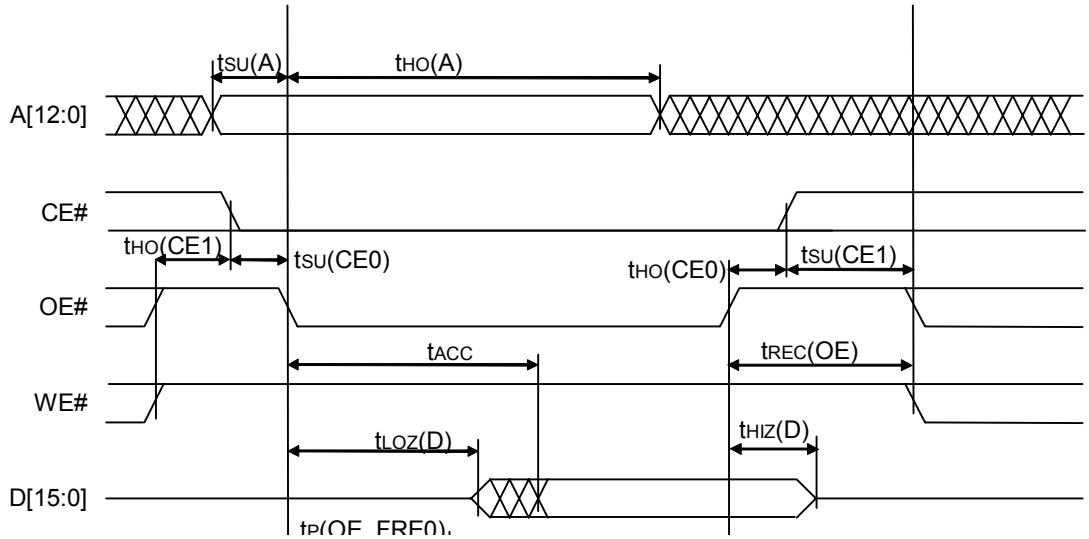


Figure 17: Standard Interface, Read Cycle Timing

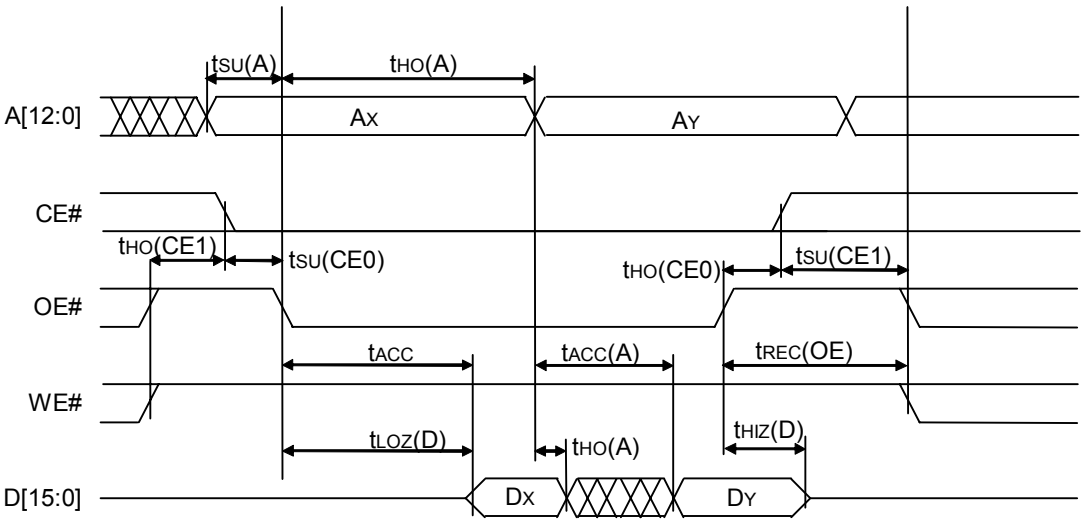


Figure 18: Standard Interface Read Cycle Timing – Asynchronous Boot Mode

Table 10: Standard Interface Read Cycle Timing Parameters

Symbol	Description		VCCQ=VCC VCC=2.5-3.6V		VCCQ=1.65-2.0V VCC=2.5-3.6V		Units
			Min	Max	Min	Max	
Tsu(A)	Address to OE# ↓ setup time		-5		-5		ns
Tho(A)	OE# ↓ to Address hold time[1]		24		24		ns
Tsu(CE0)	CE# ↓ to OE# ↓ setup time[2]		—		—		ns
Tho(CE0)	OE# ↑ to CE# ↑ hold time[3]		—		—		ns
Tho(CE1)	OE# or WE# ↑ to CE# ↓ hold time		5		5		ns
Tsu(CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time		5		5		ns
Trec(OE)	OE# negated to start of next cycle		20		20		ns
Tacc	Read access time (RAM)[1]	Turbo operation		87		88	ns
		Normal operation		84		85	
	Read access time (all other addresses)[3]	Turbo operation		33		34	
		Normal operation		55		56	
Tloz(D)	OE# ↓ to D driven[4]	Turbo operation	5		5		ns
	OE# ↓ to D driven[4]	Normal operation	14		14		ns
Thiz(D)	OE# ↑ to D Hi-Z delay[4]			TBD		TBD	ns
tacc(A)	RAM Read access time from A[9:0]	Asynchronous Boot mode		76		77	ns
tho(A-D)	Data hold time from A[9:0] (RAM)	Asynchronous Boot mode	0		0		ns

1. Add 260 ns on the first read cycle when exiting Power-Down mode. See Section 6.3 for more information.
2. CE# may be asserted any time before or after OE# is asserted. If CE# is asserted after OE#, all timing relative to when OE# was asserted will be referenced to the time CE# was asserted.
3. CE# may be negated any time before or after OE# is negated. If CE# is negated before OE#, all timing relative to when OE# was negated will be referenced to the time CE# was negated.
4. No load (C_L = 0 pF).

10.3.2 Write Cycle Timing Standard Interface

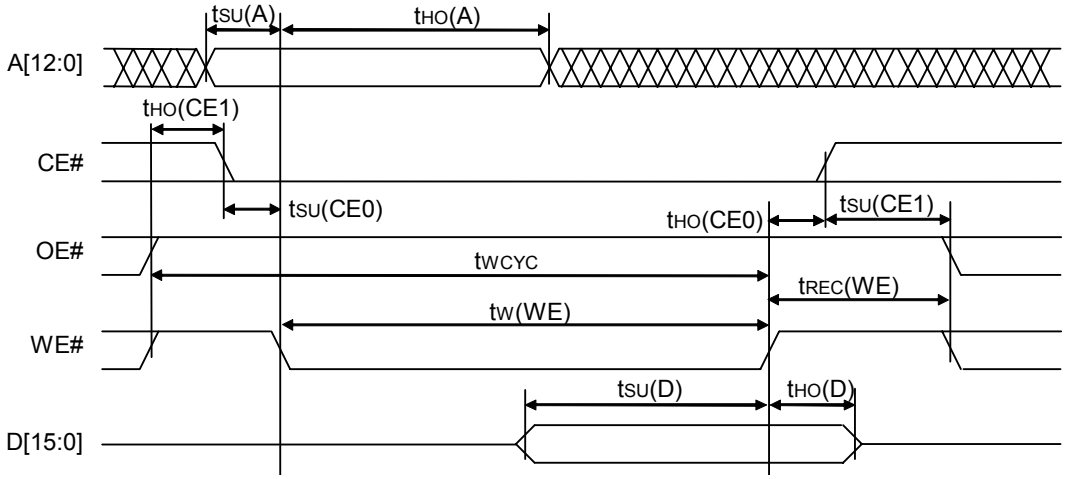


Figure 19: Standard Interface Write Cycle Timing

Table 11: Standard Interface Write Cycle Parameters

Symbol	Description	VCCQ=VCC VCC=2.5-3.6V		VCCQ=1.65-2.0V VCC=2.5-3.6V		Units
		Min	Max	Min	Max	
TSU(A)	Address to WE# ↓ setup time	-5		-5		ns
Tho(A)	WE# ↓ to Address hold time	24		24		ns
Tw(WE)	WE# asserted width (RAM)	38		38		ns
	WE# asserted width (all other addresses)	36		36		ns
Tsu(CE0)	CE# ↓ to WE# ↓ setup time[1]	--		--		ns
Tho(CE0)	WE# ↑ to CE# ↑ hold time[2]	--		--		ns
Tho(CE1)	OE# or WE# ↑ to CE# ↓ hold time	5		5		ns
Tsu(CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	5		5		ns
Trec(WE)	WE# ↑ to start of next cycle	20		20		ns
Tsu(D)	D to WE# ↑ setup time	27		27		ns
Tho(D)	WE# ↑ to D hold time	0		0		

1. CE# may be asserted any time before or after WE# is asserted. If CE# is asserted after WE#, all timing relative to WE# asserted should be referenced to the time CE# was asserted.
2. CE# may be negated any time before or after WE# is negated. If CE# is negated before WE#, all timing relative to WE# negated will be referenced to the time CE# was negated.

10.3.3 Read Cycle Timing MultiBurst

In Figure 20, the MultiBurst Control register values are: LATENCY=0, LENGTH=4, CLK_INV=0.

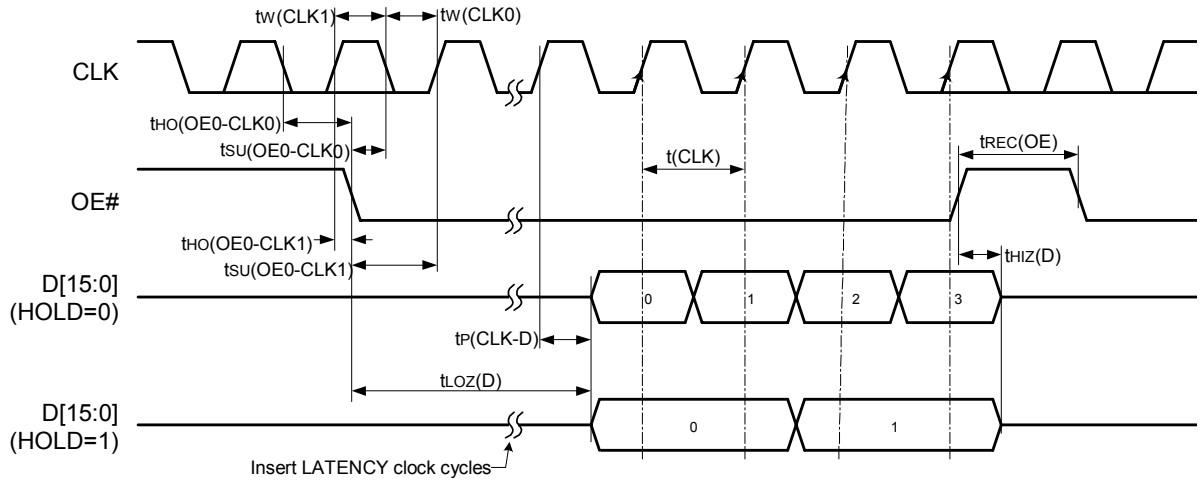


Figure 20: MultiBurst Read Timing

Note: Shown with Burst Mode Controller register values: LATENCY=0, LENGTH=4.

Table 12: MultiBurst Read Cycle Parameters

Symbol	Description		VCCQ=VCC VCC=2.5-3.6V		VCCQ=1.65-2.0V VCC=2.5-3.6V		Units
			Min	Max	Min	Max	
tSU(OE0-CLK1)	OE# ↓ to CLK ↑ setup time[1, 4]		10		10		ns
tSU(OE0-CLK0)	OE# ↓ to CLK ↓ setup time[1, 5]		10		10		ns
tHO(OE0-CLK1)	CLK ↑ to OE# ↓ hold time[1, 4]		1		1		ns
tHO(OE0-CLK0)	CLK ↓ to OE# ↓ hold time[1, 5]		1		1		ns
tP(CLK-D)	CLK ↑ to D delay			26		27	ns
tW(CLK1)	CLK high pulse width[6]		7		7		ns
	CLK high pulse width[7]		7		7		ns
tW(CLK0)	CLK low pulse width[6]		8		8		ns
	CLK low pulse width[7]		8		8		ns
t(CLK)	CLK period[6, 7]		29		30		ns
	CLK period[7]		29		29		ns
tREC(OE)	OE# negated to start of next cycle[2]		9		9		ns
tLOZ(D)	OE# ↓ to D driven[1, 3]	Turbo operation		5		5	ns

Symbol	Description		VCCQ=VCC VCC=2.5-3.6V		VCCQ=1.65-2.0V VCC=2.5-3.6V		Units
			Min	Max	Min	Max	
	OE# ↓ to D driven[1, 3]	Normal operation		14		14	ns
tHIZ(D)	OE# ↑ to D Hi-Z delay[1]			TBD		TBD	ns

1. CE# may be asserted any time before or after OE# is asserted. If CE# is asserted after OE#, all timing relative to OE# asserted will be referenced instead to the time of CE# asserted.
2. CE# may be negated any time before or after OE# is negated. If CE# is negated before OE#, all timing relative to OE# negated will be referenced instead to the time of CE# negated.
3. No load (CL = 0 pF).
4. Applicable only if the CLK_INV bit of the MultiBurst Mode Control register is 0.
5. Applicable only if the CLK_INV bit of the MultiBurst Mode Control register is 1.
6. Applicable only if the HOLD bit of the MultiBurst Mode Control register is 0.
7. Applicable only if the HOLD bit of the MultiBurst Mode Control register is 1
8. 25 nsec cycle time during Burst can be achieved at Vcc=Vccq=2.7~3.6v).

10.3.4 Flash Characteristics

Table 13: Flash Program, Erase, and Read Timing

Symbol	Description	Rate		Units
		Typ	Max	
tPROG	Page programming time	1200	6000	uS
tERASE	Block erasing time	3	10	mS
tREAD	Even Page reading time	32	40	uS
	Odd Page reading time	16	20	uS

10.3.5 Power Supply Sequence

When operating DiskOnChip G3 with separate power supplies powering the VCCQ and VCC rails, it is desirable to turn both supplies on and off simultaneously. Providing power to one supply rail and not the other (either at power-on or power-off) can cause excessive power dissipation. Damage to the device may result if this condition persists for more than 1000 msec.

10.3.6 Power-Up Timing

DiskOnChip G3 is reset by assertion of the RSTIN# input. When this signal is negated, DiskOnChip G3 initiates a download procedure from the flash memory into the internal Programmable Boot Block. During this procedure, DiskOnChip G3 does not respond to read or write accesses.

Host systems must therefore observe the requirements described below for first access to DiskOnChip G3. Any of the following methods may be employed to guarantee first-access timing requirements:

- Use a software loop to wait at least Tp (BUSY1) before accessing the device after the reset signal is negated.
- Poll the state of the BUSY# output.

- Poll the DL_RUN bit of the Download Status register until it returns 0. The DL_RUN bit will be 0 when BUSY# is negated.
- Use the BUSY# output to hold the host CPU in wait state before completing the first access which will be a RAM read cycle. The data will be valid when BUSY# is negated.

Hosts that use DiskOnChip G3 to boot the system must employ option 4 above or use another method to guarantee the required timing of the first-time access.

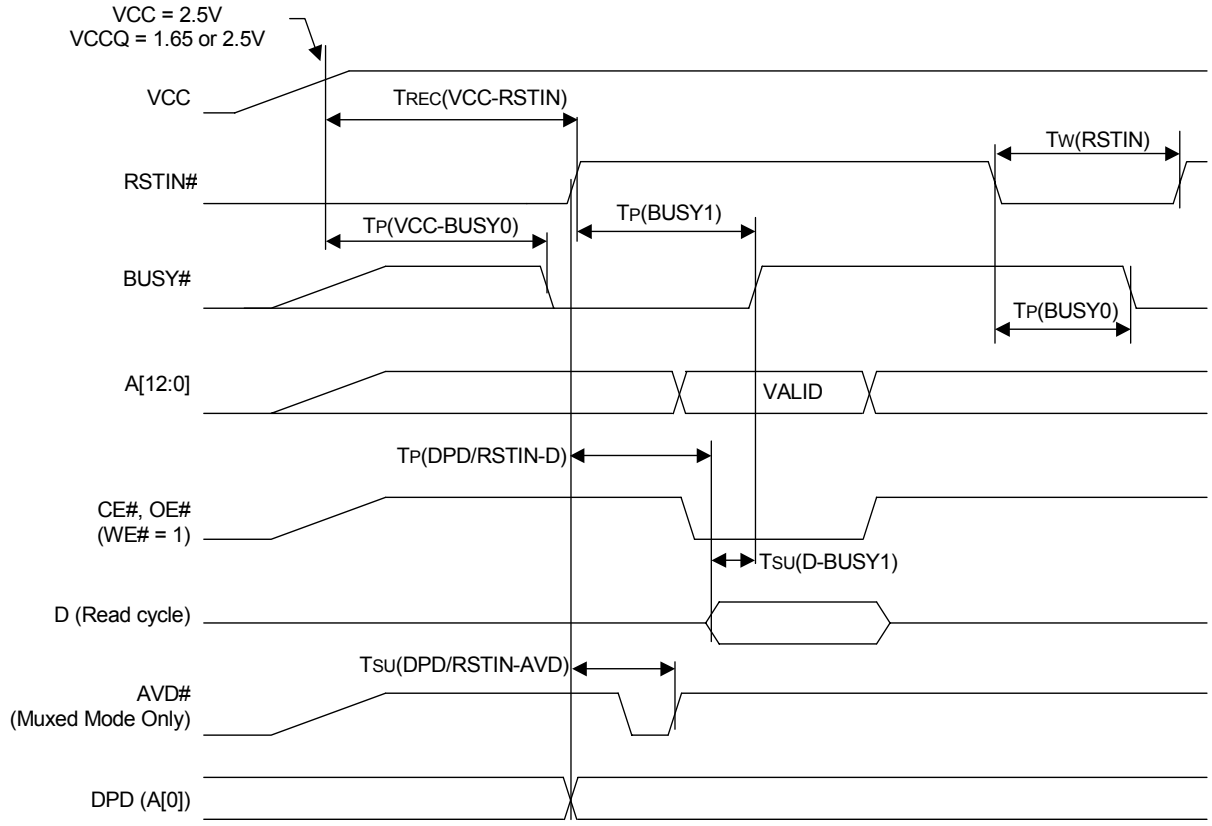


Figure 21: Reset Timing

Table 14: Power-Up Timing Parameters

Symbol	Description	Min	Max	Units
TREC (VCC-RSTIN)	VCC/VCCQ stable to RSTIN# ↑[1]	500		µs
TW (RSTIN)	RSTIN# asserted pulse width	30		ns
TP (BUSY0)	RSTIN# ↓ to BUSY# ↓		50	ns
TP (BUSY1)	RSTIN# ↑ to BUSY# ↑[2]		1055	µs
TSU (D-BUSY1)	Data valid to BUSY# ↑[3]	0		ns
tP(VCC-BUSY0)	VCC/VCCQ stable to BUSY# ↓		500	µs
tSU(DPD/RSTIN-AVD)[4,6]	DPD transition or RSTIN# ↑ to AVD# ↑	600		nS
tP(DPD/RSTIN-D)[5,6]	DPD transition or RSTIN# ↑ to Data valid	660		nS

1. Specified from the final positive crossing of VCC above 2.5V and VCCQ above 1.65 or 2.5V.
2. If the assertion of RSTIN# occurs during a flash erase cycle, this time could be extended by up to 500 µS.
3. Normal read/write cycle timing applies. This parameter applies only when the cycle is extended until the negation of the BUSY# signal.
4. Applies to multiplexed interface only.
5. Applies to SRAM mode only.
6. DPD transition refers to exiting Deep Power Down mode by toggling DPD (A[0]).
7. When operating DiskOnChip G3 with separate power supplies for VCC and VCCQ, it is recommended to turn both supplies on and off simultaneously. Providing power separately (either at power-on or power-off) can cause excessive power dissipation. Damage to the device may result if this condition persists for more than 1 second.

10.3.7 Interrupt Timing

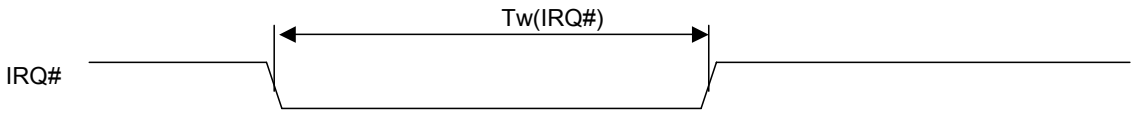
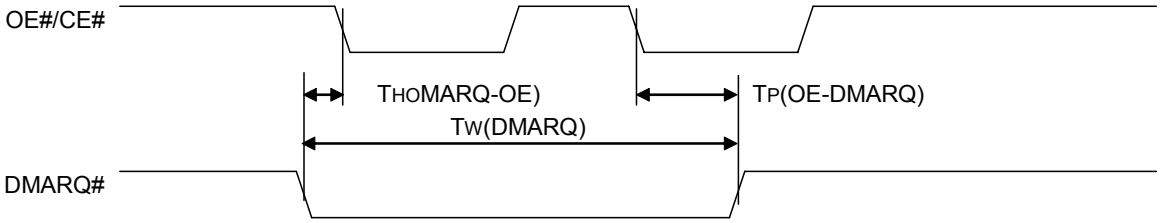


Figure 22: IRQ# Pulse Width in Edge Mode

Table 15: Interrupt Timing

Symbol	Description	Min	Max	Unit
Tw(IRQ#)	IRQ# asserted pulse width (Edge mode)	250	500	nsec

10.3.8 DMA Request Timing



Note: Polarity of DMARQ# may be inverted based on the NORMAL bit of DMA Control Register[0].

Figure 23: DMARQ# Pulse Width

Table 16: DMA Request Timing

Symbol	Description	Min	Max	Unit
Tw(DMARQ#)	DMARQ# asserted pulse width	250	500	nSec
Tho(DMARQ-OE)	DMARQ# asserted to start of cycle	0		nSec
tP(OE-DMARQ)	Start of cycle to DMARQ# negated		TBD	nSec

A. SAMPLE CODE

This appendix provides sample code to verify basic DiskOnChip G3 64MB (512Mb) operations in the system. This code is useful for the initial integration stages.

```
/*--------------------------------------------------------------------*/
/*                 Identify DiskOnChip G3 512Mb(64MB)                 */
/*                                                                    */
/* The target of this sequence is to make sure that DiskOnChip G3     */
/* 64MB (512Mb) is alive and responds to basic commands.              */
/*                                                                    */
/* The sample code will set DiskOnChip in Normal mode, then check     */
/* ChipID, and then Write/Read to the internal SRAM of DiskOnChip     */
/* in order to confirm that the DiskOnChip is connected correctly     */
/*--------------------------------------------------------------------*/


/* Read DiskOnChip G3 512Mb(64MB) ID before setting to Normal mode */
Read from offset 0x1000             /* Data undefined */


/* Set DiskOnChip G3 512Mb(64MB)to Normal mode */
Write 0x0505 to offset 0x100C       /* Write to DiskOnChip Control
Register:Enter normal mode sequence */


Write 0xFAFA to offset 0x1072       /* Write to DiskOnChip
Confirmation Register: Enter normal mode sequence */


Write 0x1000 to offset 0x101A       /* Prepare to read Chip ID[0]
register from address 0x1000 by setting the address of ChipID[0]
register that will be read in the READ address register */


Read from offset 0x1000 into temp   /* DiskOnChip ID[0] should be
0x0200 */
If temp!=0x0200 return (FALSE)


Write 0x1074 to offset 0x101A       /* Prepare to read Chip ID[1]
register from address 0x1074 by setting the address of ChipID[1]
register that will be read in the READ address register */
```

```
Read from offset 0x1074 into temp   /* DiskOnChip ID[1] should be
0xFDFF */
If temp!=0xFDFF return (FALSE)


/* Write and Read Data from IPL area of DiskOnChip G3 512Mb(64MB) */
for(i=0; i < 0x800; i+=2)           /* write/read cycle, 0x800 - IPL
size */
{
Write i to offset i                 /* write content of counter i at
offset i */
Read from offset i into temp        /* read data from same offset */
         If temp!= i return (FALSE) /* ERROR */
   }


/*-----------------------------------------------------------------*/
```

B. Low Power SDRAM 128Mbit Data Sheet

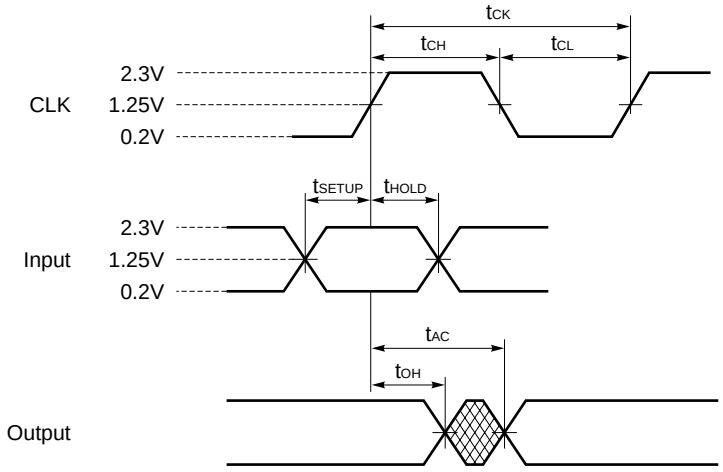
128 Mbits Low Power Synchronous Dynamic RAM

Organization ： 2M words ×16 bits ×4 banks

AC Characteristics (TA = –25 to +85°C, VDD, VDDQ = 2.8V ± 0.2V, VSS, VSSQ = 0V)

Test Conditions

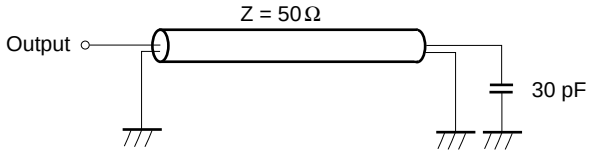
-
- AC high level input voltage / low level input voltage: 2.3 / 0.2V
- Input timing measurement reference level: 1.25V
- Transition time (Input rise and fall time): 1ns
- Output timing measurement reference level: 1.25V



Synchronous Characteristics

Parameter	Symbol	min.	max.	Unit	Note
Clock cycle time (CL= 2)	tCK2	10	—	ns	
(CL= 3)	tCK3	7.5	—	ns	
Access time from CLK (CL= 2)	tAC2	—	6	ns	1
(CL= 3)	tAC3	—	5.4	ns	1
CLK high level width	tCH	2.5	—	ns	
CLK low level width	tCL	2.5	—	ns	
Data-out hold time	tOH	2.5	—	ns	1
Data-out low-impedance time	tLZ	0	—	ns	
Data-out high-impedance time (CL= 2)	tHZ2	2.5	6	ns	
(CL= 3)	tHZ3	2.5	5.4	ns	
Data-in setup time	tDS	1.5	—	ns	
Data-in hold time	tDH	0.8	—	ns	
Address setup time	tAS	1.5	—	ns	
Address hold time	tAH	0.8	—	ns	
CKE setup time	tCKS	1.5	—	ns	
CKE hold time	tCKH	0.8	—	ns	
CKE setup time (Power down exit)	tCKSP	1.5	—	ns	
Command (/CS, /RAS, /CAS, /WE, UDQM, LDQM) setup time	tCMS	1.5	—	ns	
Command (/CS, /RAS, /CAS, /WE, UDQM, LDQM) hold time	tCMH	0.8	—	ns	

Note: 1. Output load.



Output load

Asynchronous Characteristics

Parameter	Symbol	min.	max.	Unit	Notes
ACT to REF/ACT command period (operation)	tRC	67.5	—	ns	
ACT to REF/ACT command period (refresh)	tRC1	67.5	—	ns	
ACT to PRE command period	tRAS	45	120000	ns	
PRE to ACT command period	tRP	15	—	ns	
Delay time ACT to READ/WRITE command	tRCD	20	—	ns	
ACT (one) to ACT (another) command period	tRRD	15	—	ns	
Data-in to PRE command period	tDPL	15	—	ns	
Data-in to ACT (REF) command period (Auto precharge) (CL = 2)	tDAL2	2CLK + 15	—	ns	
(CL = 3)	tDAL3	2CLK + 15	—	ns	
Mode register set cycle time	tRSC	2	—	CLK	
Transition time	tT	0.5	30	ns	
Refresh time (4,096 refresh cycles)	tREF	64	—	ms	

Pin Function

CLK (input pin)

CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.

CKE (input pins)

CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the Mobile RAM suspends operation.

When the Mobile RAM is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.

/CS (input pins)

/CS low starts the command input cycle. When /CS is high, commands are ignored but operations continue.

/RAS, /CAS, and /WE (input pins)

/RAS, /CAS and /WE have the same symbols on conventional DRAM but different functions. For details, refer to the command table.

A0 to A11 (input pins)

Row Address is determined by A0 to A11 at the CLK (clock) rising edge in the active command cycle. It does not depend on the bit organization.

Column Address is determined by A0 to 8 at the CLK rising edge in the read or write command cycle.

A10 defines the precharge mode. When A10 is high in the precharge command cycle, all banks are precharged; when A10 is low, only the bank selected by BA0 and BA1 is precharged.

When A10 is high in read or write command cycle, the precharge starts automatically after the burst access.

BA0 and BA1 (input pin)

BA0 and BA1 are bank select signal. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank A	L	L
Bank B	H	L
Bank C	L	H
Bank D	H	H

Remark: H: VIH. L: VIL. ×: VIH or VIL

UDQM and LDQM (input pins)

UDQM and LDQM control upper byte and lower byte I/O buffers, respectively. In read mode, DQM controls the output buffers like a conventional /OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.

DQ0 to DQ15 (input/output pins)

DQ pins have the same function as I/O pins on a conventional DRAM.

VDD, VSS, VDDQ, VSSQ (Power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

Command Operation

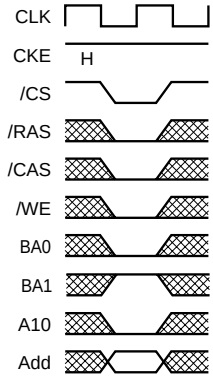
Extended Mode register set command (/CS, /RAS, /CAS, /WE, BA0 = Low, BA1 = High)

The Mobile RAM has an extended mode register that defines low power functions. In this command, A0 through A11 are the data input pins.

After power on, the extended mode register set command must be executed to fix low power functions.

The extended mode register can be set only when all banks are in idle state.

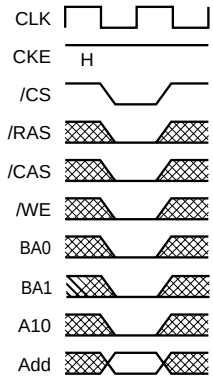
During tRSC following this command, the Mobile RAM can not accept any other commands.



Extended Mode register set command

Mode register set command (/CS, /RAS, /CAS, /WE, BA0, BA1 = Low)

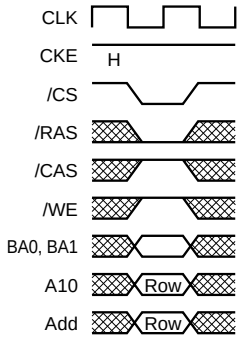
The Mobile RAM has a mode register that defines how the device operates. In this command, A0 through A11 are the data input pins. After power on, the mode register set command must be executed to initialize the device. The mode register can be set only when all banks are in idle state. During tRSC following this command, the Mobile RAM cannot accept any other commands.



Mode register set command

Activate command (/CS, /RAS = Low, /CAS, /WE = High)

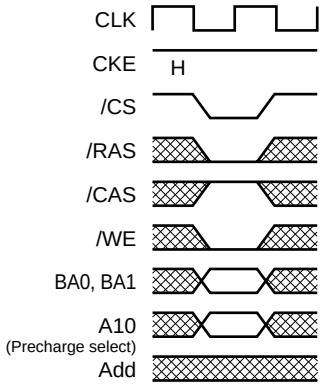
The Mobile RAM has four banks, each with 4,096 rows. This command activates the bank selected by BA0 and BA1 and a row address selected by A0 through A11. This command corresponds to a conventional DRAM's /RAS falling.



Activate command

Precharge command (/CS, /RAS, /WE = Low, /CAS = High)

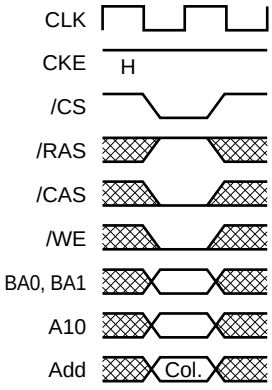
This command begins precharge operation of the bank selected by BA0 and BA1. When A10 is High, all banks are precharged, regardless of BA0 and BA1. When A10 is Low, only the bank selected by BA0 and BA1 is precharged. After this command, the Mobile RAM can't accept the activate command to the precharging bank during tRP (precharge to activate command period). This command corresponds to a conventional DRAM's /RAS rising.



Precharge command

Write command (/CS, /CAS, /WE = Low, /RAS = High)

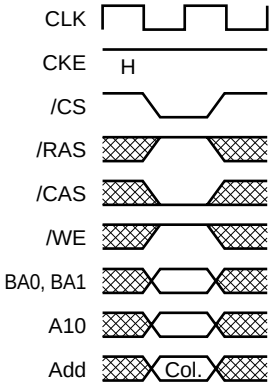
This command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst mode can input with this command with subsequent data on following clocks.



Write command

Read command (/CS, /CAS = Low, /RAS, /WE = High)

Read data is available after /CAS latency requirements have been met. This command sets the burst start address given by the column address.

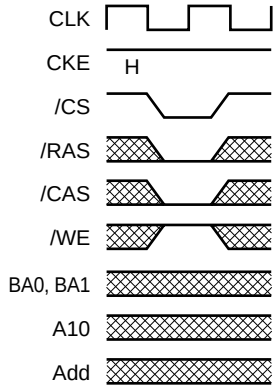


Read command

Auto refresh command (/CS, /RAS, /CAS = Low, /WE, CKE = High)

This command is a request to begin the Auto refresh operation. The refresh address is generated internally.

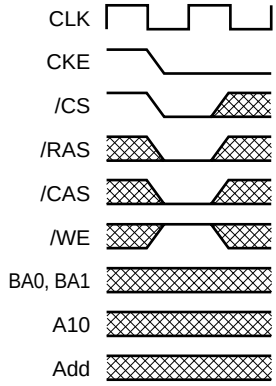
Before executing Auto refresh, all banks must be precharged. After this cycle, all banks will be in the idle (precharged) state and ready for a row activate command. During tRC1 period (from refresh command to refresh or activate command), the Mobile RAM cannot accept any other command



Auto refresh command

Self refresh entry command (/CS, /RAS, /CAS, CKE = Low, /WE = High)

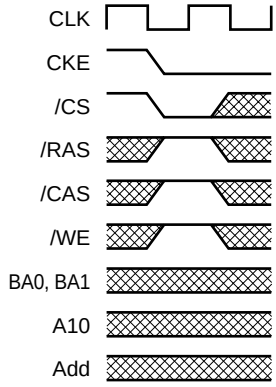
After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the Mobile RAM exits the self refresh mode. During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control. Before executing self refresh, all banks must be precharged.



Self refresh entry command

Power down entry command (/CS, CKE = Low, /RAS, /CAS, /WE = High)

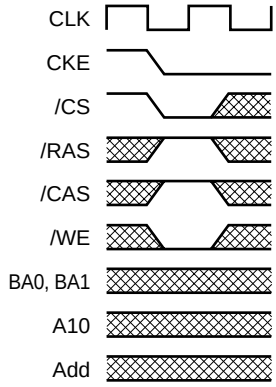
After the command execution, power down mode continues while CKE remains low. When CKE goes high, the Mobile RAM exits the power down mode. Before executing power down, all banks must be precharged.



Power down entry command

Deep power down entry command(/CS, CKE, /WE = Low, /RAS, /CAS = High)

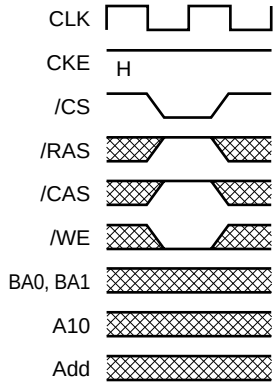
After the command execution, deep power down mode continues while CKE remains low. When CKE goes high, the Mobile RAM exits the deep power down mode. Before executing deep power down, all banks must be precharged.



Deep power down entry command

Burst stop command (/CS = /WE = Low, /RAS, /CAS = High)

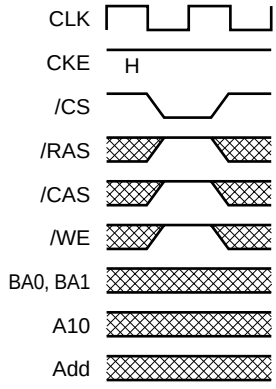
This command can stop the current burst operation.



Burst stop command

No operation (/CS = Low, /RAS, /CAS, /WE = High)

This command is not an execution command. No operations begin or terminate by this command.



No operation

Truth Table

Command Truth Table

Function	Symbol	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	BA1	BA0	A10	A11, A9 - A0
Device deselect	DESL	H	×	H	×	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×	×
Burst stop	BST	H	H	L	H	H	L	×	×	×	×
Read	READ	H	×	L	H	L	H	V	V	L	V
Read with auto precharge	READA	H	×	L	H	L	H	V	V	H	V
Write	WRIT	H	×	L	H	L	L	V	V	L	V
Write with auto precharge	WRITA	H	×	L	H	L	L	V	V	H	V
Bank activate	ACT	H	×	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	V	L	×
Precharge all banks	PALL	H	×	L	L	H	L	×	×	H	×
Mode register set	MRS	H	×	L	L	L	L	L	L	L	V
Extended mode register set	EMRS	H	×	L	L	L	L	H	L	L	V

Remark: H: VIH. L: VIL. ×: VIH or VIL, V = Valid data

DQM Truth Table

Function	Symbol	CKE n – 1	CKE n	DQM U	DQM L
Data write / output enable	ENB	H	×	L	L
Data mask / output disable	MASK	H	×	H	H
Upper byte write enable / output enable	ENBU	H	×	L	×
Lower byte write enable / output enable	ENBL	H	×	×	L
Upper byte write inhibit / output disable	MASKU	H	×	H	×
Lower byte write inhibit / output disable	MASKL	H	×	×	H

Remark: H: VIH. L: VIL. ×: VIH or VIL

CKE Truth Table

Current state	Function	Symbol	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	Address
Activating	Clock suspend mode entry		H	L	×	×	×	×	×
Any	Clock suspend mode		L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit		L	H	×	×	×	×	×
Idle	Auto refresh command	REF	H	H	L	L	L	H	×
Idle	Self refresh entry	SELF	H	L	L	L	L	H	×
Idle	Power down entry	PD	H	L	L	H	H	H	×
			H	L	H	×	×	×	×
Idle	Deep power down entry	DPD	H	L	L	H	H	L	×
Self refresh	Self refresh exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Power down	Power down exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Deep power down	Deep power down exit		L	H	×	×	×	×	×

Remark: H: VIH. L: VIL. ×: VIH or VIL

Function Truth Table

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Idle	H	×	×	×	×	DESL	Nop	
	L	H	H	H	×	NOP	Nop	
	L	H	H	L	×	BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	→ Row activating	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	×	REF	Auto refresh	
	L	L	L	L	OC, BA1= L	MRS	Mode register set	
	L	L	L	L	OC, BA1= H	EMRS	Extended mode register set	
Row active	H	×	×	×	×	DESL	Nop	
	L	H	H	H	×	NOP	Nop	
	L	H	H	L	×	BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read	3
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin write	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Precharge/Precharge all banks	4
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Read	H	×	×	×	×	DESL	Continue burst to end → Row active	
	L	H	H	H	×	NOP	Continue burst to end → Row active	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, begin new read	5
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, begin write	5, 6
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst → Precharging	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write	H	×	×	×	×	DESL	Continue burst to end → Write recovering	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, start read : Determine AP	5, 6
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, new write : Determine AP	5
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst → Precharging	7
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Read with auto	H	×	×	×	×	DESL	Continue burst to end → Precharging	
precharge	L	H	H	H	×	NOP	Continue burst to end → Precharging	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Precharging	H	×	×	×	×	DESL	Nop → Enter idle after tRP	
	L	H	H	H	×	NOP	Nop → Enter idle after tRP	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after tRP	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Row activating	H	×	×	×	×	DESL	Nop → Enter bank active after tRCD	
	L	H	H	H	×	NOP	Nop → Enter bank active after tRCD	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2, 8
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

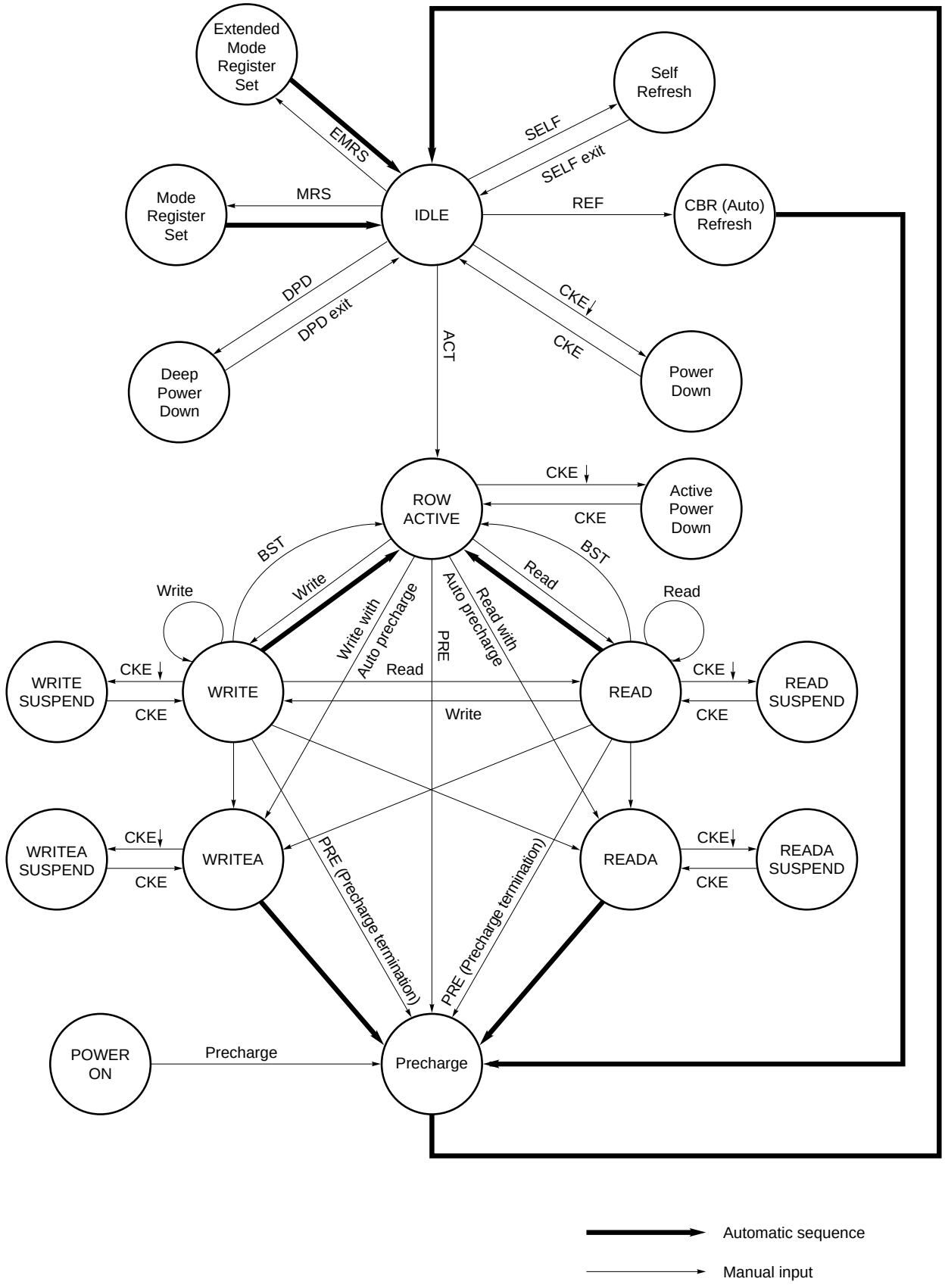
Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Write recovering	H	×	×	×	×	DESL	Nop → Enter row active after tDPL	
	L	H	H	H	×	NOP	Nop → Enter row active after tDPL	
	L	H	H	L	×	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read	6
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin new write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write recovering	H	×	×	×	×	DESL	Nop → Enter precharge after tDPL	
with auto	L	H	H	H	×	NOP	Nop → Enter precharge after tDPL	
precharge	L	H	H	L	×	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2, 6
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Refresh	H	×	×	×	×	DESL	Nop → Enter idle after tRC1	
	L	H	H	H	×	NOP	Nop → Enter idle after tRC1	
	L	H	H	L	×	BST	Nop → Enter idle after tRC1	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Mode register	H	×	×	×	×	DESL	Nop → Enter idle after tRSC	
accessing	L	H	H	H	×	NOP	Nop → Enter idle after tRSC	
	L	H	H	L	×	BST	Nop → Enter idle after tRSC	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Extended mode	H	×	×	×	×	DESL	Nop → Enter idle after tRSC	
register	L	H	H	H	×	NOP	Nop → Enter idle after tRSC	
accessing	L	H	H	L	×	BST	Nop → Enter idle after tRSC	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA0,BA1	MRS/EMRS	ILLEGAL	

Remark: H: VIH. L: VIL. ×: VIH or VIL, V = Valid data
BA: Bank Address, CA: Column Address, RA: Row Address, OC: Op-Code

Notes: 1. All entries assume that CKE is active (CKE_{n-1}=CKE_n=H).
2. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
3. Illegal if tRCD is not satisfied.
4. Illegal if tRAS is not satisfied.
5. Must satisfy burst interrupt condition.
6. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
7. Must mask preceding data which don't satisfy tDPL.
8. Illegal if tRRD is not satisfied.

Simplified State Diagram



Initialization

The synchronous DRAM is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, when power is applied, a 200 μs or longer pause must precede any signal toggling.

(2) After the pause, all banks must be precharged using the Precharge command (The Precharge all banks command is convenient).

(3) Once the precharge is completed and the minimum tRP is satisfied, two or more Auto refresh must be performed.

(4) Both the mode register and the extended mode register must be programmed. After the mode register set cycle or the extended mode register set cycle, tRSC (2 CLK minimum) pause must be satisfied.

Remarks:

1 The sequence of Auto refresh, mode register programming and extended mode register programming above may be transposed.

2 CKE and DQM must be held high until the Precharge command is issued to ensure data-bus High-Z.

Programming Mode Registers

The mode register and extended mode register are programmed by the Mode register set command and Extended mode register command, respectively using address bits A11 through A0, BA0 and BA1 as data inputs. The registers retain data until they are re-programmed, or the device enters into the deep power down or the device loses power.

Mode register

The mode register has three fields;

Options	:	A11 through A7
/CAS latency	:	A6 through A4
Wrap type	:	A3
Burst length	:	A2 through A0

Following mode register programming, no command can be issued before at least 2 CLK have elapsed.

/CAS Latency

/CAS latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available. The value is determined by the frequency of the clock and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become High-Z. The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either “Sequential” or “Interleave”. The method chosen will depend on the type of CPU in the system.

Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. “Burst Length Sequence” shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Additionally, sequence supports the full page length.

Extended Mode Register

The extended mode register has four fields;

Options : A11 through A7
Drive Strength : A6 through A5
Temperature Compensated Self Refresh
: A4 through A3
Partial Array Self Refresh
: A2 through A0

Following extended mode register programming, no command can be issued before at least 2 CLK have elapsed.

Drive Strength

Driving capability of data output drivers.

Temperature Compensated Self Refresh

Programmable refresh rate for self refresh mode to allow the system to control power as a function of temperature.

Partial Array Self Refresh

Memory array size to be refreshed during self refresh operation is programmable in order to reduce power. Data outside the defined area will not be retained during self refresh.

Mode Register Definition

BA0	BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	LTMODE			WT	BL		

Mode Register Set

	Bits6-4	/CAS latency
Latency mode	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

	Bits2-0	WT = 0	WT = 1
Burst length	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type	0	Sequential
	1	Interleave

BA0	BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	DS		TCSR		PASR		

Extended Mode Register Set

	Bits6-5	Strength
Drive Strength	00	Normal
	01	1/2 strength
	10	1/4 strength
	11	R

	Bits2-0	Refresh Array
Partial Array Self Refresh	000	All banks
	001	Bank A & Bank B (BA1=0)
	010	Bank A (BA0=BA1=0)
	011	R
	100	R
	101	R
	110	R
	111	R

	Bits4-3	Max Temperature
Temprature Compensated Self Refresh	00	70°C
	01	45°C
	10	15°C
	11	85°C

Remark R : Reserved

Burst Length and Sequence

[Burst of Two]

Starting address (column address A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

Starting address (column address A1–A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

Starting address (column address A2–A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of sequential addressing, with the length being 512.

Address Bits of Bank-Select and Precharge

Row

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	BA1	BA0

(Activate command)

BA1	BA0	Result
0	0	**Select Bank A “Activate” command**
0	1	**Select Bank B “Activate” command**
1	0	**Select Bank C “Activate” command**
1	1	**Select Bank D “Activate” command**

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	BA1	BA0

(Precharge command)

A10	BA1	BA0	Result
0	0	0	**Precharge Bank A**
0	0	1	**Precharge Bank B**
0	1	0	**Precharge Bank C**
0	1	1	**Precharge Bank D**
1	x	x	**Precharge All Banks**

x : Don’t care

Col.

A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	BA1	BA0

(/CAS strobes)

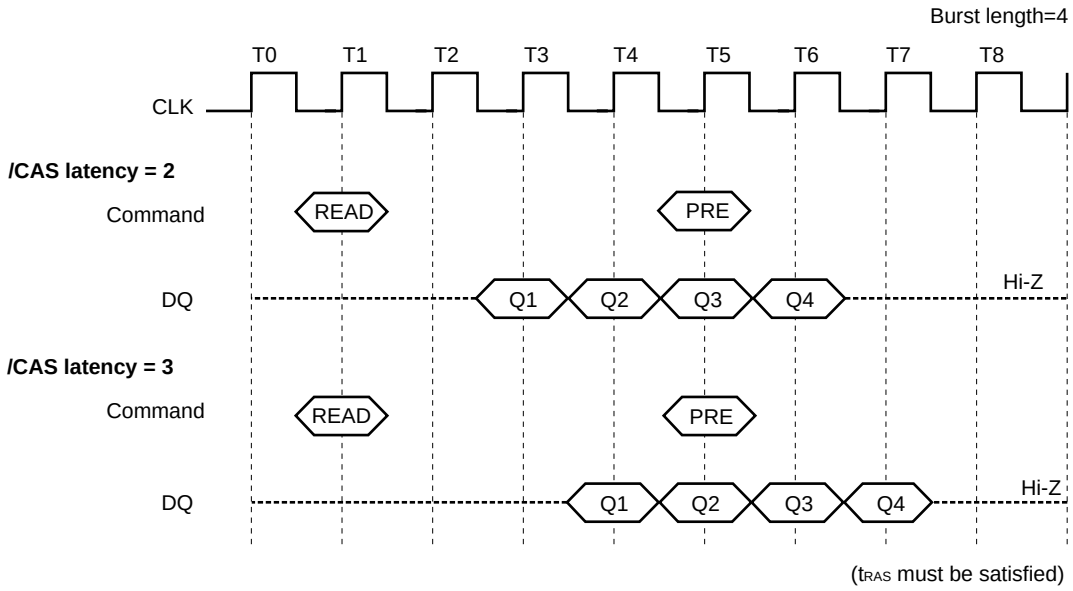
0	**disables Auto-Precharge (End of Burst)**
1	**enables Auto-Precharge (End of Burst)**

BA1	BA0	Result
0	0	**enables Read/Write commands for Bank A**
0	1	**enables Read/Write commands for Bank B**
1	0	**enables Read/Write commands for Bank C**
1	1	**enables Read/Write commands for Bank D**

Operation of the Mobile RAM

Precharge

The precharge command can be issued anytime after tRAS min. is satisfied. Soon after the precharge command is issued, precharge operation performed and the synchronous DRAM enters the idle state after tRP is satisfied. The parameter tRP is the time required to perform the precharge. The earliest timing in a read cycle that a precharge command can be issued without losing any data in the burst is as follows.



Precharge

In order to write all data to the memory cell correctly, the asynchronous parameter tDPL must be satisfied. The tDPL (min.) specification defines the earliest time that a precharge command can be issued. Minimum number of clocks is calculated by dividing tDPL (min.) with clock cycle time. In summary, the precharge command can be issued relative to reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

/CAS latency	Read	Write
2	-1	+tDPL(min.)
3	-2	+tDPL(min.)

Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the Read or Write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically. The tRAS must be satisfied with a read with auto precharge or a write with auto precharge operation. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends.

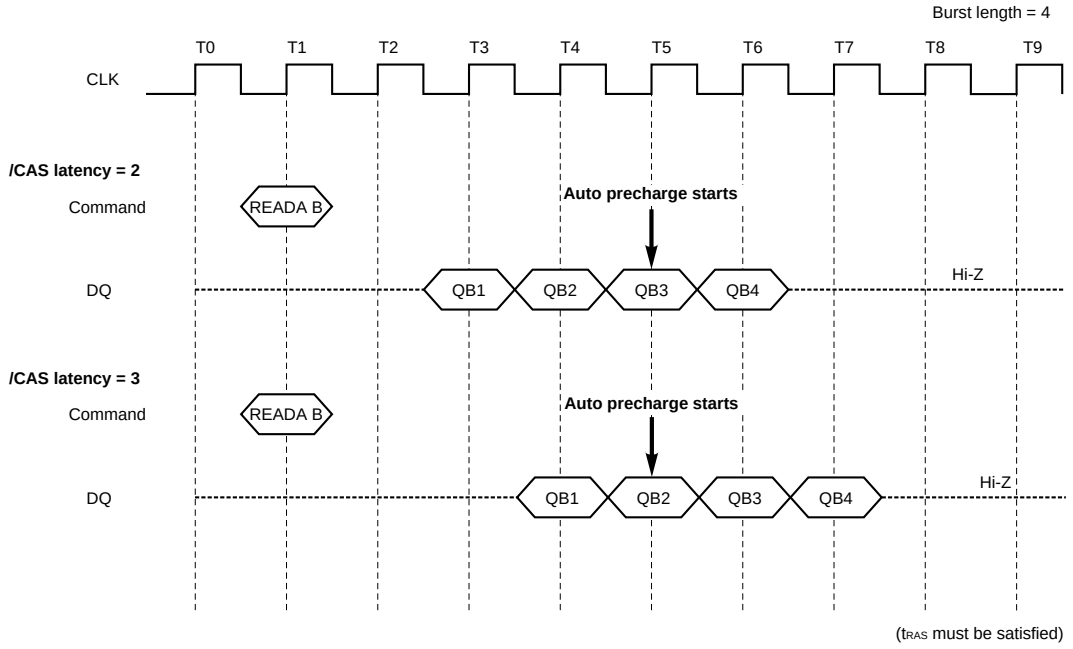
In read cycle, once auto precharge has started, an activate command to the bank can be issued after tRP has been satisfied.

In write cycle, the tDAL must be satisfied to issue the next activate command to the bank being precharged.

The timing that begins the auto precharge cycle depends on whether read or write cycle.

Read with Auto Precharge

During a read cycle, the auto precharge begins one clock earlier (/CAS latency of 2) or two clocks earlier (/CAS latency of 3) the last data word output.

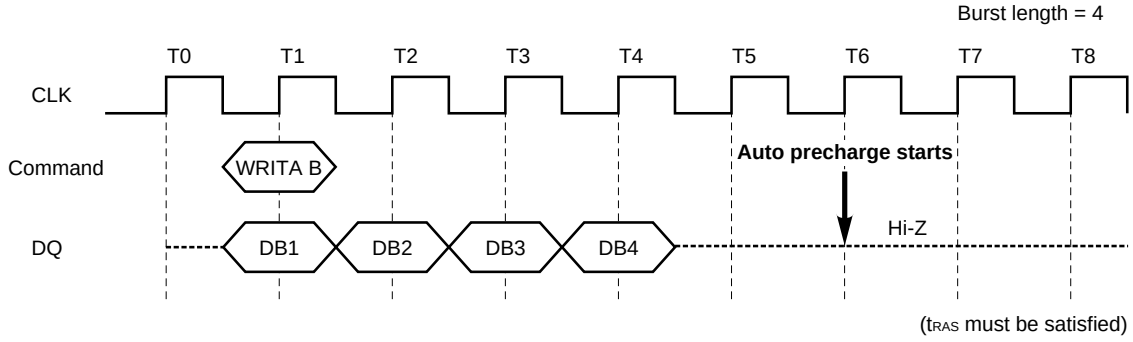


Read with Auto Precharge

Remark: READA means Read with Auto precharge

Write with Auto Precharge

During a write cycle, the auto precharge starts at the timing of 2 clocks after the last data word input to the device.



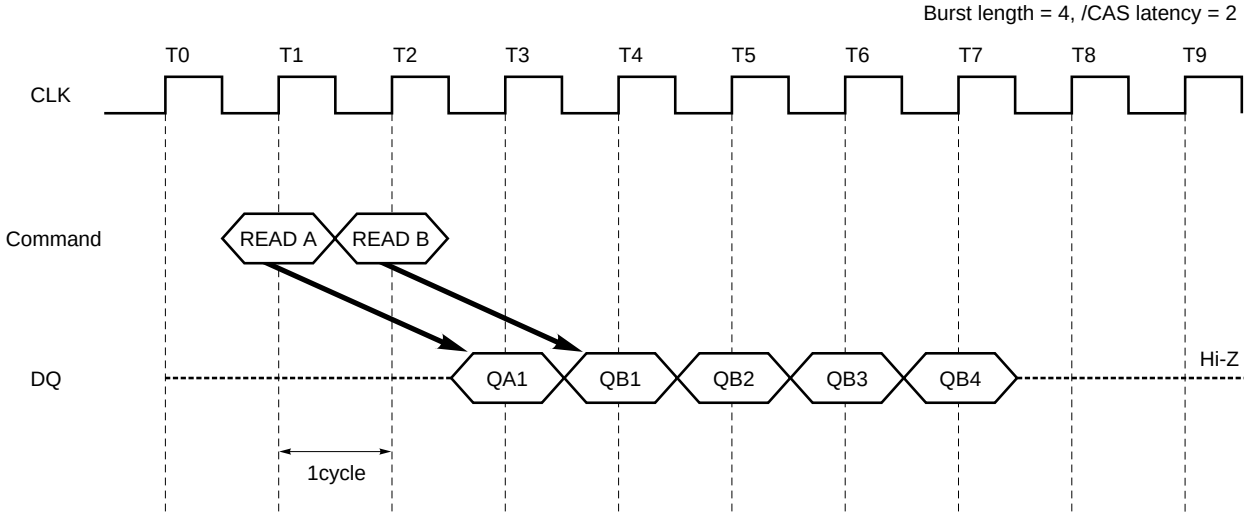
Write with Auto Precharge

Remark: WRITA means Write with Auto Precharge

Read / Write Command Interval

Read to Read Command Interval

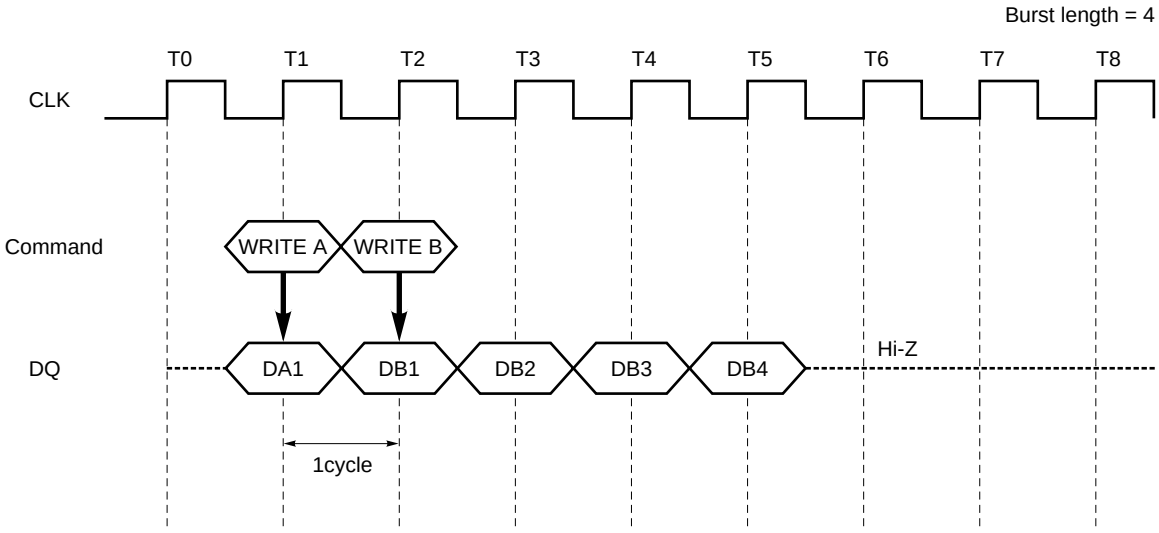
During a read cycle, when new Read command is issued, it will be effective after /CAS latency, even if the previous read operation does not completed. READ will be interrupted by another READ. The interval between the commands is 1 cycle minimum. Each Read command can be issued in every clock without any restriction.



Read to Read Command Interval

Write to Write Command Interval

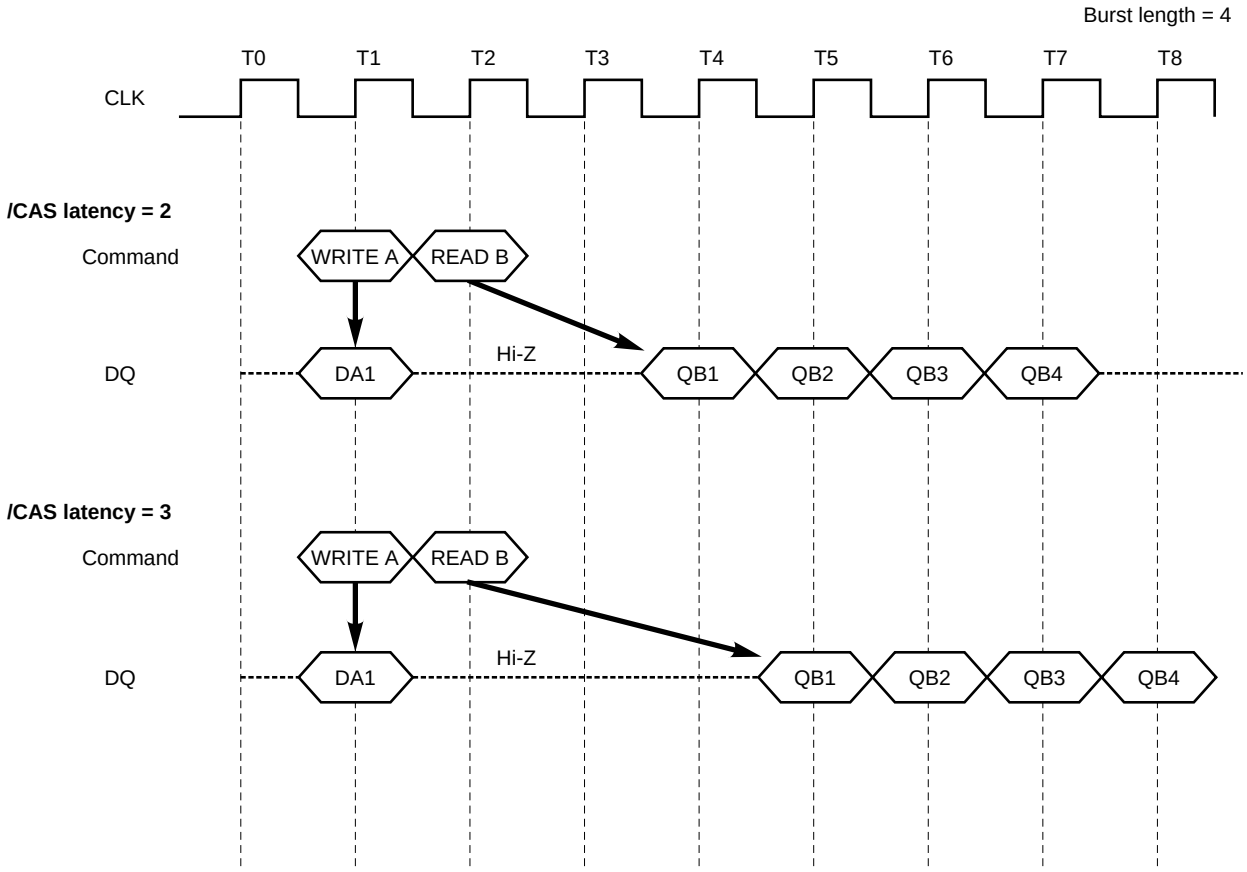
During a write cycle, when a new Write command is issued, the previous burst will terminate and the new burst will begin with a new Write command. WRITE will be interrupted by another WRITE. The interval between the commands is minimum 1 cycle. Each Write command can be issued in every clock without any restriction.



Write to Write Command Interval

Write to Read Command Interval

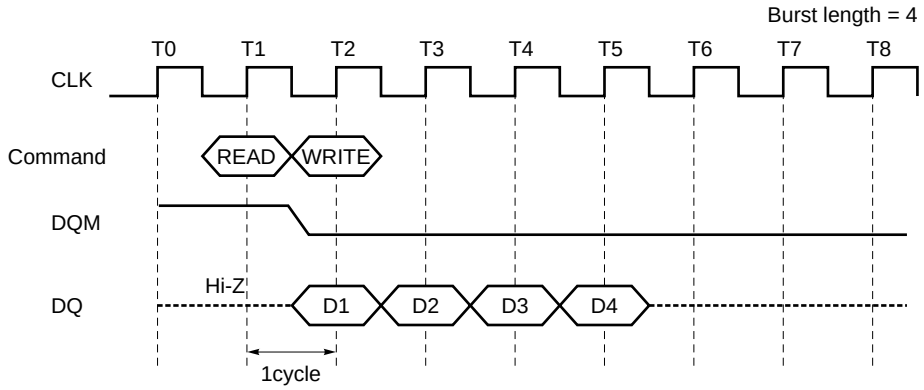
Write command and Read command interval is also 1 cycle. Only the write data before Read command will be written. The data bus must be High-Z at least one cycle prior to the first DOUT.



Write to Read Command Interval

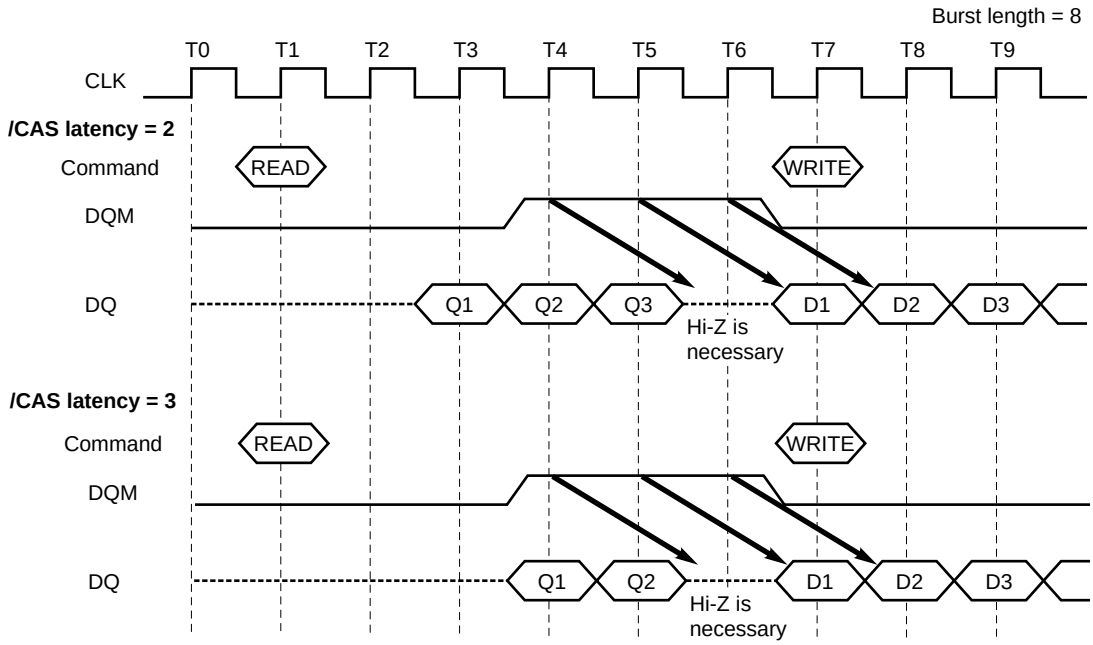
Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE. The Read and Write command interval is 1 cycle minimum. There is a restriction to avoid data conflict. The Data bus must be High-Z using DQM before WRITE.



Read to Write Command Interval 1

READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.



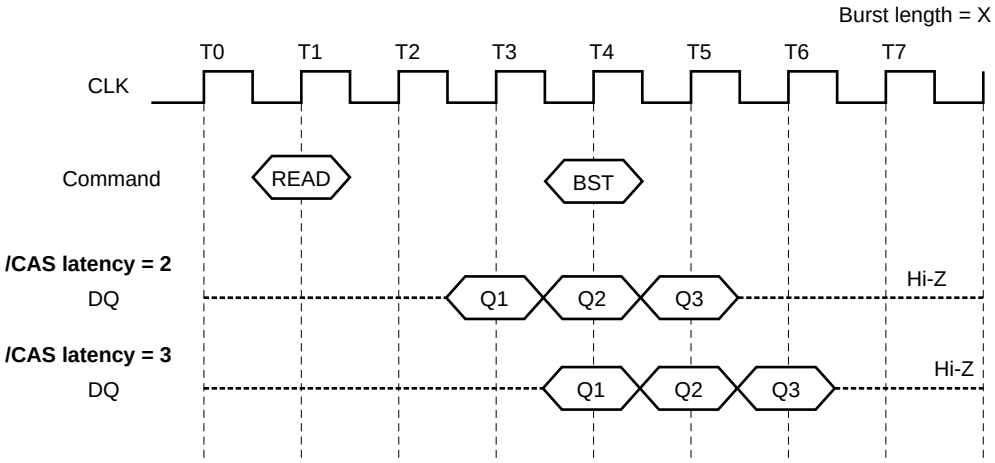
Read to Write Command Interval 2

Burst Termination

There are two methods to terminate a burst operation other than using a Read or a Write command. One is the burst stop command and the other is the precharge command.

Burst Termination in READ Cycle

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to High-Z after the /CAS latency from the burst stop command.

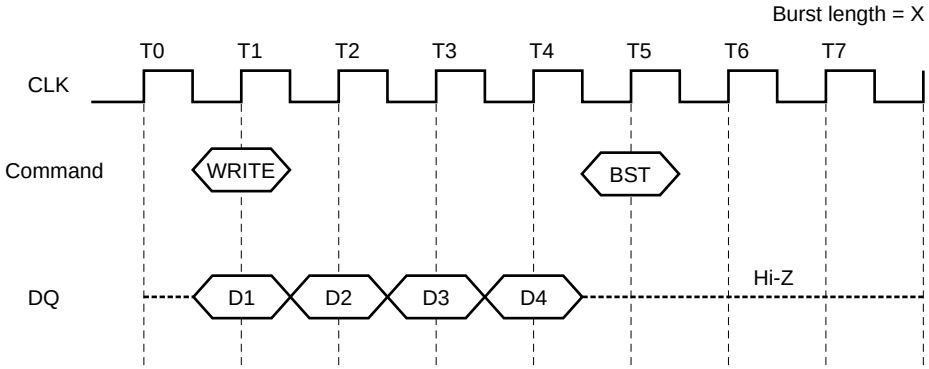


Burst Termination in READ Cycle

Remark: BST: Burst stop command

Burst Termination in WRITE Cycle

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to High-Z at the same clock with the burst stop command.



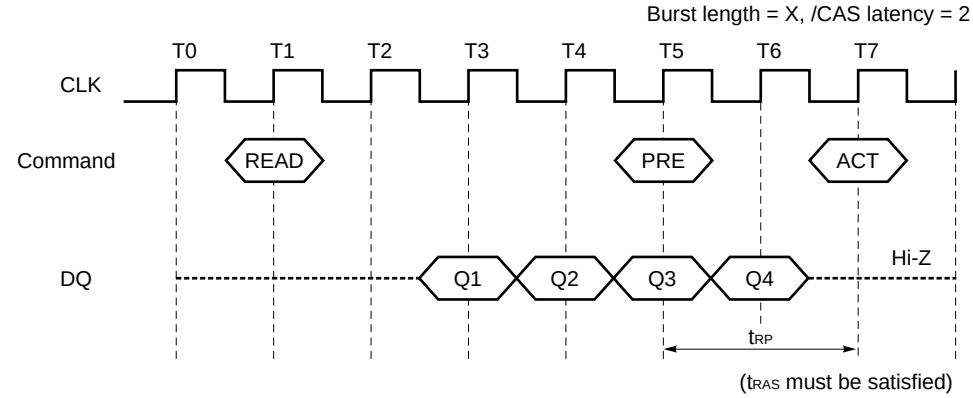
Burst Termination in WRITE Cycle

Remark: BST: Burst stop command

Precharge Termination in READ Cycle

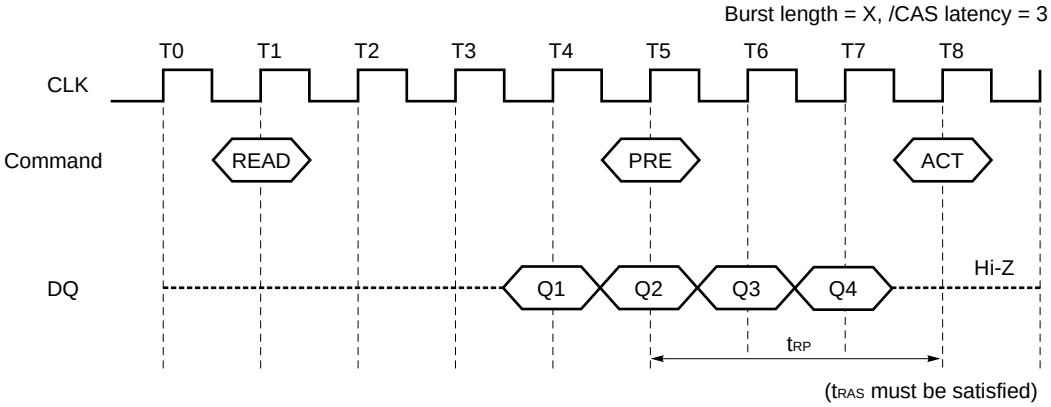
During a read cycle, the burst read operation is terminated by a precharge command. When the precharge command is issued, the burst read operation is terminated and precharge starts. The same bank can be activated again after tRP from the precharge command. To issue a precharge command, tRAS must be satisfied.

When /CAS latency is 2, the read data will remain valid until one clock after the precharge command.



Precharge Termination in READ Cycle (CL = 2)

When /CAS latency is 3, the read data will remain valid until two clocks after the precharge command.

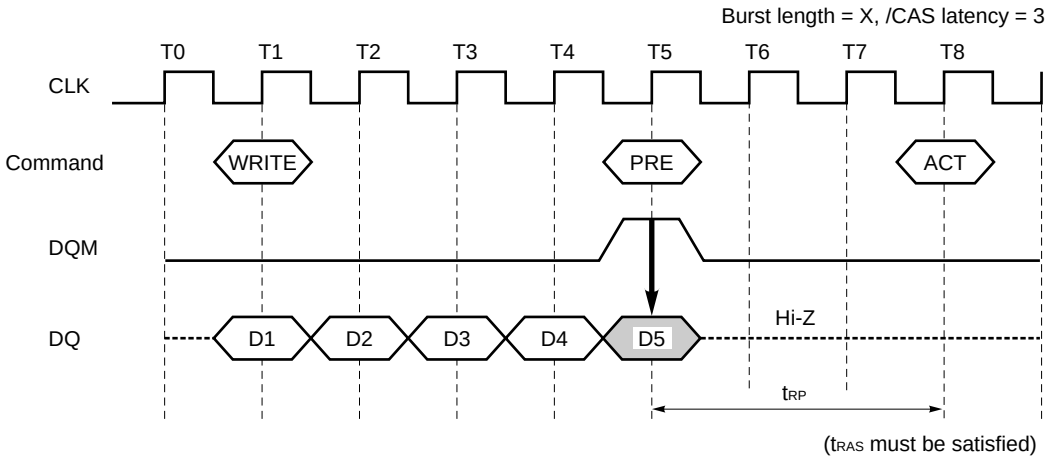


Precharge Termination in READ Cycle (CL = 3)

Precharge Termination in WRITE Cycle

During a write cycle, the burst write operation is terminated by a precharge command. When the precharge command is issued, the burst write operation is terminated and precharge starts. The same bank can be activated again after tRP from the precharge command. To issue a precharge command, tRAS must be satisfied.

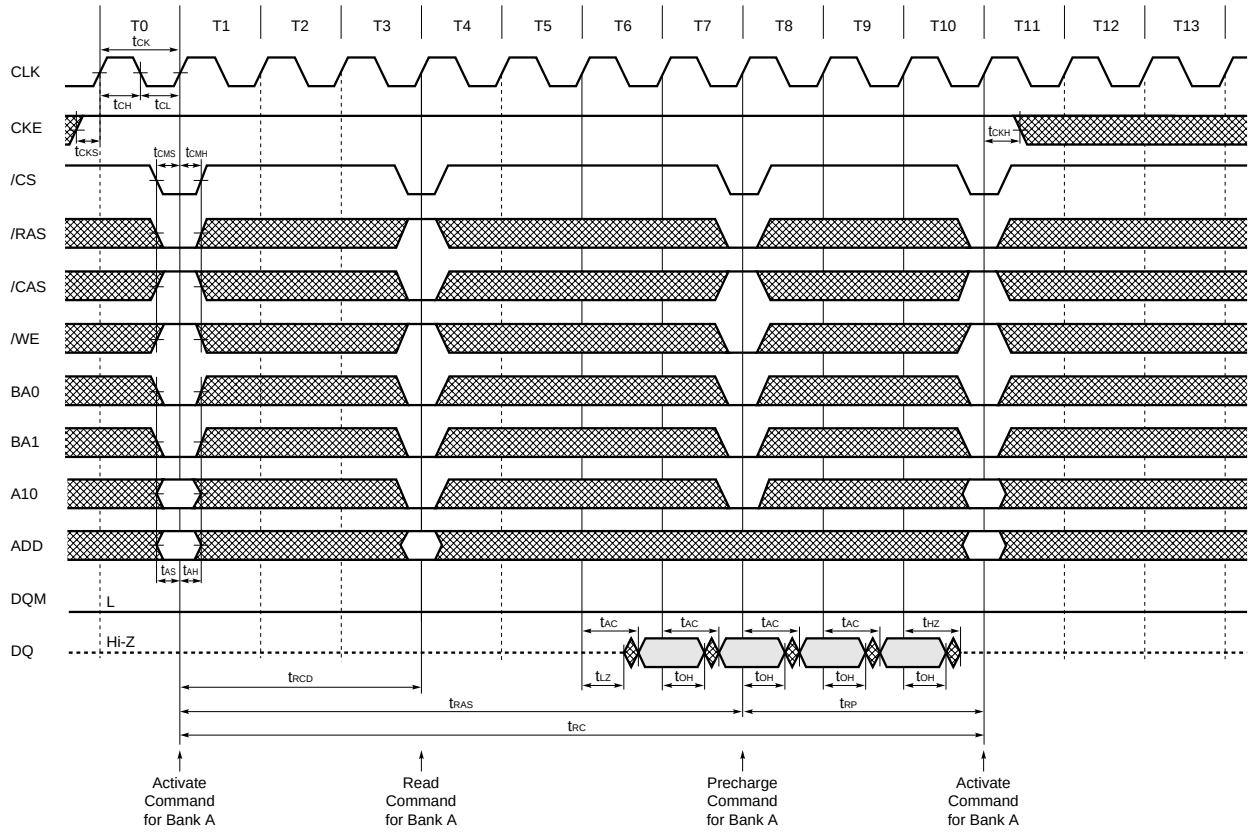
The write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



Precharge Termination in WRITE Cycle

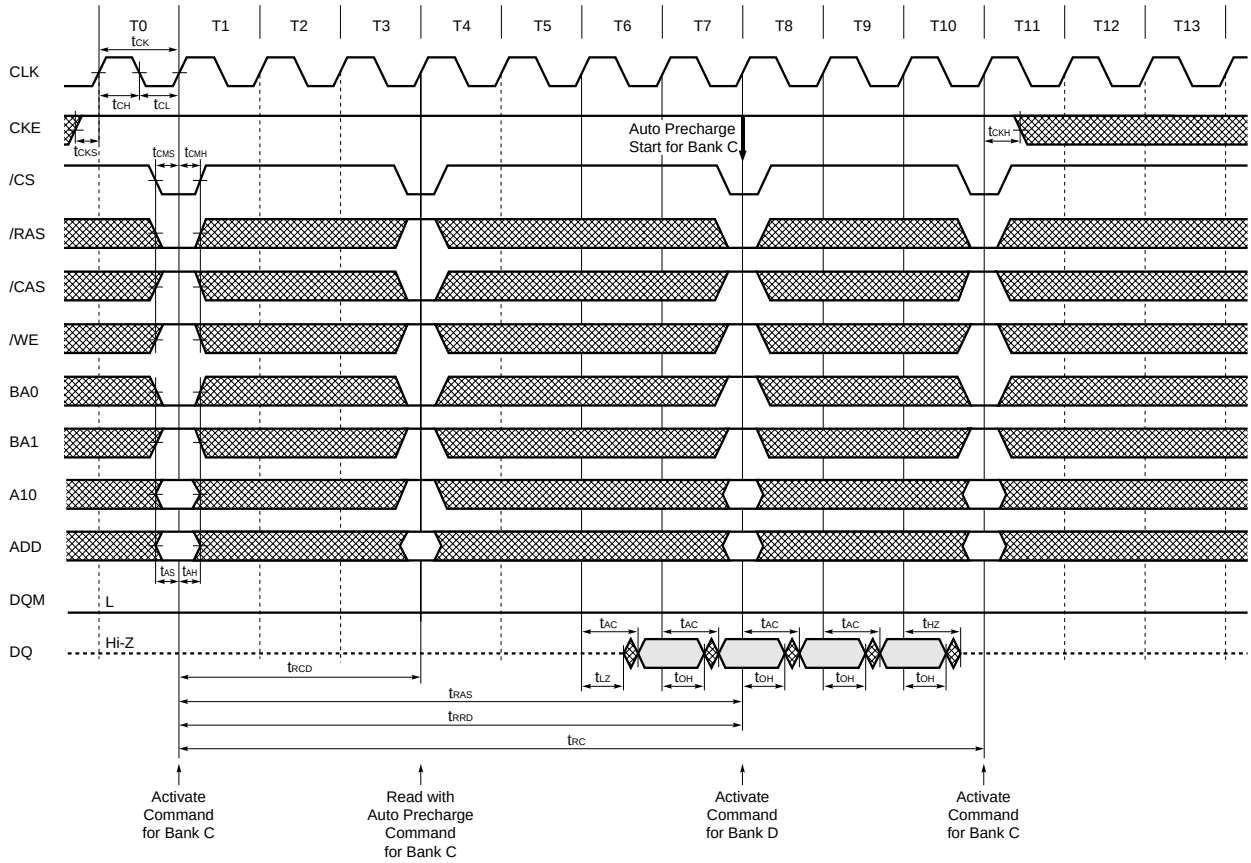
Timing Waveforms

AC Parameters for Read Timing with Manual Precharge



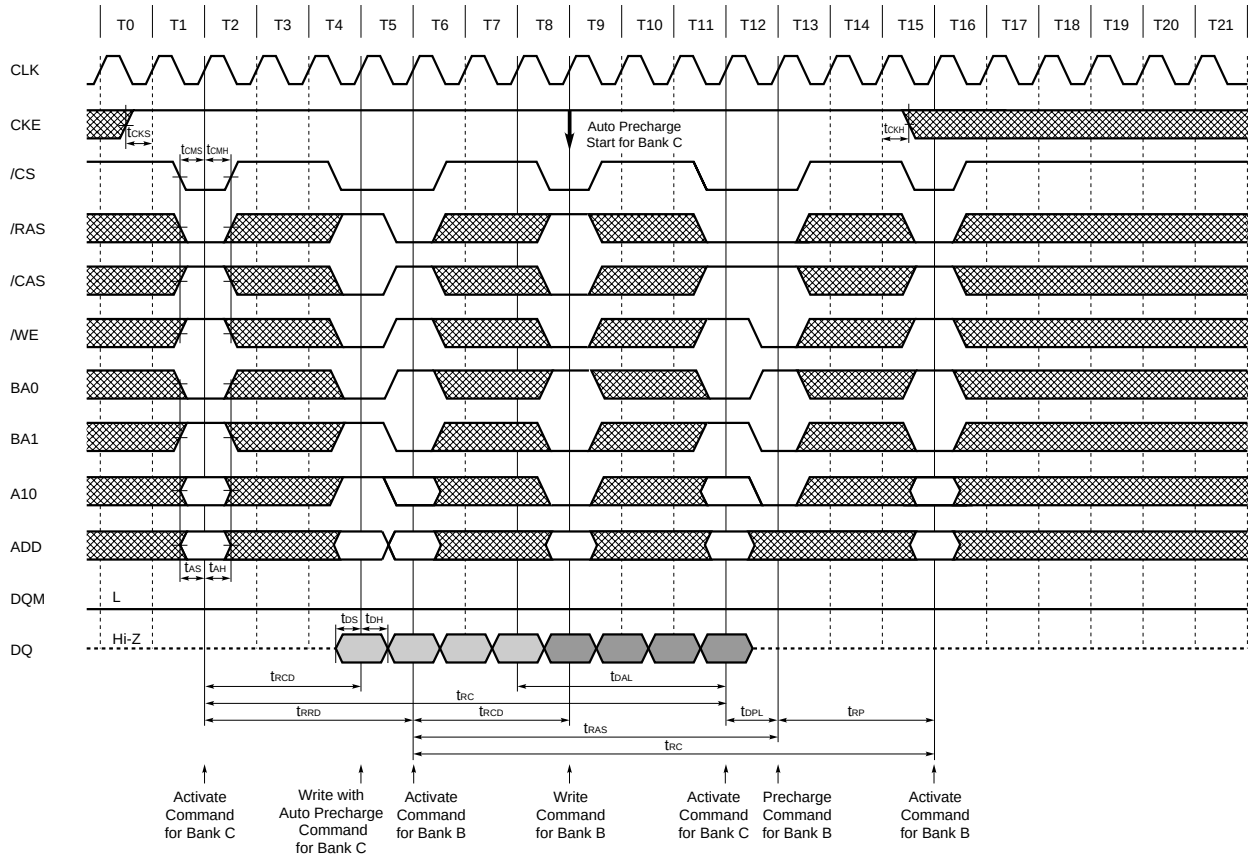
[Burst Length = 4, /CAS Latency = 3]

AC Parameters for Read Timing with Auto Precharge



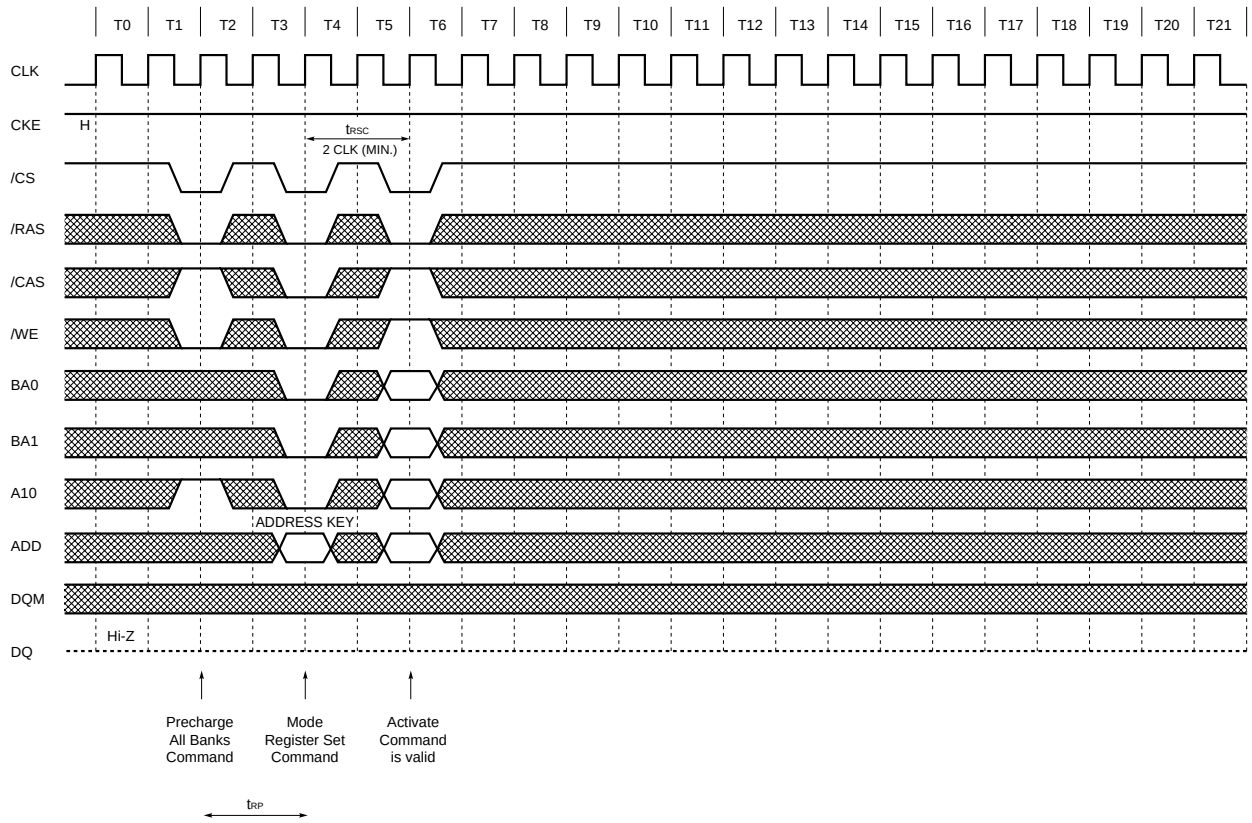
[Burst Length = 4, /CAS Latency = 3]

AC Parameters for Write Timing

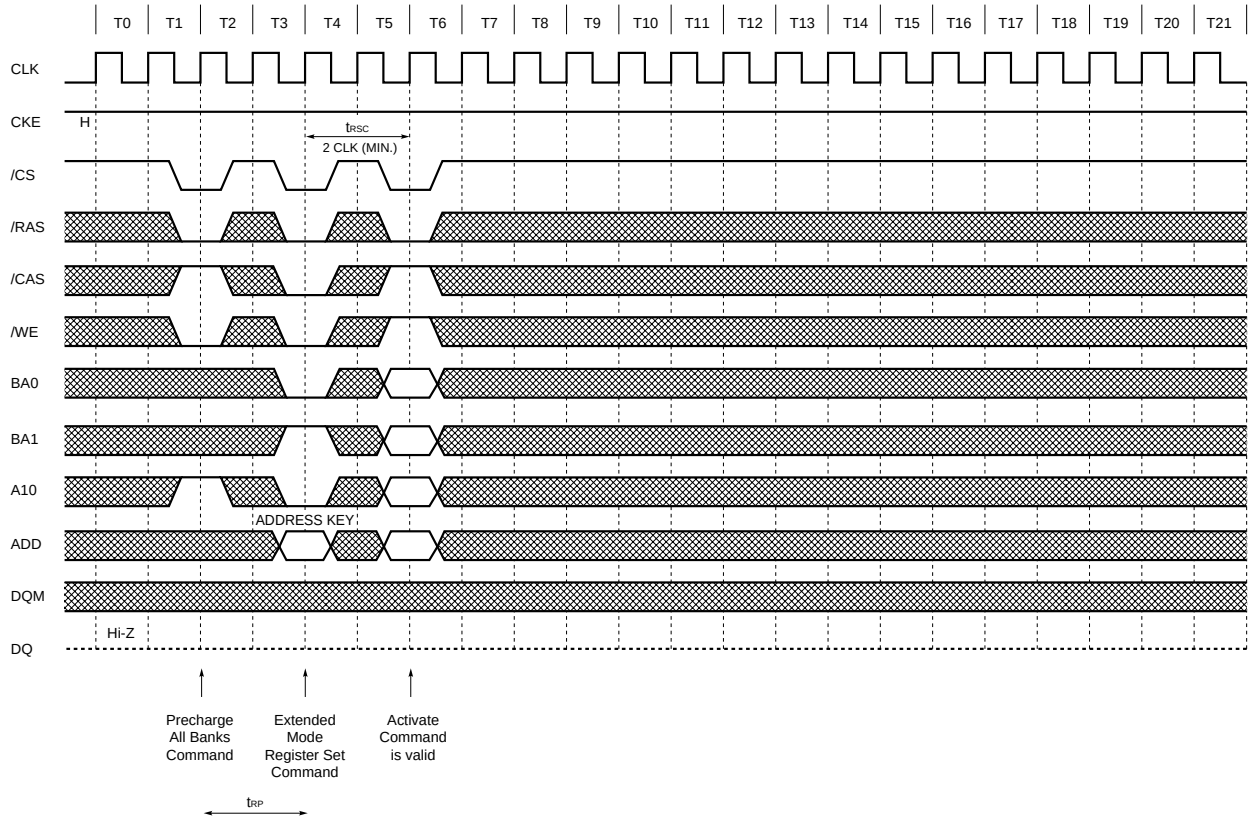


[Burst Length = 4]

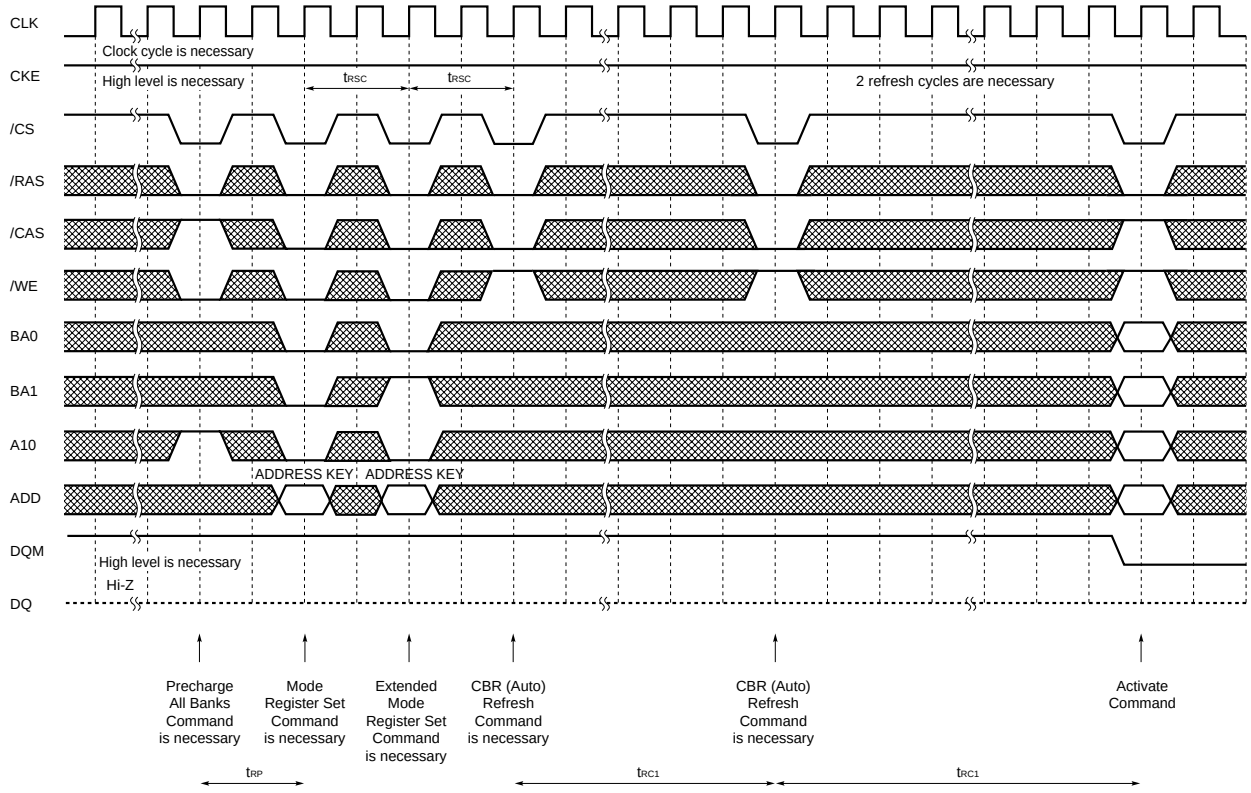
Mode Register Set



Extended Mode Register Set

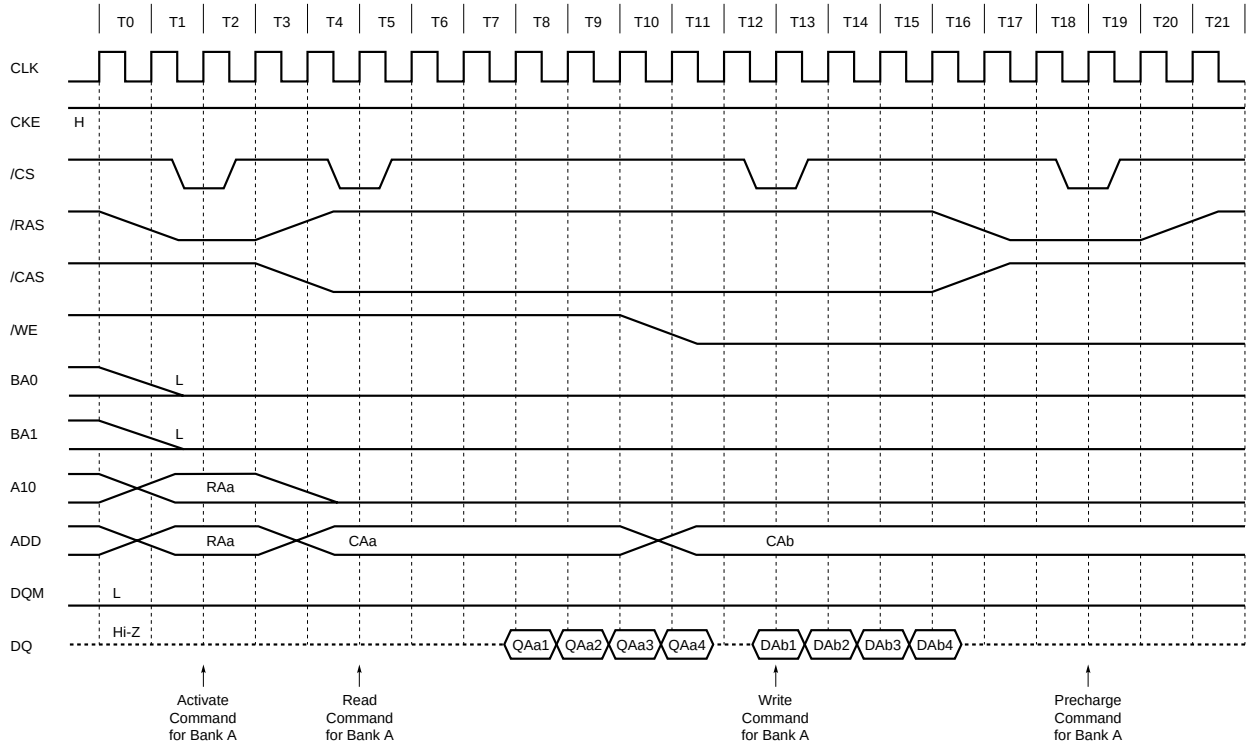


Power On Sequence



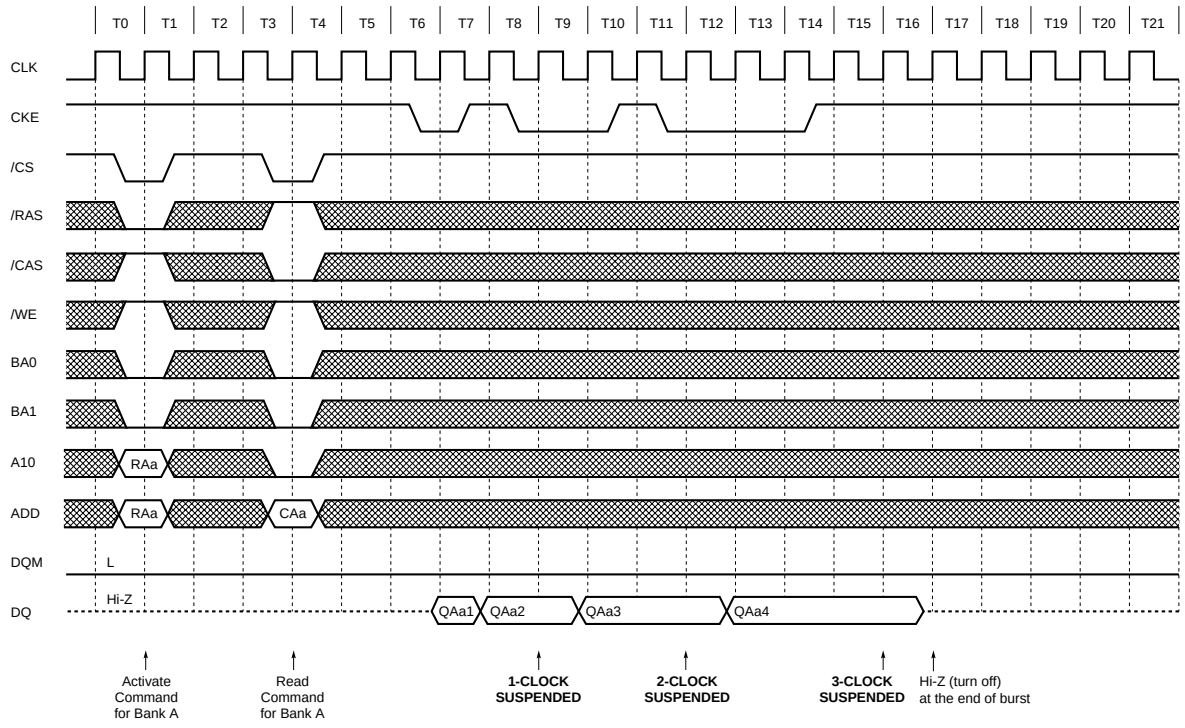
/CS Function

Only /CS signal needs to be issued at minimum rate

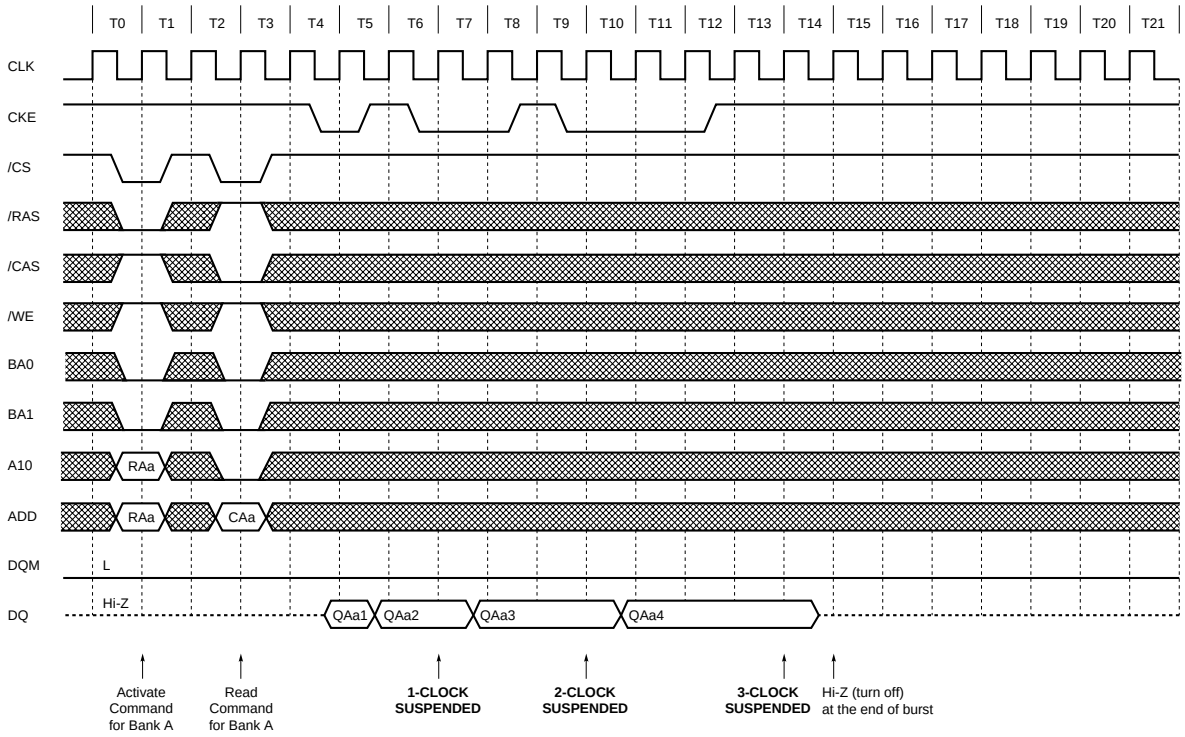


[Burst Length = 4, /CAS Latency = 3]

Clock Suspension during Burst Read

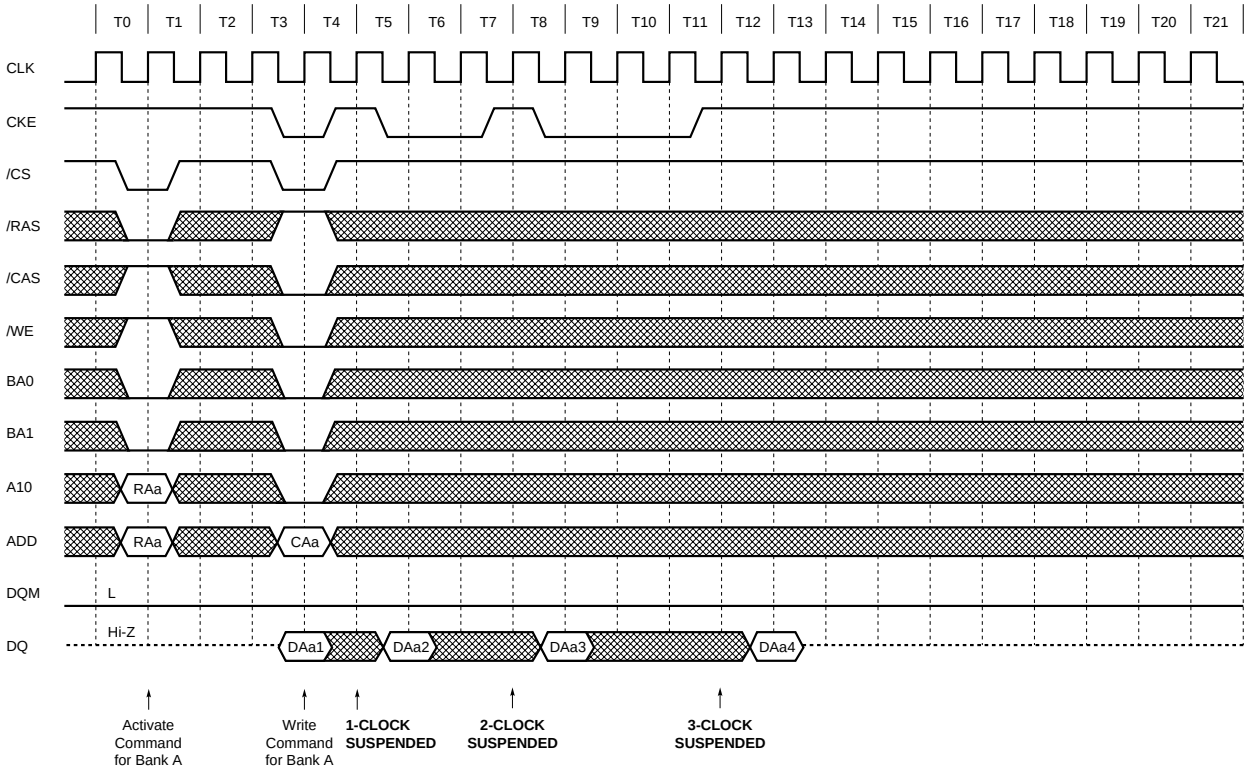


[Burst Length = 4, /CAS Latency = 3]

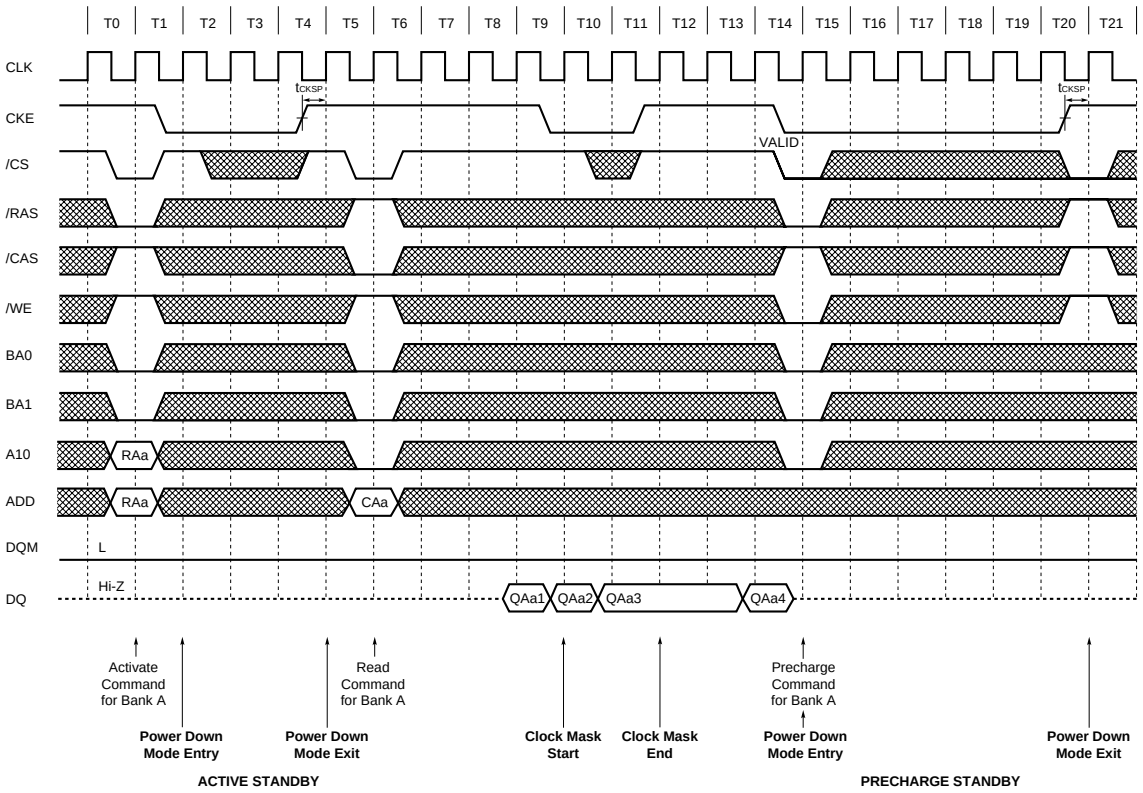


[Burst Length = 4, /CAS Latency = 2]

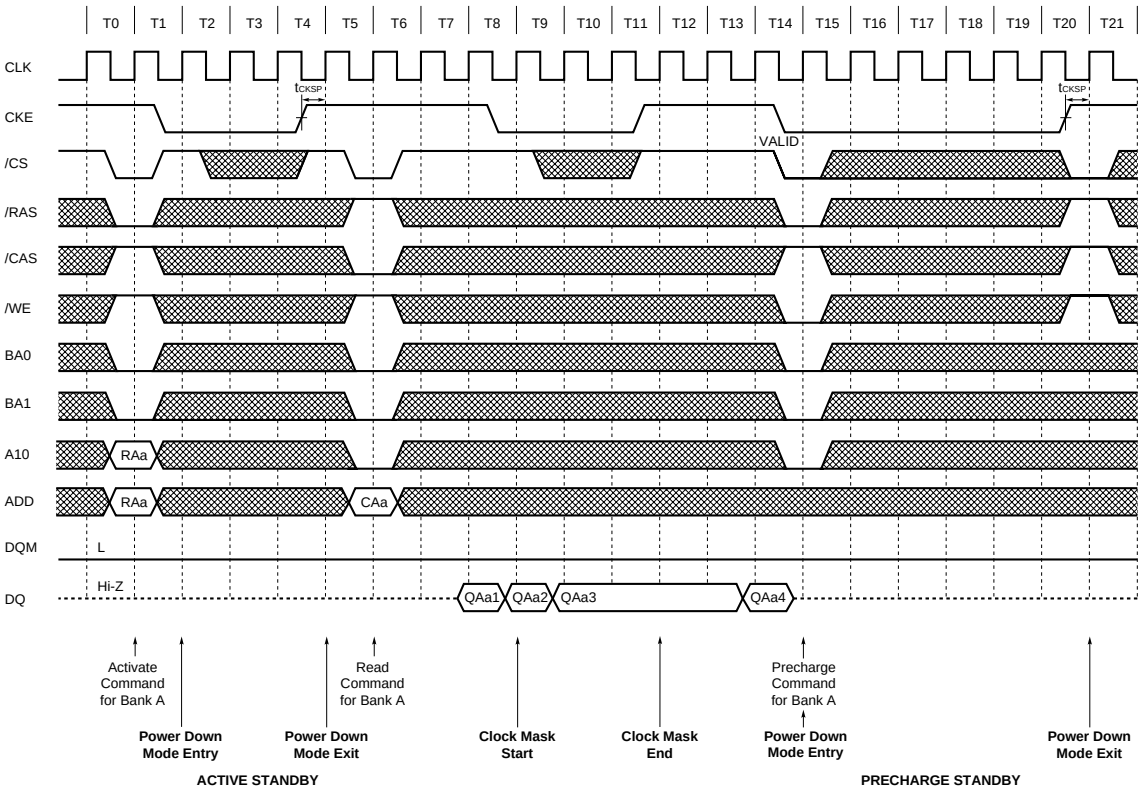
Clock Suspension during Burst Write



Power Down Mode and Clock Mask

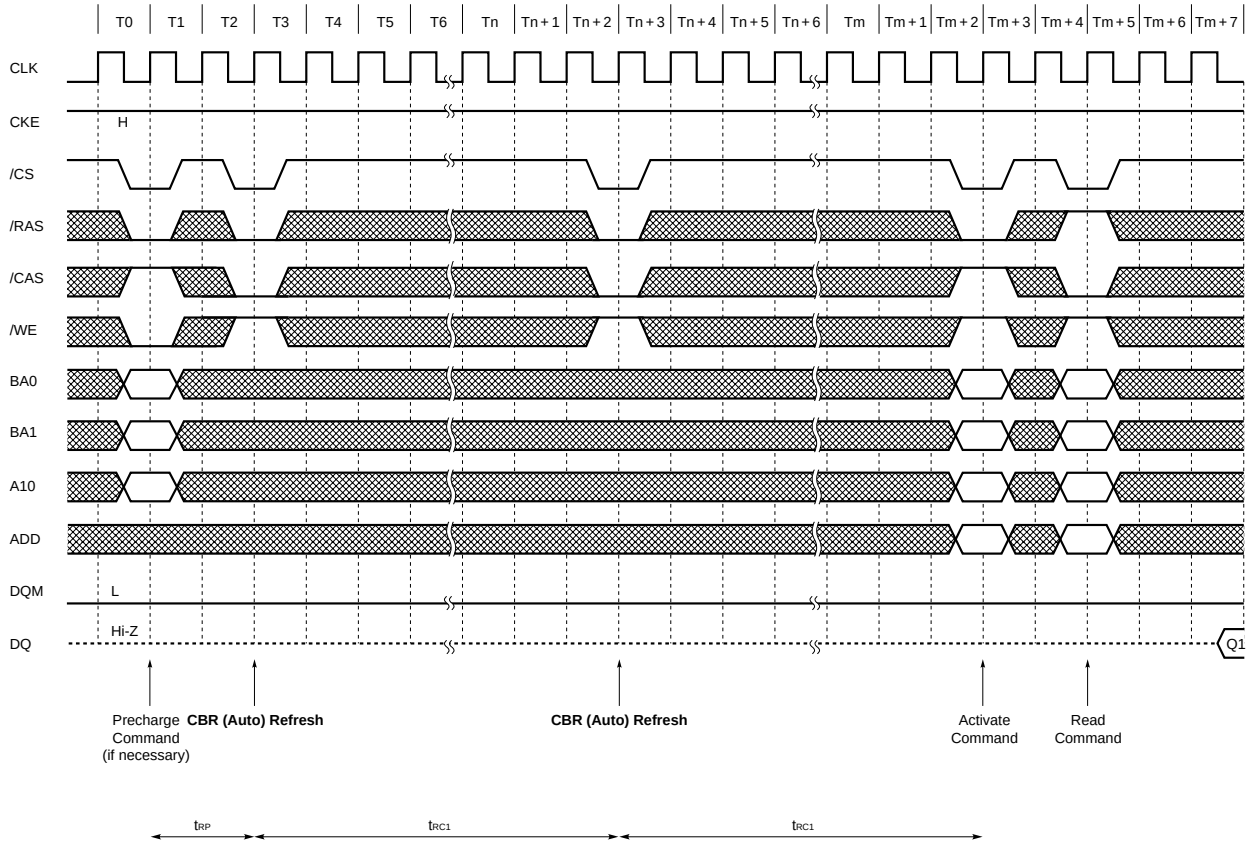


[Burst Length = 4, /CAS Latency = 3]

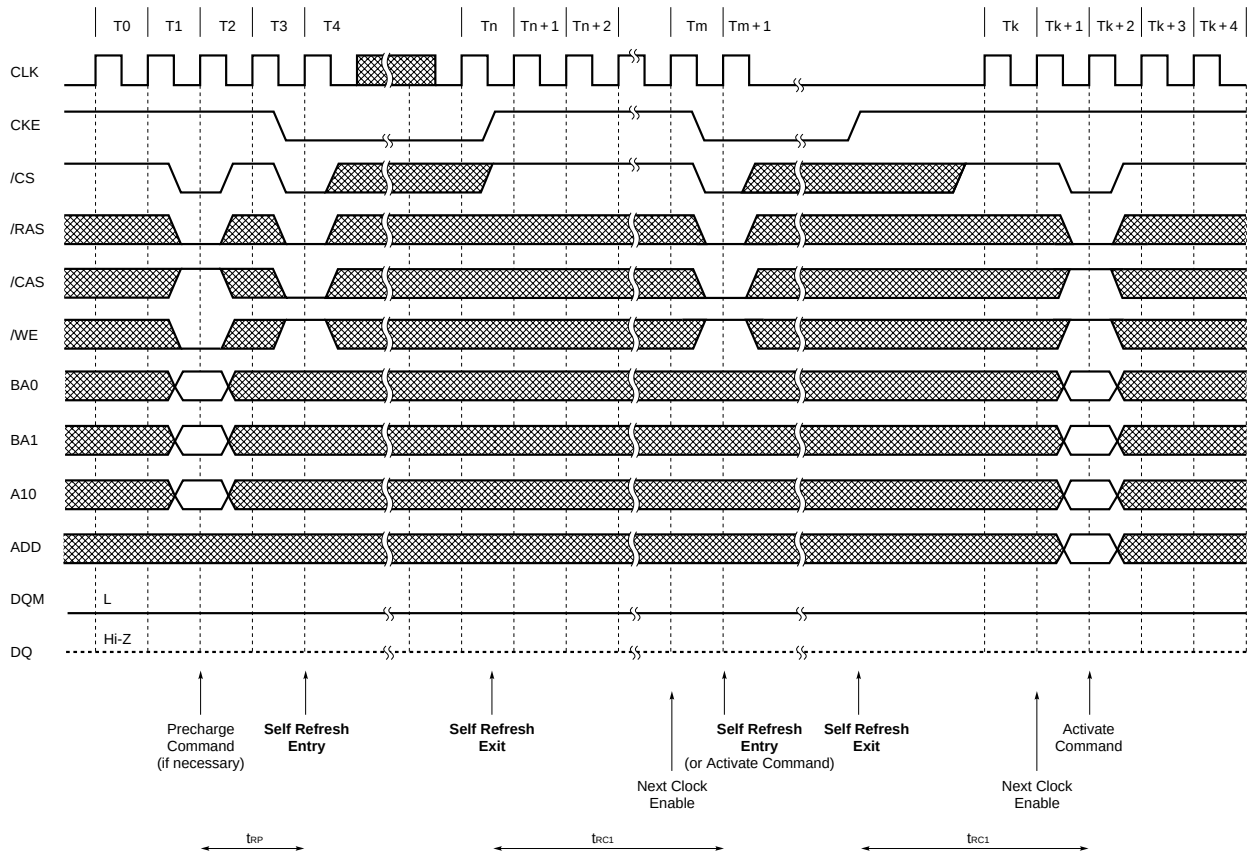


[Burst Length = 4, /CAS Latency = 2]

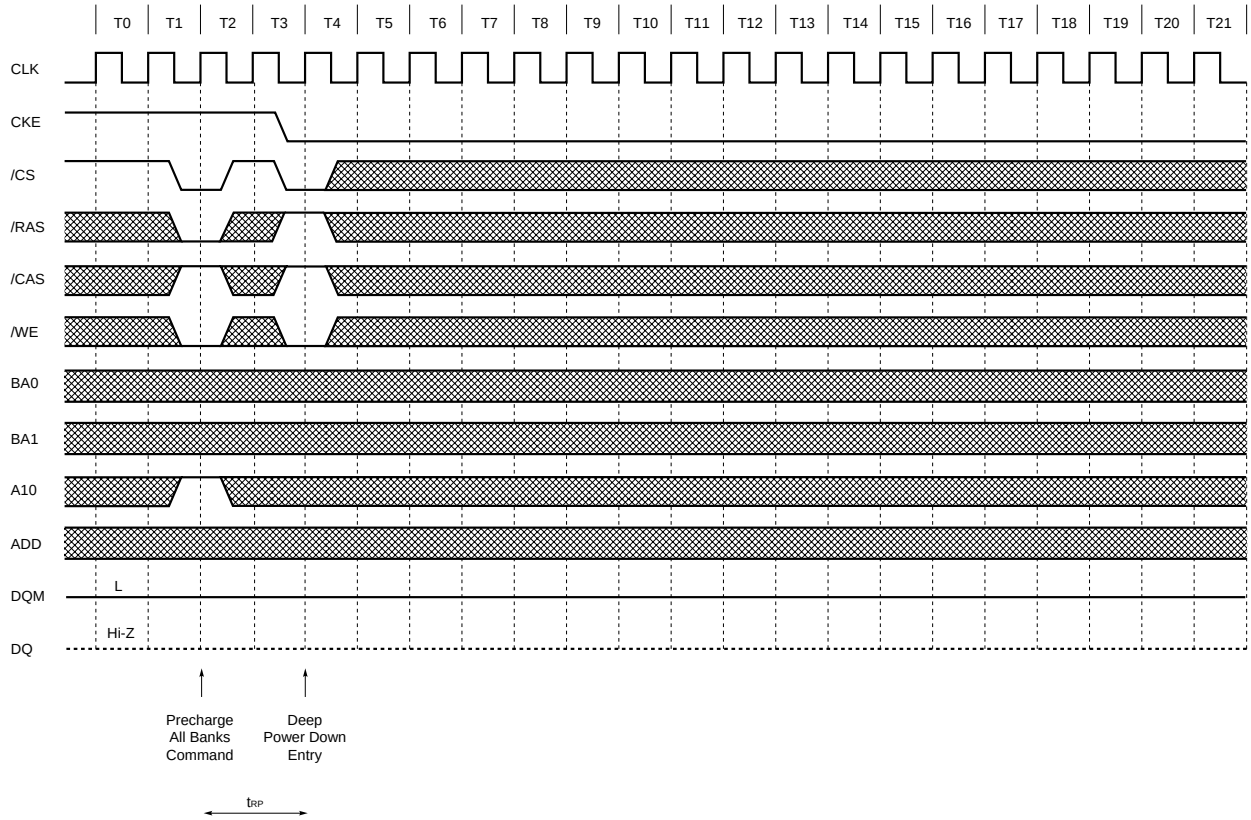
Auto Refresh



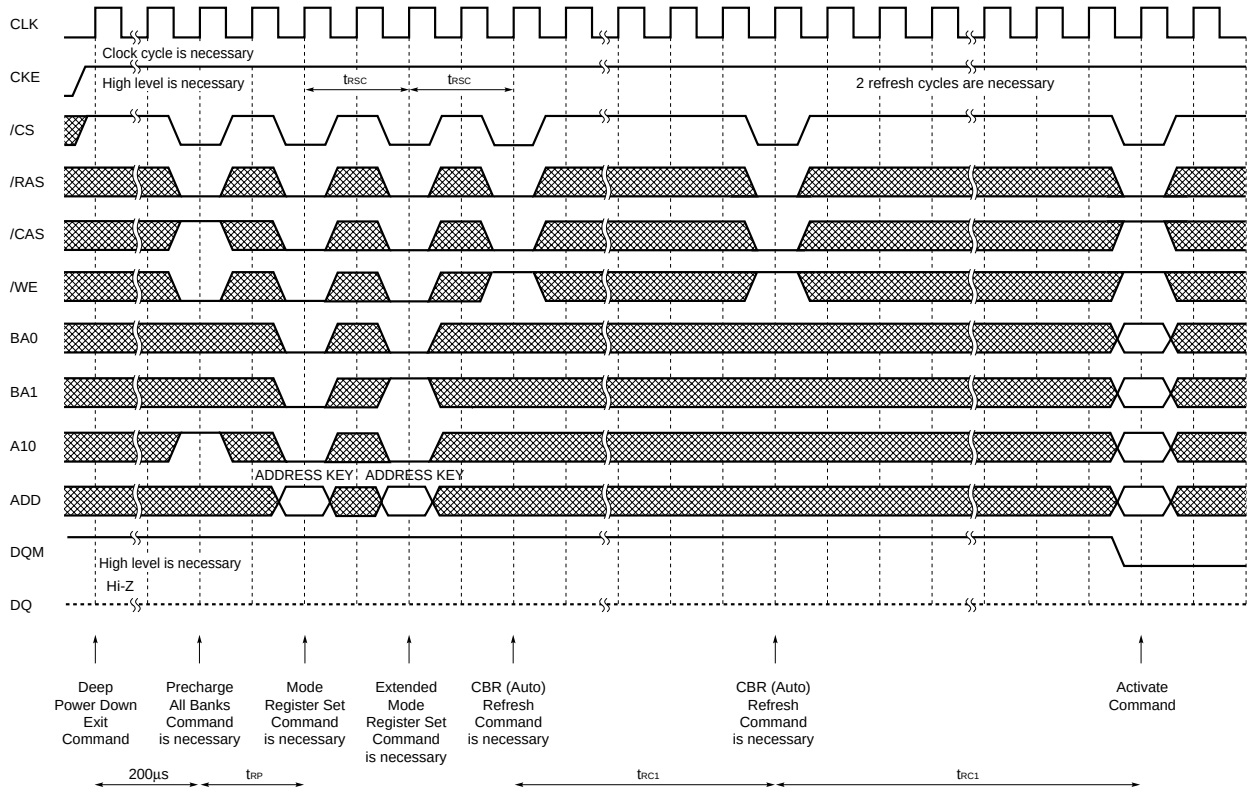
Self Refresh (Entry and Exit)



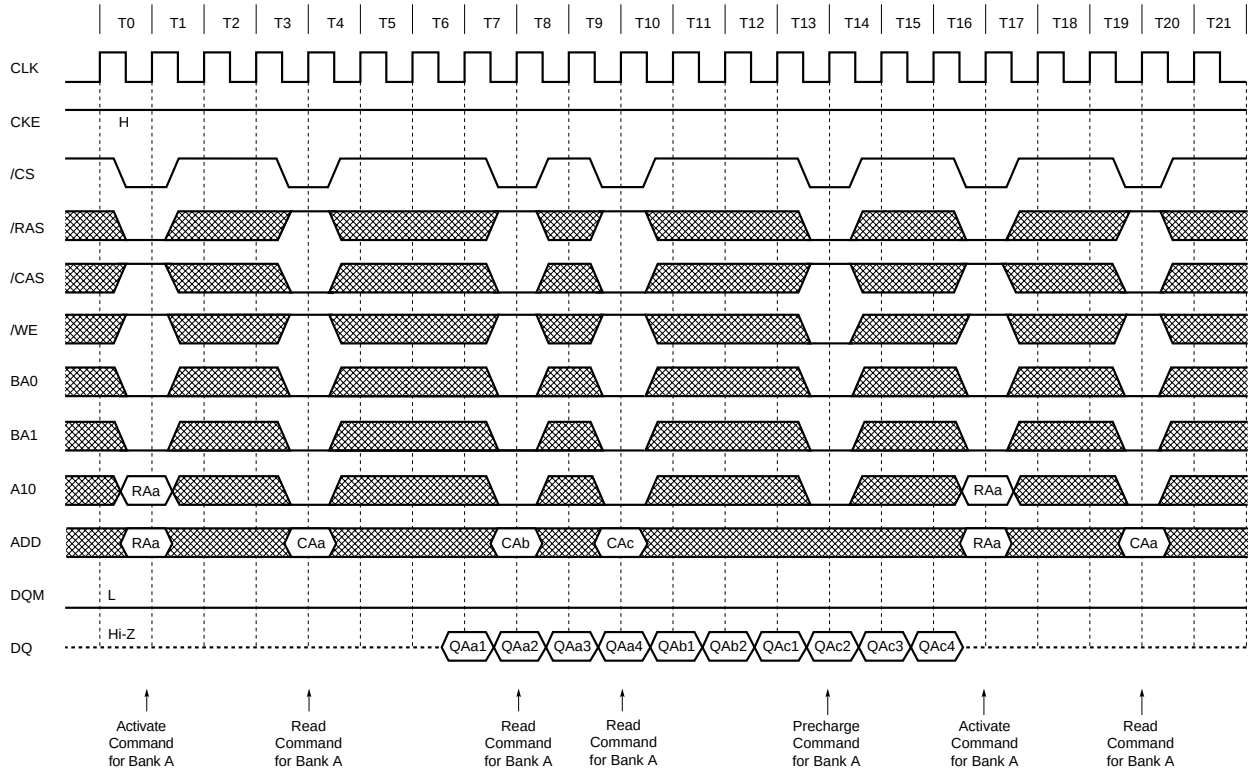
Deep Power Down Entry



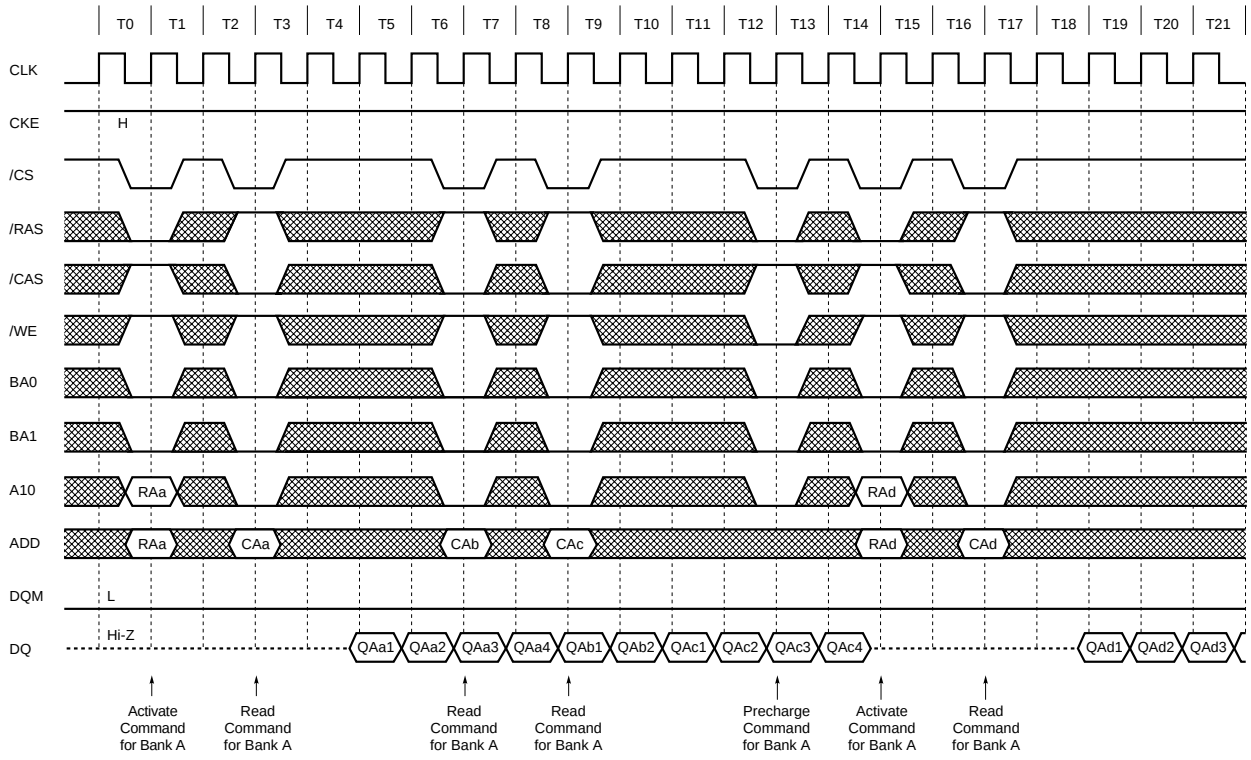
Deep Power Down Exit



Random Column Read

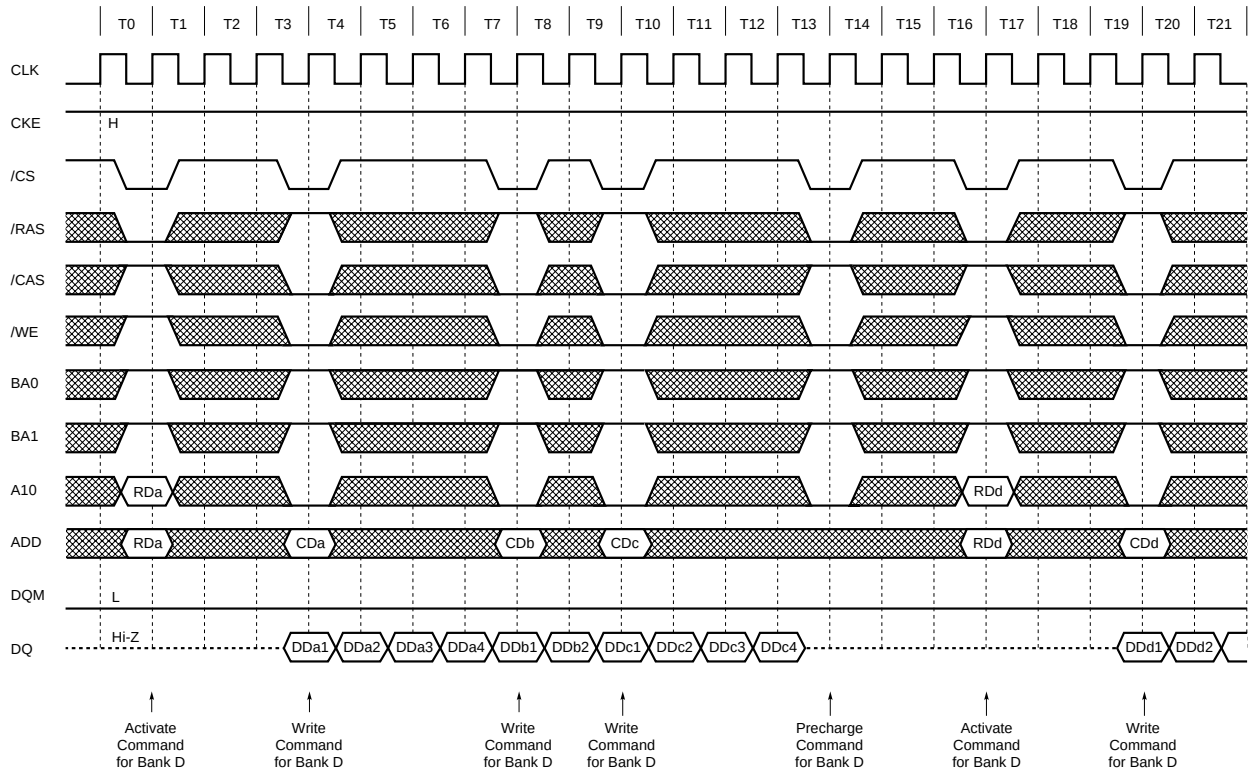


[Burst Length = 4, /CAS Latency = 3]



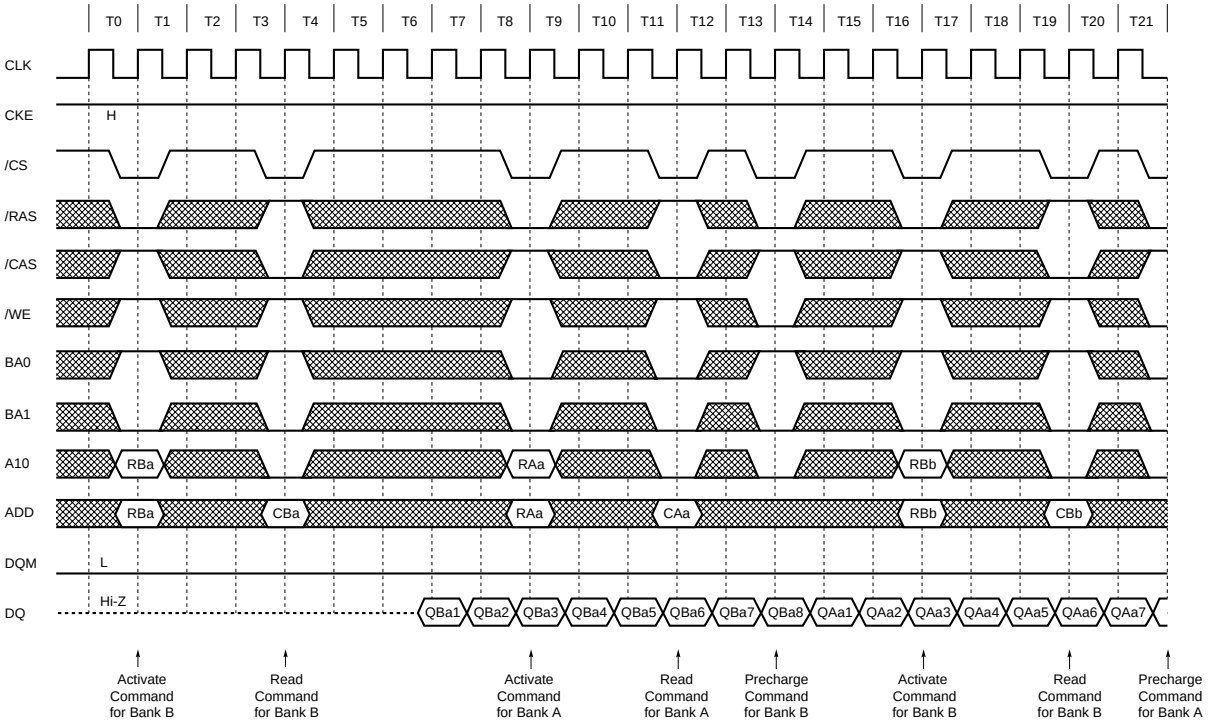
[Burst Length = 4, /CAS Latency = 2]

Random Column Write

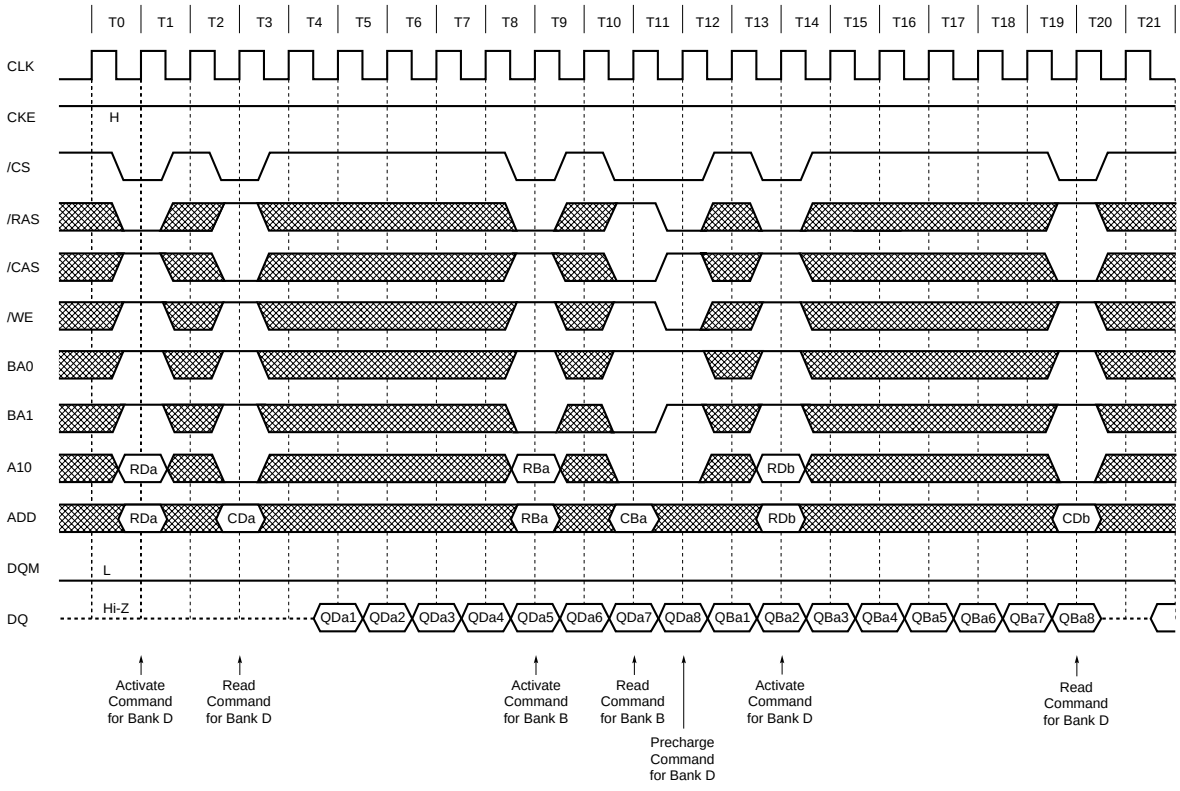


[Burst Length = 4]

Random Row Read

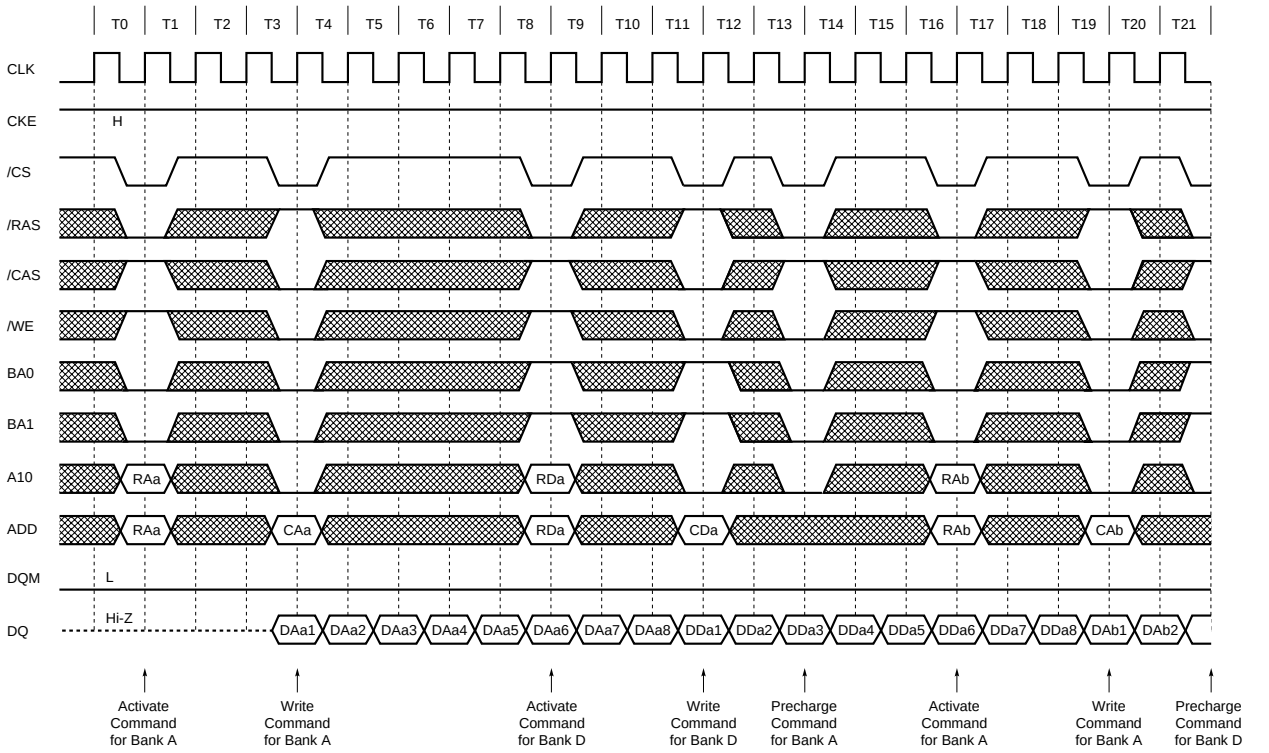


[Burst Length = 8, /CAS Latency = 3]



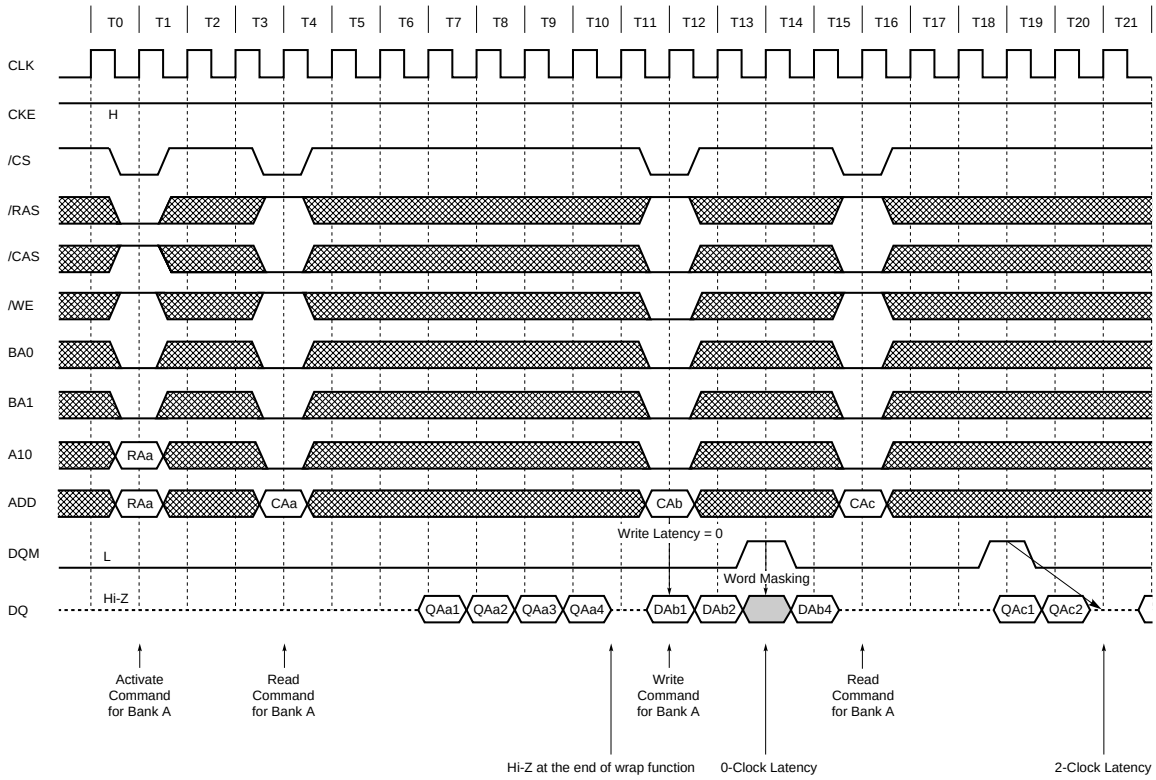
[Burst Length = 8, /CAS Latency = 2]

Random Row Write

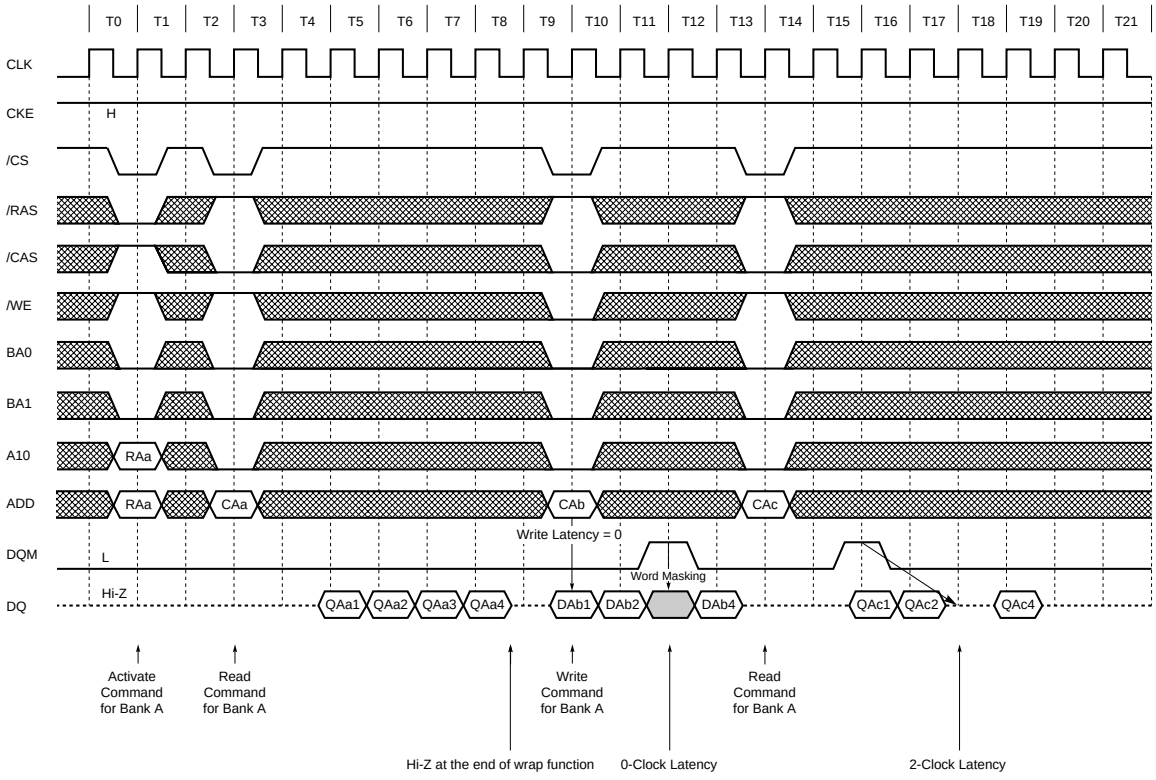


[Burst Length = 8]

Read and Write

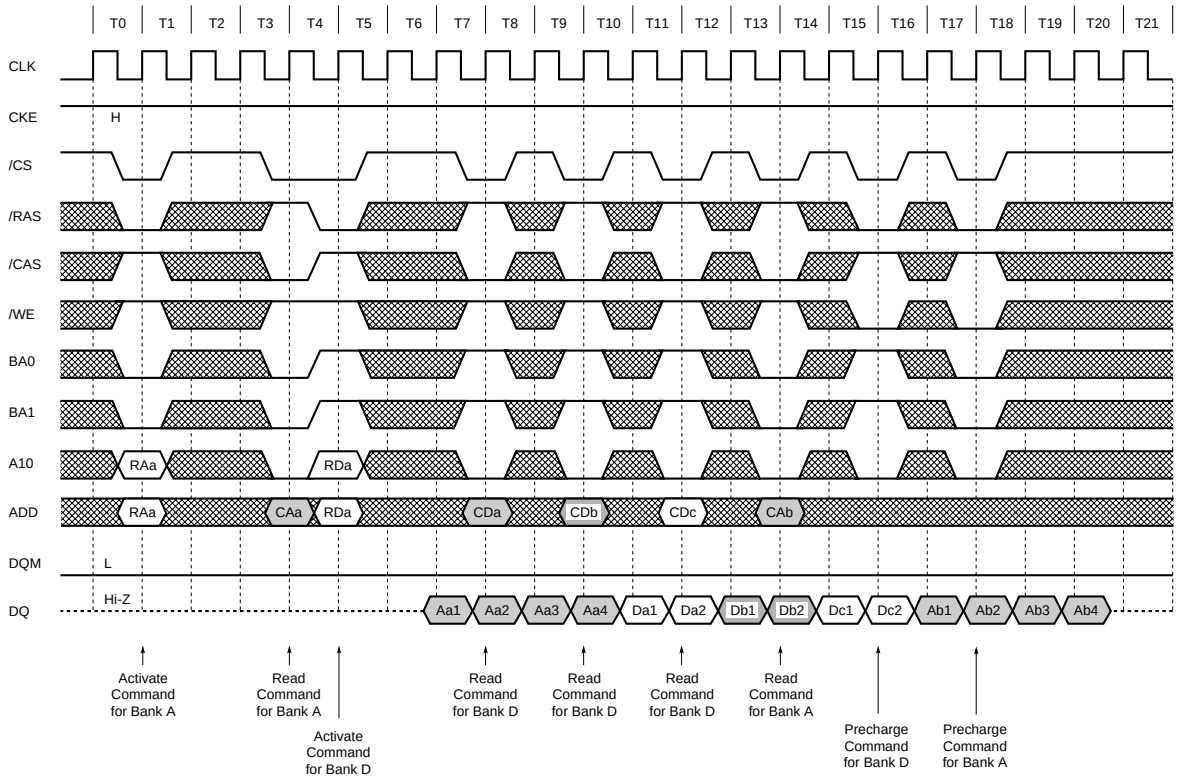


[Burst Length = 4, /CAS Latency = 3]

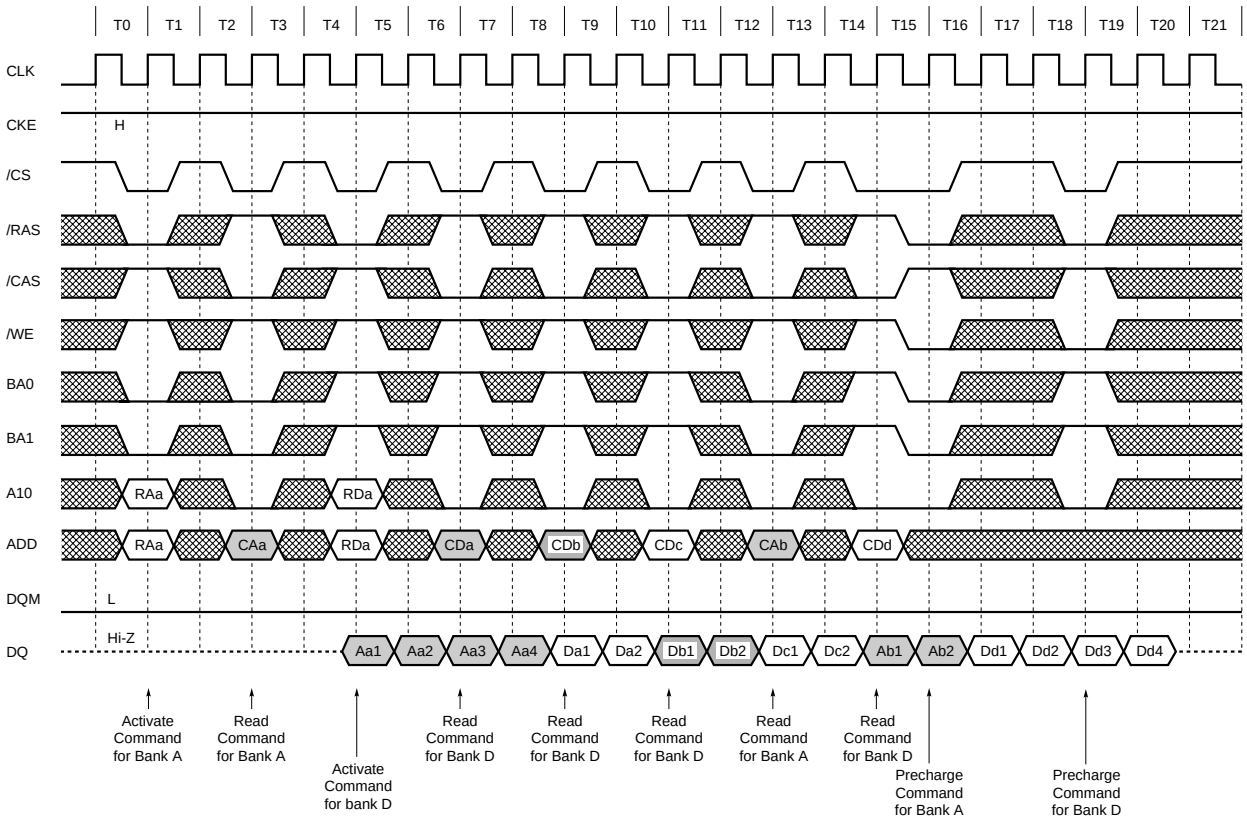


[Burst Length = 4, /CAS Latency = 2]

Interleaved Column Read Cycle

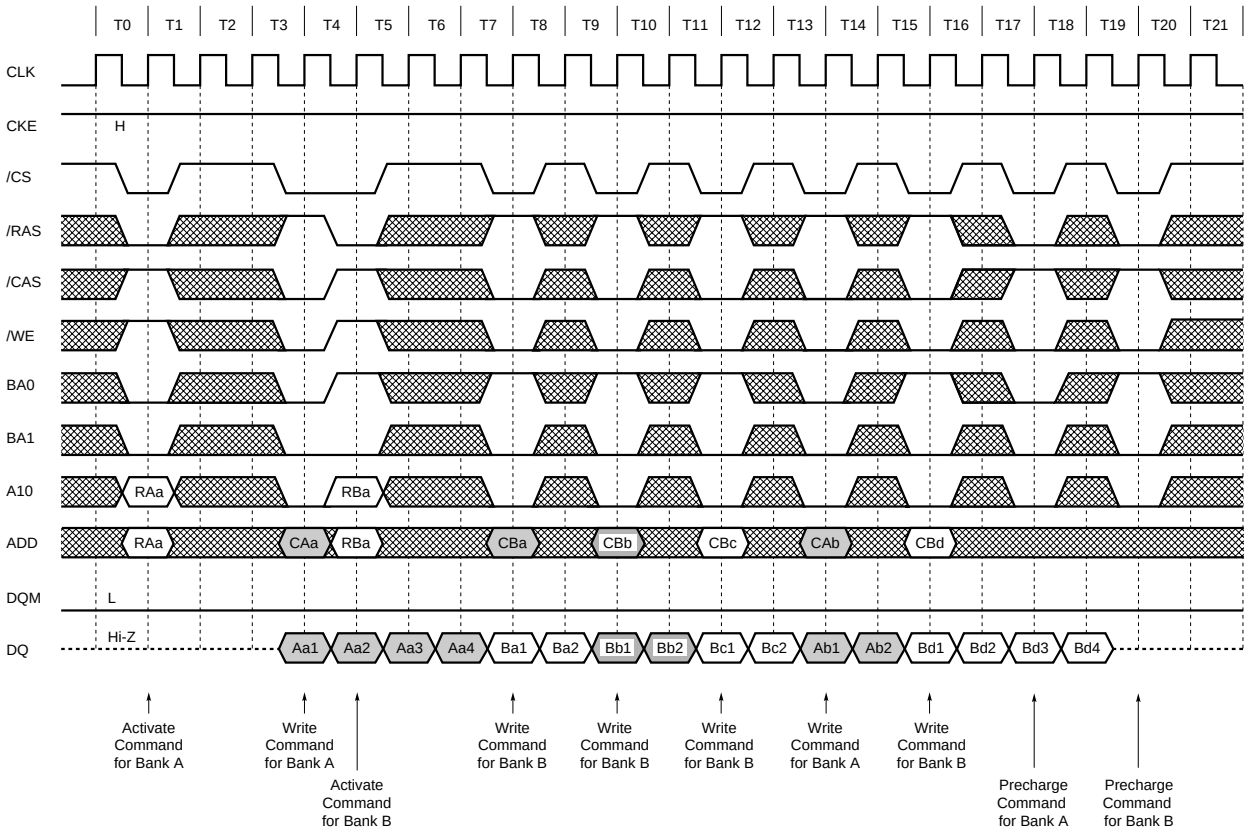


[Burst Length = 4, /CAS Latency = 3]



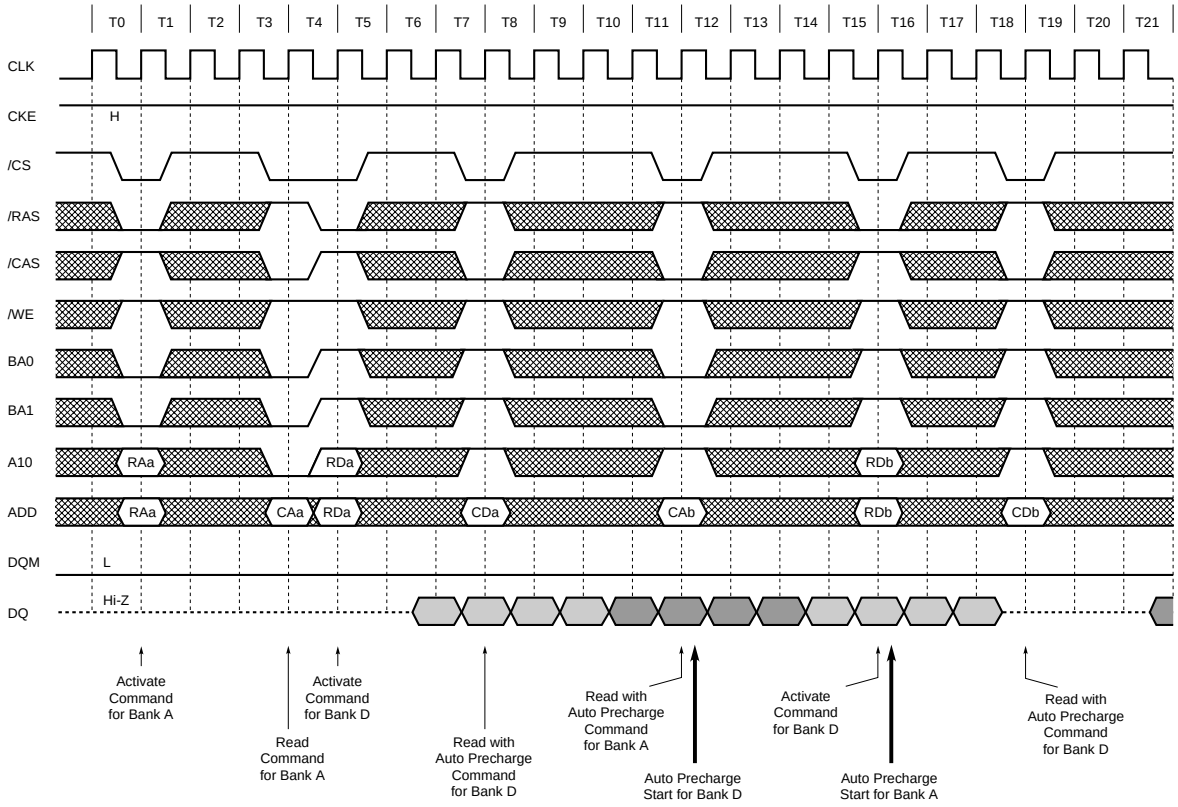
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Interleaved Column Write Cycle

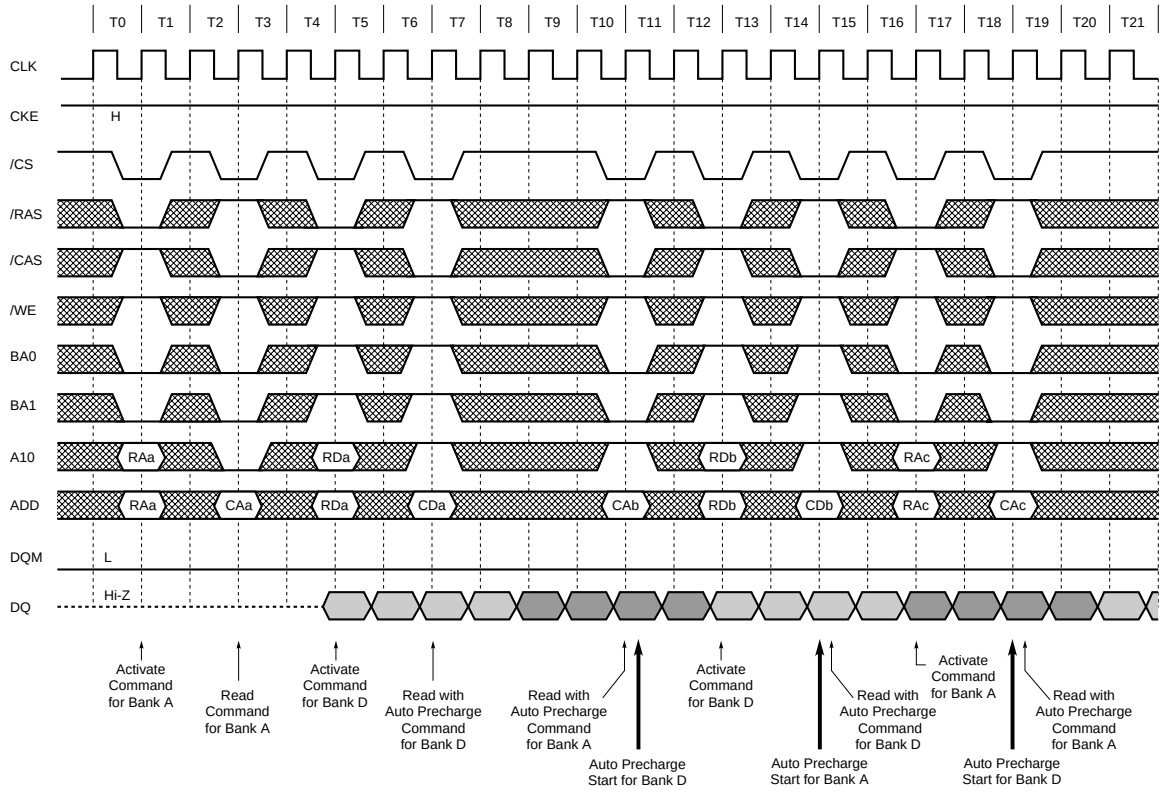


[Burst Length = 4]

Auto Precharge after Read Burst

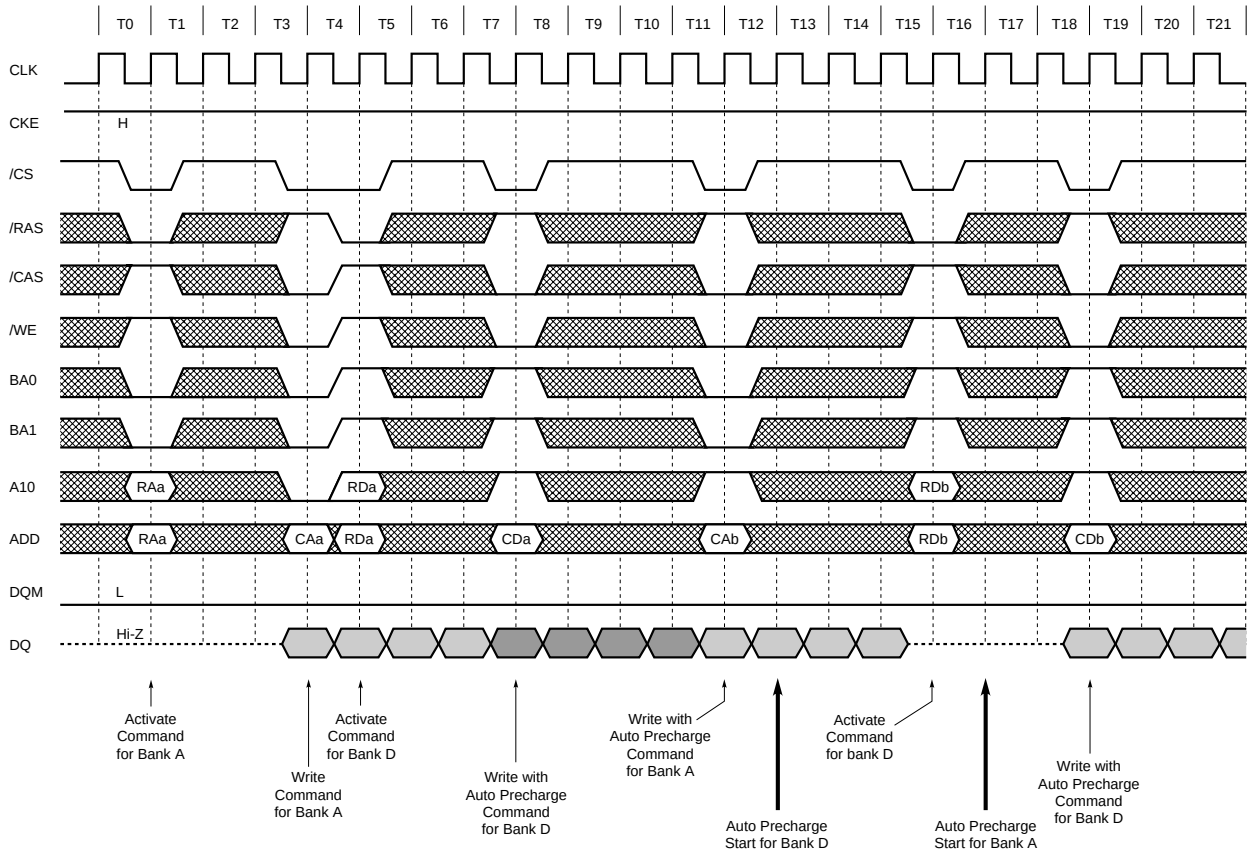


[Burst Length = 4, /CAS Latency = 3]



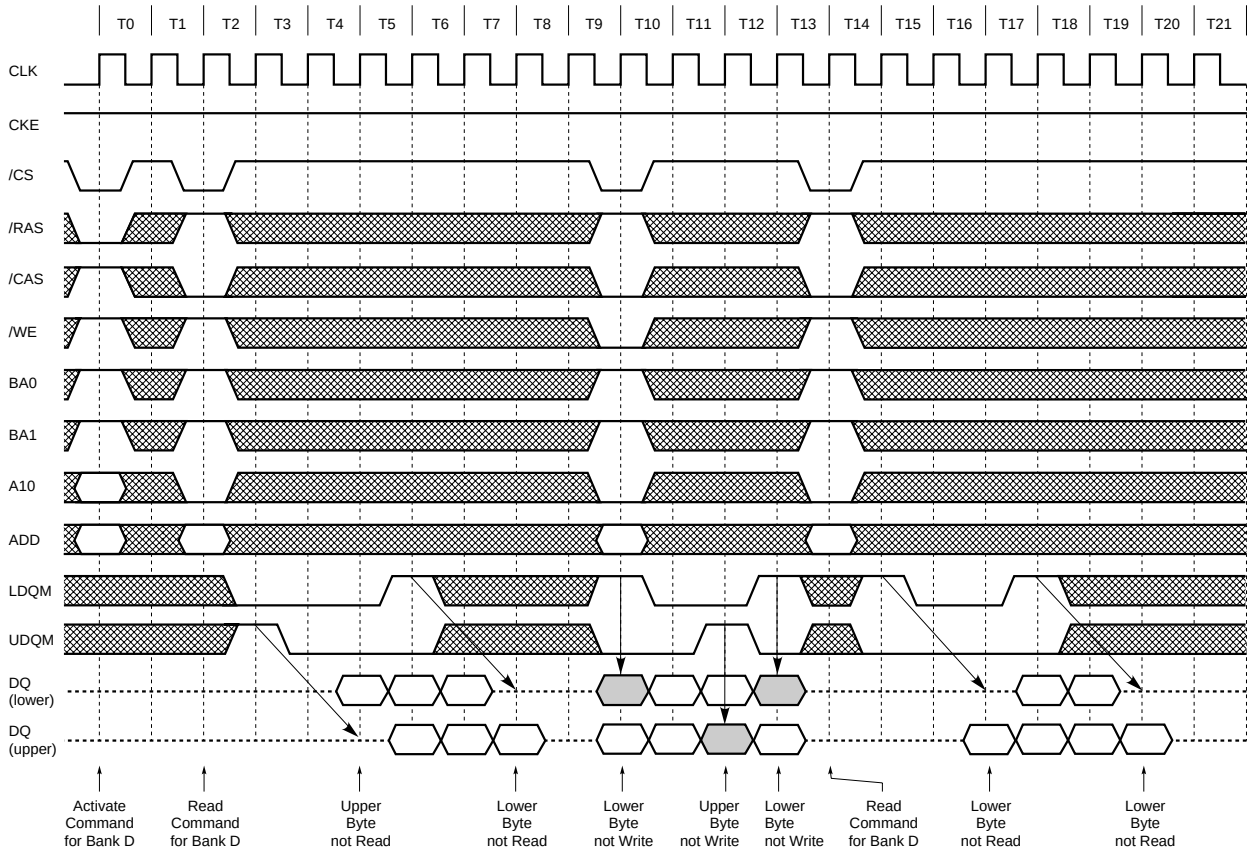
[Burst Length = 4, /CAS Latency = 2]

Auto Precharge after Write Burst



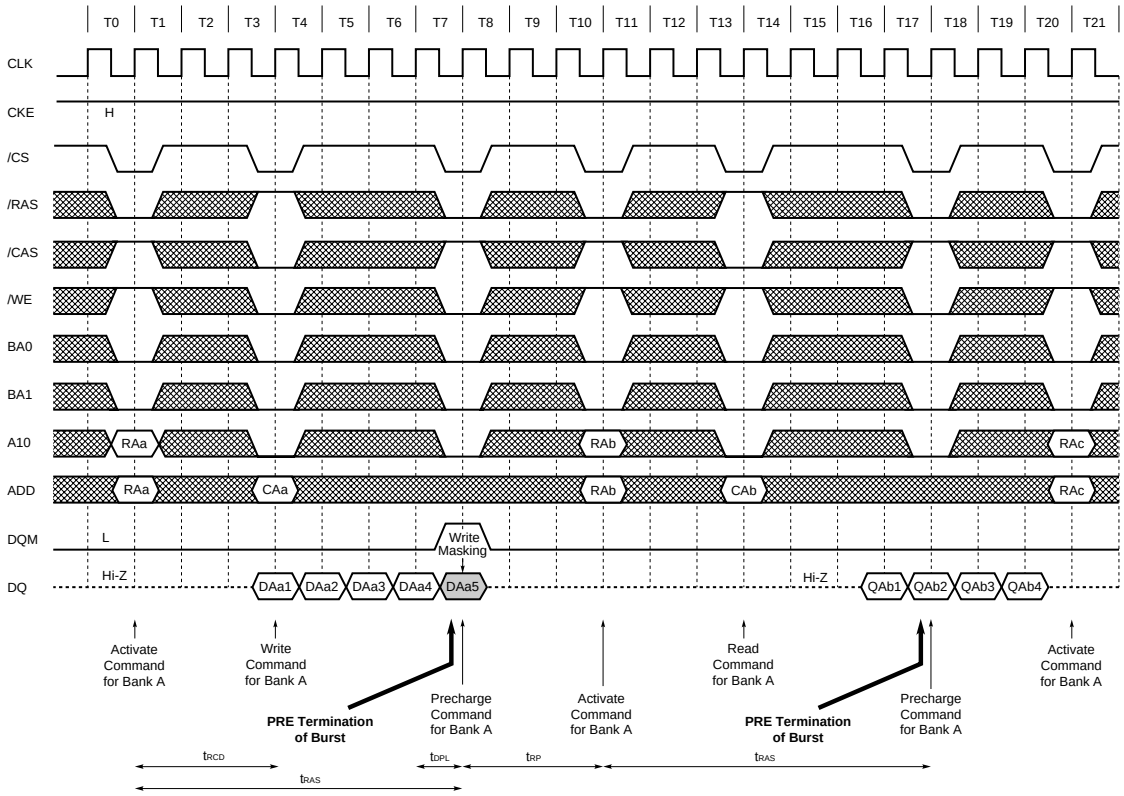
[Burst Length = 4]

Burst Write Operation

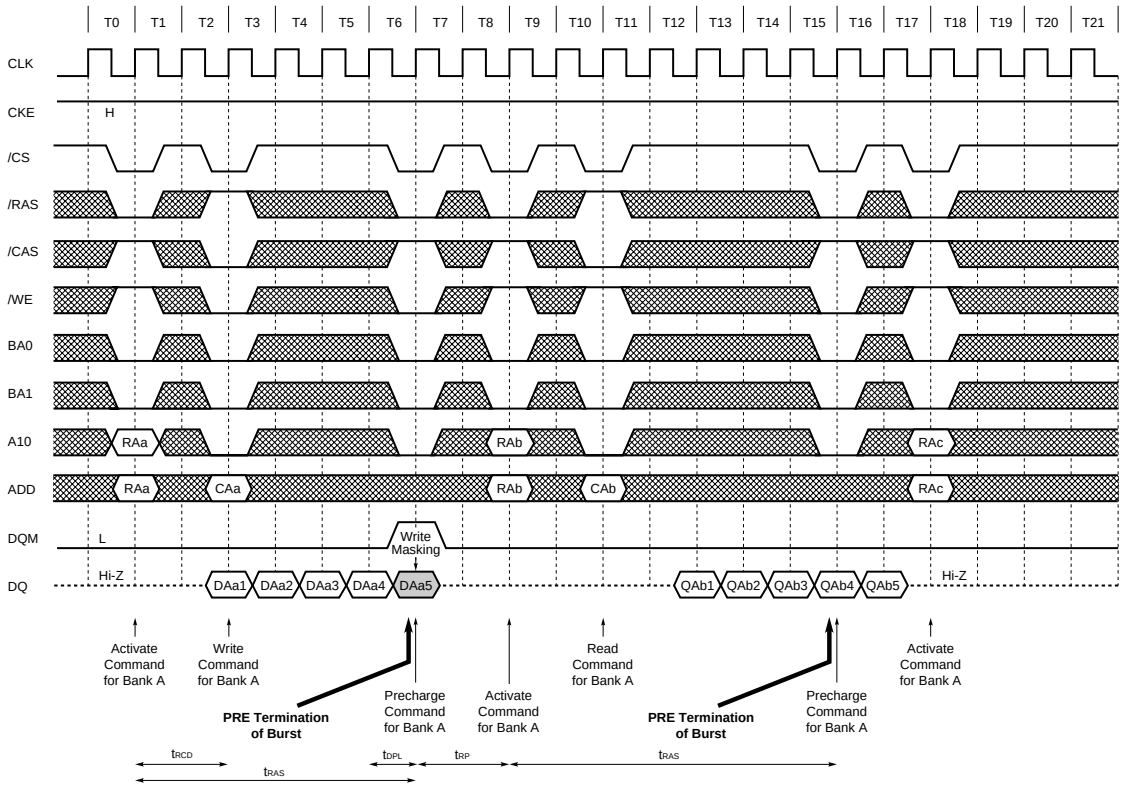


[Burst Length = 4]

Precharge Termination



[Burst Length = 8, /CAS Latency = 3]



[Burst Length = 8, /CAS Latency = 2]

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